19-3543; Rev 0; 2/05

EVALUATION KIT AVAILABLE

Dual, 65Msps, 12-Bit, IF/Baseband ADC

MAX12527

General Description

The MAX12527 is a dual 3.3V, 12-bit analog-to-digital converter (ADC) featuring fully differential wideband track-and-hold (T/H) inputs, driving internal quantizers. The MAX12527 is optimized for low power, small size, and high dynamic performance in intermediate frequency (IF) and baseband sampling applications. This dual ADC operates from a single 3.3V supply, consuming only 620mW while delivering a typical 69.8dB signal-to-noise ratio (SNR) performance at a 175MHz input frequency. The T/H input stages accept single-ended or differential inputs up to 400MHz. In addition to low operating power, the MAX12527 features a 166µW power-down mode to conserve power during idle periods.

A flexible reference structure allows the MAX12527 to use the internal 2.048V bandgap reference or accept an externally applied reference and allows the reference to be shared between the two ADCs. The reference structure allows the full-scale analog input range to be adjusted from ±0.35V to ±1.15V. The MAX12527 provides a common-mode reference to simplify design and reduce external component count in differential analog input circuits.

The MAX12527 supports either a single-ended or differential input clock. User-selectable divide-by-two (DIV2) and divide-by-four (DIV4) modes allow for design flexibility and help eliminate the negative effects of clock jitter. Wide variations in the clock duty cycle are compensated with the ADC's internal duty-cycle equalizer (DCE).

The MAX12527 features two parallel, 12-bit-wide, CMOS-compatible outputs. The digital output format is pin-selectable to be either two's complement or Gray code. A separate power-supply input for the digital outputs accepts a 1.7V to 3.6V voltage for flexible interfacing with various logic levels. The MAX12527 is available in a 10mm x 10mm x 0.8mm, 68-pin thin QFN package with exposed paddle (EP), and is specified for the extended (-40°C to +85°C) temperature range.

For a 14-bit, pin-compatible version of this ADC, refer to the MAX12557 data sheet.

Applications

IF and Baseband Communication Receivers
Cellular, LMDS, Point-to-Point Microwave, MMDS, HFC, WLAN

I/Q Receivers

Ultrasound and Medical Imaging

Portable Instrumentation

Digital Set-Top Boxes

Low-Power Data Acquisition

Features

- **Direct IF Sampling Up to 400MHz**
- **Excellent Dynamic Performance**
  - **70.4dB/69.8dB SNR at f_{IN} = 70MHz/175MHz**
  - **84.4dBc/80.2dBc SFDR at f_{IN} = 70MHz/175MHz**
- **3.3V Low Power Operation**
  - **647mW (Differential Clock Mode)**
  - **620mW (Single-Ended Clock Mode)**
- **Fully Differential or Single-Ended Analog Input**
- **Adjustable Differential Analog Input Voltage**
- **750MHz Input Bandwidth**
- **Adjustable, Internal or External, Shared Reference**
- **Differential or Single-Ended Clock**
- **Accepts 25% to 75% Clock Duty Cycle**
- **User-Selectable DIV2 and DIV4 Clock Modes**
- **Power-Down Mode**
- **CMOS Outputs in Two's Complement or Gray Code**
- **Out-of-Range and Data-Valid Indicators**
- **Small, 68-Pin Thin QFN Package**
- **14-Bit Compatible Version Available (MAX12557)**
- **Evaluation Kit Available (Order MAX12527 EV Kit)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX12527ETK	-40°C to +85°C	68 Thin QFN-EP* (10mm x 10mm x 0.8mm)

*EP = Exposed paddle.

Selector Guide

PART	SAMPLING RATE (Msps)	RESOLUTION (Bits)
MAX12557	65	14
MAX12527	65	12

Pin Configuration appears at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ....-0.3V to +3.6V
OV_{DD} to GND............-0.3V to the lower of (V_{DD} + 0.3V) and +3.6V
INAP, INAN to GND ...-0.3V to the lower of (V_{DD} + 0.3V) and +3.6V
INBP, INBN to GND ...-0.3V to the lower of (V_{DD} + 0.3V) and +3.6V
CLKP, CLKN to
GND ....-0.3V to the lower of (V_{DD} + 0.3V) and +3.6V
REFIN, REFOUT
to GND ....-0.3V to the lower of (V_{DD} + 0.3V) and +3.6V
REFAP, REFAN,
COMA to GND ......-0.3V to the lower of (V_{DD} + 0.3V) and +3.6V
REFBP, REFBN,
COMB to GND ......-0.3V to the lower of (V_{DD} + 0.3V) and +3.6V

DIFFCLK/$\overline{\text{SECLK}}$, G/$\overline{\text{T}}$, PD, SHREF, DIV2,
DIV4 to GND ....-0.3V to the lower of (V_{DD} + 0.3V) and +3.6V
D0A–D11A, D0B–D11B, DAV,
DORA, DORB to GND..............................-0.3V to (OV_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
68-Pin Thin QFN 10mm x 10mm x 0.8mm
(derate 70mW/°C above +70°C) 4000mW
Operating Temperature Range................................-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering 10s)......................................+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference), $C_L \approx$ 10pF at digital outputs, V_{IN} = -0.5dBFS (differential), DIFFCLK/$\overline{\text{SECLK}}$ = OV_{DD}, PD = GND, SHREF = GND, DIV2 = GND, DIV4 = GND, G/$\overline{\text{T}}$ = GND, f_{CLK} = 65MHz, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			12			Bits
Integral Nonlinearity	INL	f_{IN} = 3MHz		±0.3	±1.1	LSB
Differential Nonlinearity	DNL	f_{IN} = 3MHz, no missing codes		±0.3	±0.65	LSB
Offset Error				±0.1	±0.7	%FSR
Gain Error				±0.5	±5.7	%FSR
		(Note 2)		±0.5	±3.4	
ANALOG INPUT (INAP, INAN, INBP, INBN)						
Differential Input Voltage Range	V_{DIFF}	Differential or single-ended inputs		±1.024		V
Common-Mode Input Voltage				V_{DD} / 2		V
Analog Input Resistance	R_{IN}	Each input (Figure 3)		3.4		kΩ
Analog Input Capacitance	C_{PAR}	Fixed capacitance to ground, each input (Figure 3)		2		pF
	C_{SAMPLE}	Switched capacitance, each input (Figure 3)		4.5		
CONVERSION RATE						
Maximum Clock Frequency	f_{CLK}		65			MHz
Minimum Clock Frequency					5	MHz
Data Latency		Figure 5		8		Clock Cycles
DYNAMIC CHARACTERISTICS (differential inputs)						
Small-Signal Noise Floor	SSNF	Input at -35dBFS (Note 2)	67.0	71.1		dBFS
Signal-to-Noise Ratio	SNR	f_{IN} = 3MHz at -0.5dBFS	68.2	70.8		dB
		f_{IN} = 32.5MHz at -0.5dBFS		70.6		
		f_{IN} = 70MHz at -0.5dBFS		70.4		
		f_{IN} = 175MHz at -0.5dBFS	67.2	69.8		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference), $C_L \approx$ 10pF at digital outputs, V_{IN} = -0.5dBFS (differential), DIFFCLK/$\overline{SECLK}$ = OV_{DD}, PD = GND, SHREF = GND, DIV2 = GND, DIV4 = GND, G/$\overline{T}$ = GND, f_{CLK} = 65MHz, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Signal-to-Noise Plus Distortion	SINAD	f_{IN} = 3MHz at -0.5dBFS	68.1	70.7		dB
		f_{IN} = 32.5MHz at -0.5dBFS		70.4		
		f_{IN} = 70MHz at -0.5dBFS		70.2		
		f_{IN} = 175MHz at -0.5dBFS	65.9	69.3		
Spurious-Free Dynamic Range	SFDR	f_{IN} = 3MHz at -0.5dBFS (Note 2)	81.9	91		dBc
		f_{IN} = 32.5MHz at -0.5dBFS		86.3		
		f_{IN} = 70MHz at -0.5dBFS		84.4		
		f_{IN} = 175MHz at -0.5dBFS	71.1	80.2		
Total Harmonic Distortion	THD	f_{IN} = 3MHz at -0.5dBFS (Note 2)		-92.6	-82.9	dBc
		f_{IN} = 32.5MHz at -0.5dBFS		-84.3		
		f_{IN} = 70MHz at -0.5dBFS		-83.7		
		f_{IN} = 175MHz at -0.5dBFS		-78.9	-69.8	
Second Harmonic	HD2	f_{IN} = 3MHz at -0.5dBFS		-98		dBc
		f_{IN} = 32.5MHz at -0.5dBFS		-91.7		
		f_{IN} = 70MHz at -0.5dBFS		-94.5		
		f_{IN} = 175MHz at -0.5dBFS		-80.2		
Third Harmonic	HD3	f_{IN} = 3MHz at -0.5dBFS		-97		dBc
		f_{IN} = 32.5MHz at -0.5dBFS		-86.3		
		f_{IN} = 70MHz at -0.5dBFS		-84.4		
		f_{IN} = 175MHz at -0.5dBFS		-85.6		
Two-Tone Intermodulation Distortion (Note 3)	TTIMD	f_{IN1} = 68.5MHz at -7dBFS f_{IN2} = 71.5MHz at -7dBFS		-89		dBc
		f_{IN1} = 172.5MHz at -7dBFS f_{IN2} = 177.5MHz at -7dBFS		-82.2		
3rd-Order Intermodulation Distortion	IM3	f_{IN1} = 68.5MHz at -7dBFS f_{IN2} = 71.5MHz at -7dBFS		-92.2		dBc
		f_{IN1} = 172.5MHz at -7dBFS f_{IN2} = 177.5MHz at -7dBFS		-88.9		
Two-Tone Spurious-Free Dynamic Range	$SFDR_{TT}$	f_{IN1} = 68.5MHz at -7dBFS f_{IN2} = 71.5MHz at -7dBFS		90.6		dBc
		f_{IN1} = 172.5MHz at -7dBFS f_{IN2} = 177.5MHz at -7dBFS		82.9		
Full-Power Bandwidth	FPBW	Input at -0.2dBFS, -3dB rolloff		750		MHz
Aperture Delay	t_{AD}	Figure 5		1.2		ns
Aperture Jitter	t_{AJ}			<0.15		ps_{RMS}
Output Noise	n_{OUT}	INAP = INAN = COMA INBP = INBN = COMB		0.3		LSB_{RMS}

Dual, 65Msps, 12-Bit, IF/Baseband ADC

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference), $C_L \approx$ 10pF at digital outputs, V_{IN} = -0.5dBFS (differential), DIFFCLK/$\overline{SECLK}$ = OV_{DD}, PD = GND, SHREF = GND, DIV2 = GND, DIV4 = GND, G/$\overline{T}$ = GND, f_{CLK} = 65MHz, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Overdrive Recovery Time		±10% beyond full-scale		1		Clock cycle
INTERCHANNEL CHARACTERISTICS						
Crosstalk Rejection		f_{INA} or f_{INB} = 70MHz at -0.5dBFS		90		dB
		f_{INA} or f_{INB} = 175MHz at -0.5dBFS		85		
Gain Matching				±0.01	±0.1	dB
Offset Matching				±0.01		%FSR
INTERNAL REFERENCE (REFOUT)						
REFOUT Output Voltage	V_{REFOUT}		2.000	2.048	2.080	V
REFOUT Load Regulation		-1mA < I_{REFOUT} < +1mA		35		mV/mA
REFOUT Temperature Coefficient	TC_{REF}			±50		ppm/°C
REFOUT Short-Circuit Current		Short to V_{DD}—sinking		0.24		mA
		Short to GND—sourcing		2.1		
BUFFERED REFERENCE MODE (REFIN is driven by REFOUT or an external 2.048V single-ended reference source; V_{REFAP}/V_{REFAN}/V_{COMA} and V_{REFBP}/V_{REFBN}/V_{COMB} are generated internally)						
REFIN Input Voltage	V_{REFIN}			2.048		V
REFIN Input Resistance	R_{REFIN}			>50		MΩ
COM_ Output Voltage	V_{COMA} V_{COMB}	V_{DD} / 2	1.60	1.65	1.70	V
REF_P Output Voltage	V_{REFAP} V_{REFBP}	V_{DD} / 2 + (V_{REFIN} x 3/8)		2.418		V
REF_N Output Voltage	V_{REFAN} V_{REFBN}	V_{DD} / 2 - (V_{REFIN} x 3/8)		0.882		V
Differential Reference Voltage	V_{REFA} V_{REFB}	V_{REFA} = V_{REFAP} - V_{REFAN} V_{REFB} = V_{REFBP} - V_{REFBN}	1.440	1.536	1.590	V
Differential Reference Temperature Coefficient	TC_{REF}			±25		ppm/°C
UNBUFFERED EXTERNAL REFERENCE (REFIN = GND, V_{REFAP}/V_{REFAN}/V_{COMA} and V_{REFBP}/V_{REFBN}/V_{COMB} are applied externally, V_{COMA} = V_{COMB} = V_{DD} / 2)						
REF_P Input Voltage	V_{REFAP} V_{REFBP}	V_{REF_P} - V_{COM}		+0.768		V
REF_N Input Voltage	V_{REFAN} V_{REFBN}	V_{REF_N} - V_{COM}		-0.768		V
COM_ Input Voltage	V_{COM}	V_{DD} / 2		1.65		V
Differential Reference Voltage	V_{REFA} V_{REFB}	$V_{REF\_}$ = V_{REF_P} - V_{REF_N} = V_{REFIN} x 3/4		1.536		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference), $C_L \approx$ 10pF at digital outputs, V_{IN} = -0.5dBFS (differential), DIFFCLK/$\overline{SECLK}$ = OV_{DD}, PD = GND, SHREF = GND, DIV2 = GND, DIV4 = GND, G/$\overline{T}$ = GND, f_{CLK} = 65MHz, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REF_P Sink Current	I_{REFAP} I_{REFBP}	V_{REF_P} = 2.418V		1.2		mA
REF_N Source Current	I_{REFAN} I_{REFBN}	V_{REF_N} = 0.882V		0.85		mA
COM_ Sink Current	I_{COMA} I_{COMB}	$V_{COM\_}$ = 1.65V		0.85		mA
REF_P, REF_N Capacitance	C_{REF_P}, C_{REF_N}			13		pF
COM_ Capacitance	$C_{COM\_}$			6		pF
CLOCK INPUTS (CLKP, CLKN)						
Single-Ended Input High Threshold	V_{IH}	DIFFCLK/$\overline{SECLK}$ = GND, CLKN = GND	0.8 x V_{DD}			V
Single-Ended Input Low Threshold	V_{IL}	DIFFCLK/$\overline{SECLK}$ = GND, CLKN = GND			0.2 x V_{DD}	V
Minimum Differential Clock Input Voltage Swing		DIFFCLK/$\overline{SECLK}$ = OV_{DD}		0.2		V_{P-P}
Differential Input Common-Mode Voltage		DIFFCLK/$\overline{SECLK}$ = OV_{DD}		V_{DD} / 2		V
CLK_ Input Resistance	R_{CLK}	Each input (Figure 4)		5		kΩ
CLK_ Input Capacitance	C_{CLK}	Each input		2		pF
DIGITAL INPUTS (DIFFCLK/$\overline{SECLK}$, G/$\overline{T}$, PD, DIV2, DIV4)						
Input High Threshold	V_{IH}		0.8 x OV_{DD}			V
Input Low Threshold	V_{IL}				0.2 x OV_{DD}	V
Input Leakage Current		OV_{DD} applied to input			±5	µA
		Input connected to ground			±5	
Digital Input Capacitance	C_{DIN}			5		pF
DIGITAL OUTPUTS (D0A–D11A, D0B–D11B, DORA, DORB, DAV)						
Output-Voltage Low	V_{OL}	D0A–D11A, D0B–D11B, DORA, DORB: I_{SINK} = 200µA			0.2	V
		DAV: I_{SINK} = 600µA			0.2	
Output-Voltage High	V_{OH}	D0A–D11A, D0B–D11B, DORA, DORB: I_{SOURCE} = 200µA	OV_{DD} - 0.2			V
		DAV: I_{SOURCE} = 600µA	OV_{DD} - 0.2			
Tri-State Leakage Current (Note 4)	I_{LEAK}	OV_{DD} applied to input			±5	µA
		Input connected to ground			±5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference), $C_L \approx$ 10pF at digital outputs, V_{IN} = -0.5dBFS (differential), DIFFCLK/$\overline{SECLK}$ = OV_{DD}, PD = GND, SHREF = GND, DIV2 = GND, DIV4 = GND, G/$\overline{T}$ = GND, f_{CLK} = 65MHz, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
D0A–D11A, DORA, D0B–D11B and DORB Tri-State Output Capacitance (Note 4)	C_{OUT}			3		pF
DAV Tri-State Output Capacitance (Note 4)	C_{DAV}			6		pF
POWER REQUIREMENTS						
Analog Supply Voltage	V_{DD}		3.15	3.30	3.60	V
Digital Output Supply Voltage	OV_{DD}		1.70	2.0	V_{DD}	V
Analog Supply Current	I_{VDD}	Normal operating mode f_{IN} = 175MHz at -0.5dBFS, single-ended clock (DIFFCLK/$\overline{SECLK}$ = GND)		188		mA
		Normal operating mode f_{IN} = 175MHz at -0.5dBFS differential clock (DIFFCLK/$\overline{SECLK}$ = OV_{DD})		196	215	
		Power-down mode (PD = OV_{DD}) clock idle		0.05		
Analog Power Dissipation	P_{VDD}	Normal operating mode f_{IN} = 175MHz at -0.5dBFS single-ended clock (DIFFCLK/$\overline{SECLK}$ = GND)		620		mW
		Normal operating mode f_{IN} = 175MHz at -0.5dBFS differential clock (DIFFCLK/$\overline{SECLK}$ = OV_{DD})		647	710	
		Power-down mode (PD = OV_{DD}) clock idle		0.165		
Digital Output Supply Current	I_{OVDD}	Normal operating mode f_{IN} = 175MHz at -0.5dBFS		19.7		mA
		Power-down mode (PD = OV_{DD}) clock idle		0.001		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference), $C_L \approx$ 10pF at digital outputs, V_{IN} = -0.5dBFS (differential), DIFFCLK/$\overline{\text{SECLK}}$ = OV_{DD}, PD = GND, SHREF = GND, DIV2 = GND, DIV4 = GND, G/$\overline{\text{T}}$ = GND, f_{CLK} = 65MHz, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

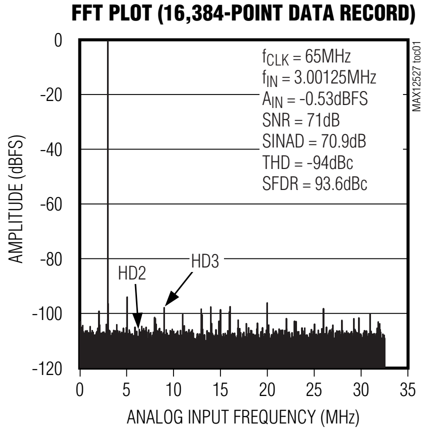
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Figure 5)						
Clock Pulse-Width High	t_{CH}			7.7		ns
Clock Pulse-Width Low	t_{CL}			7.7		ns
Data-Valid Delay	t_{DAV}			5.4		ns
Data Setup Time Before Rising Edge of DAV	t_{SETUP}	(Note 5)	7.0			ns
Data Hold Time After Rising Edge of DAV	t_{HOLD}	(Note 5)	7.0			ns
Wake-Up Time from Power-Down	t_{WAKE}	V_{REFIN} = 2.048V		10		ms

Note 1: Specifications ≥+25°C guaranteed by production test, <+25°C guaranteed by design and characterization.
Note 2: Specifications guaranteed by production test for ≥+25°C.
Note 3: Two-tone intermodulation distortion measured with respect to a single-carrier amplitude, and not the peak-to-average input power of both input tones.
Note 4: During power-down, D0A–D11A, D0B–D11B, DORA, DORB, and DAV are high impedance.
Note 5: Guaranteed by design and characterization.

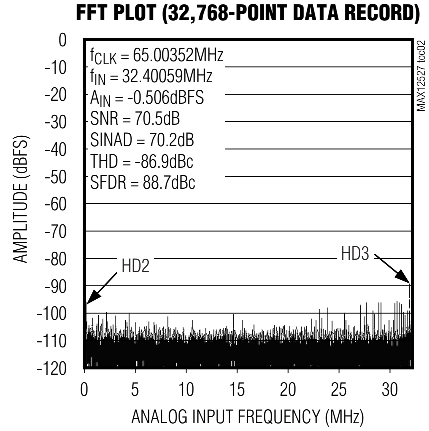
Typical Operating Characteristics

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference mode), $C_L \approx$ 5pF at digital outputs, V_{IN} = -0.5dBFS, DIFFCLK/$\overline{\text{SECLK}}$ = OV_{DD}, PD = GND, G/$\overline{\text{T}}$ = GND, f_{CLK} = 65MHz (50% duty cycle), T_A = +25°C, unless otherwise noted.)

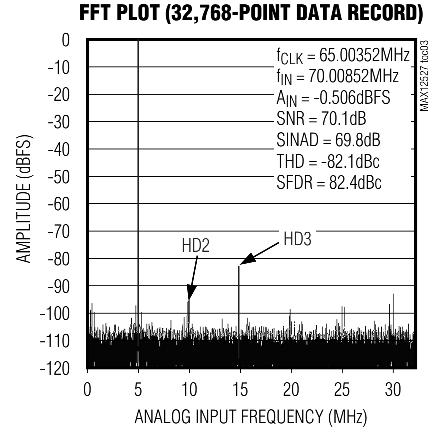
FFT PLOT (16,384-POINT DATA RECORD)



FFT PLOT (32,768-POINT DATA RECORD)



FFT PLOT (32,768-POINT DATA RECORD)

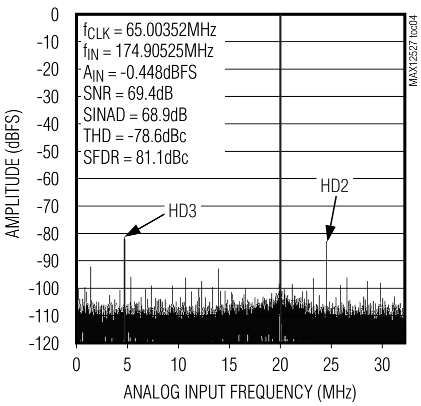


Dual, 65Msps, 12-Bit, IF/Baseband ADC

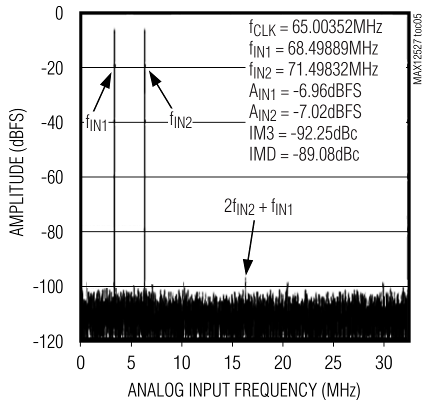
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference mode), $C_L \approx$ 5pF at digital outputs, V_{IN} = -0.5dBFS, DIFFCLK/$\overline{SECLK}$ = OV_{DD}, PD = GND, G/$\overline{T}$ = GND, f_{CLK} = 65MHz (50% duty cycle), T_A = +25°C, unless otherwise noted.)

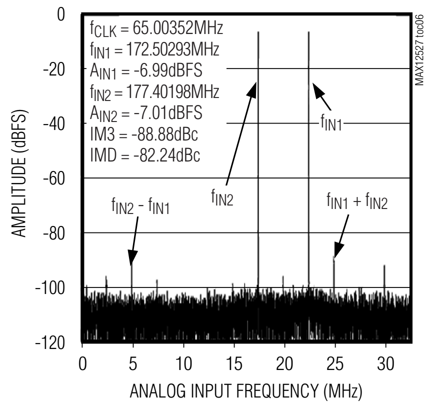
FFT PLOT (32,768-POINT DATA RECORD)



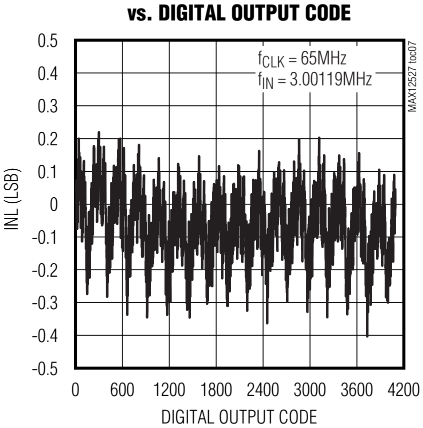
TWO-TONE IMD PLOT (16,384-POINT DATA RECORD)



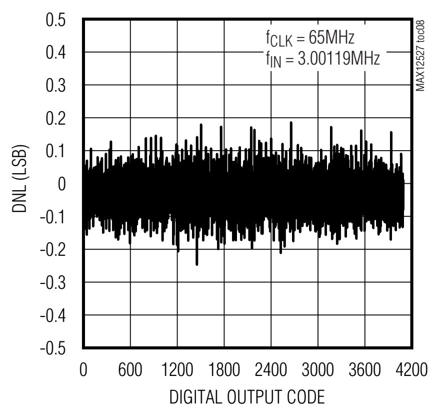
TWO-TONE IMD PLOT (16,384-POINT DATA RECORD)



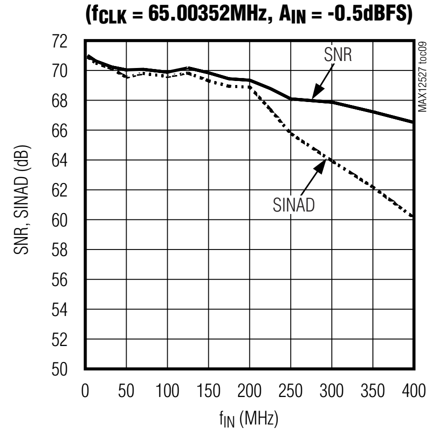
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



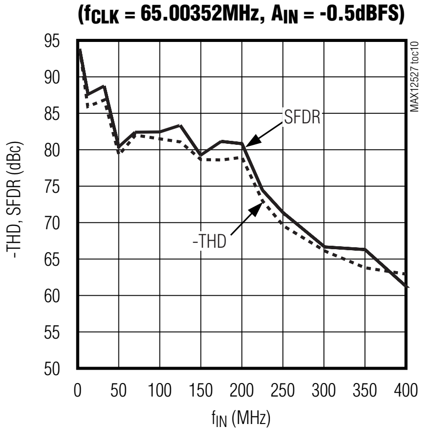
DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



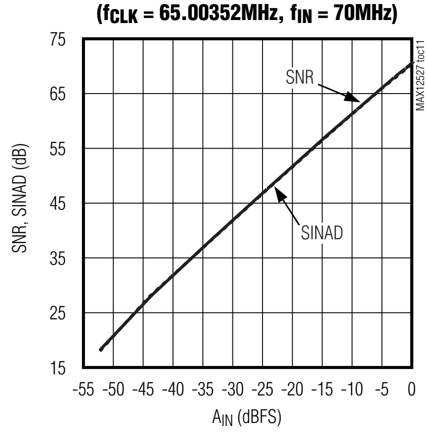
SNR, SINAD vs. ANALOG INPUT FREQUENCY (f_{CLK} = 65.00352MHz, A_{IN} = -0.5dBFS)



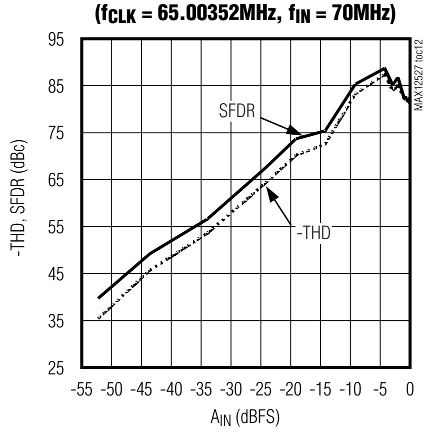
-THD, SFDR vs. ANALOG INPUT FREQUENCY (f_{CLK} = 65.00352MHz, A_{IN} = -0.5dBFS)



SNR, SINAD vs. ANALOG INPUT AMPLITUDE (f_{CLK} = 65.00352MHz, f_{IN} = 70MHz)



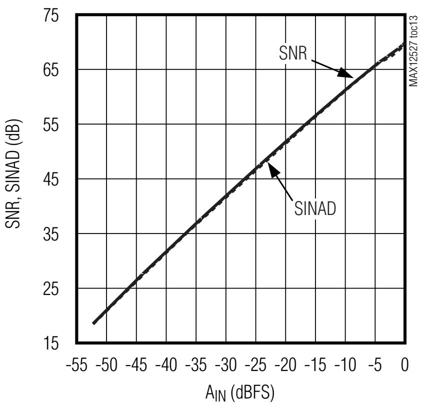
-THD, SFDR vs. ANALOG INPUT AMPLITUDE (f_{CLK} = 65.00352MHz, f_{IN} = 70MHz)



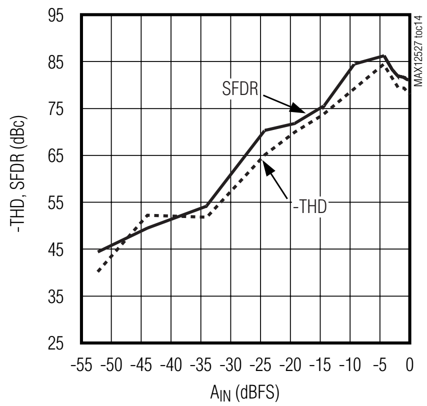
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference mode), $C_L \approx$ 5pF at digital outputs, V_{IN} = -0.5dBFS, DIFFCLK/$\overline{SECLK}$ = OV_{DD}, PD = GND, G/$\overline{T}$ = GND, f_{CLK} = 65MHz (50% duty cycle), T_A = +25°C, unless otherwise noted.)

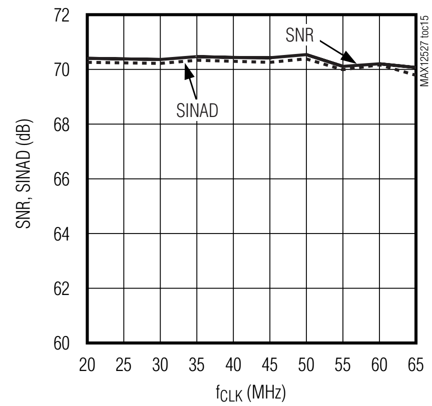
SNR, SINAD vs. ANALOG INPUT AMPLITUDE (f_{CLK} = 65.00352MHz, f_{IN} = 175MHz)



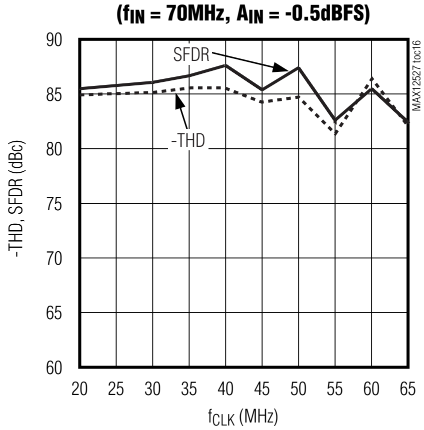
-THD, SFDR vs. ANALOG INPUT AMPLITUDE (f_{CLK} = 65.00352MHz, f_{IN} = 175MHz)



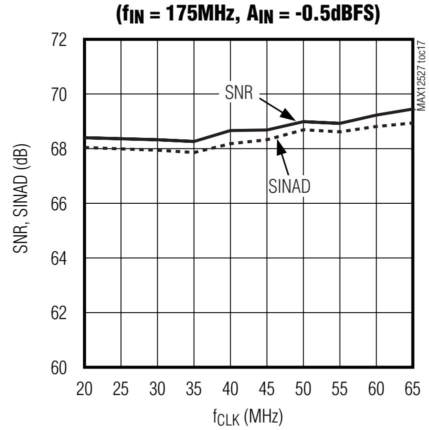
SNR, SINAD vs. CLOCK SPEED (f_{IN} = 70MHz, A_{IN} = -0.5dBFS)



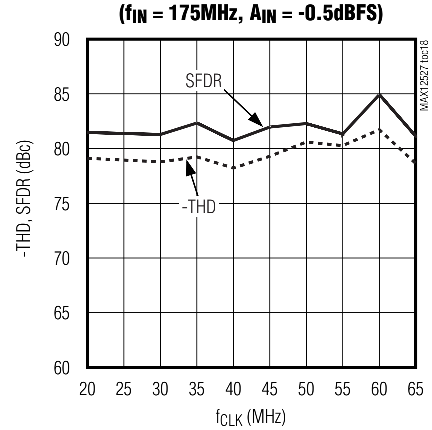
-THD, SFDR vs. CLOCK SPEED (f_{IN} = 70MHz, A_{IN} = -0.5dBFS)



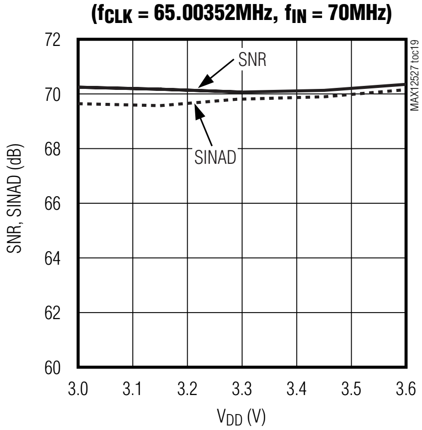
SNR, SINAD vs. CLOCK SPEED (f_{IN} = 175MHz, A_{IN} = -0.5dBFS)



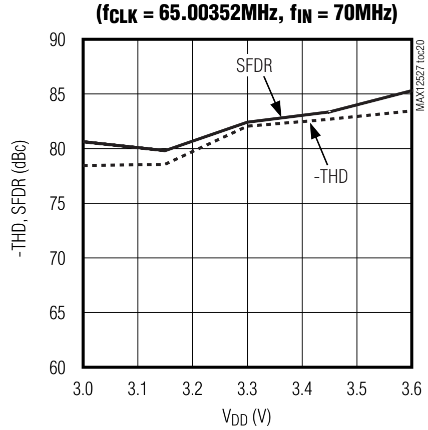
-THD, SFDR vs. CLOCK SPEED (f_{IN} = 175MHz, A_{IN} = -0.5dBFS)



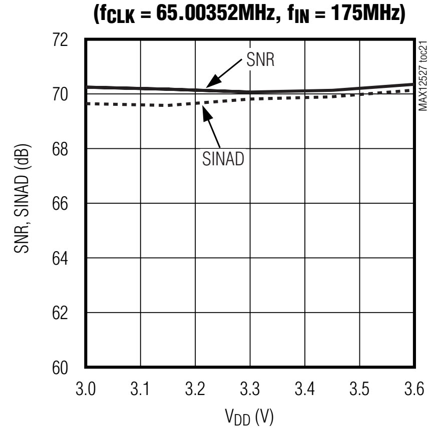
SNR, SINAD vs. ANALOG SUPPLY VOLTAGE (f_{CLK} = 65.00352MHz, f_{IN} = 70MHz)



-THD, SFDR vs. ANALOG SUPPLY VOLTAGE (f_{CLK} = 65.00352MHz, f_{IN} = 70MHz)



SNR, SINAD vs. ANALOG SUPPLY VOLTAGE (f_{CLK} = 65.00352MHz, f_{IN} = 175MHz)

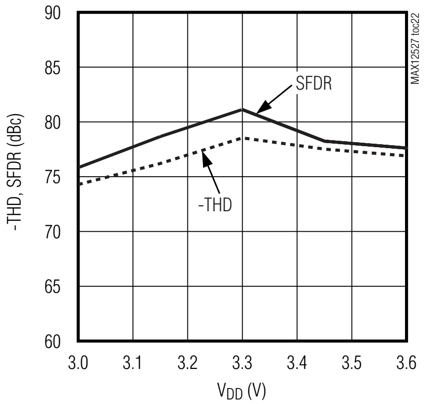


Dual, 65Msps, 12-Bit, IF/Baseband ADC

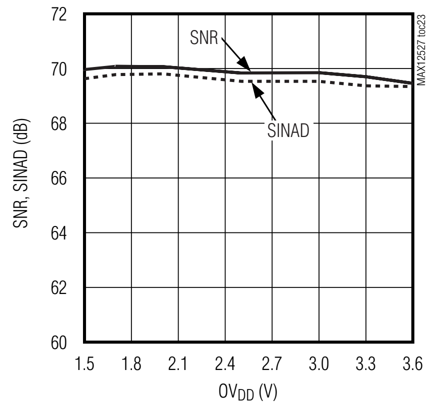
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference mode), $C_L \approx$ 5pF at digital outputs, V_{IN} = -0.5dBFS, DIFFCLK/$\overline{SECLK}$ = OV_{DD}, PD = GND, G/$\overline{T}$ = GND, f_{CLK} = 65MHz (50% duty cycle), T_A = +25°C, unless otherwise noted.)

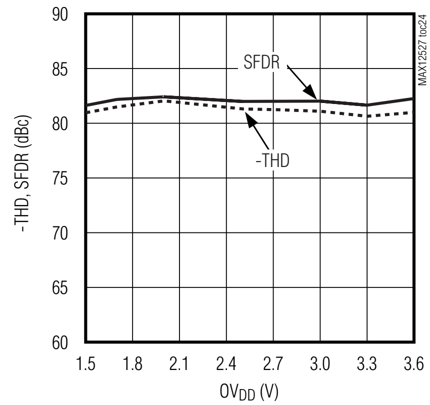
-THD, SFDR vs. ANALOG SUPPLY VOLTAGE (f_{CLK} = 65.00352MHz, f_{IN} = 175MHz)



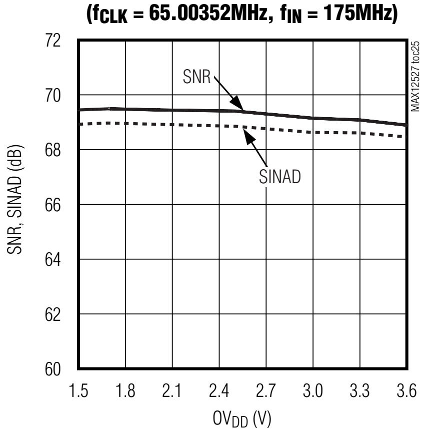
SNR, SINAD vs. DIGITAL SUPPLY VOLTAGE (f_{CLK} = 65.00352MHz, f_{IN} = 70MHz)



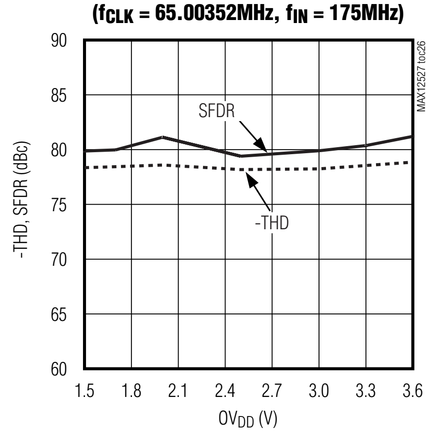
-THD, SFDR vs. DIGITAL SUPPLY VOLTAGE (f_{CLK} = 65.00352MHz, f_{IN} = 70MHz)



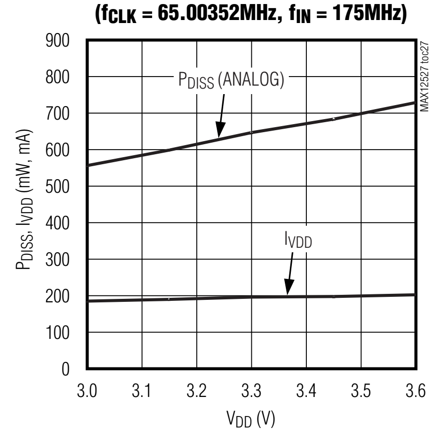
SNR, SINAD vs. DIGITAL SUPPLY VOLTAGE (f_{CLK} = 65.00352MHz, f_{IN} = 175MHz)



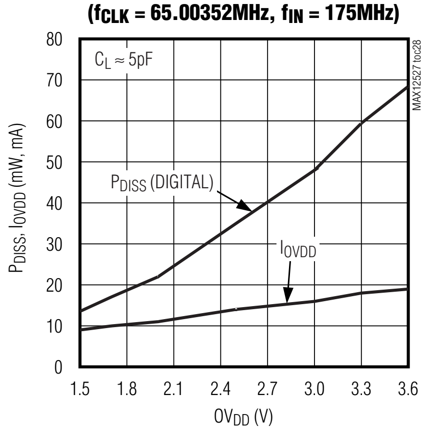
-THD, SFDR vs. DIGITAL SUPPLY VOLTAGE (f_{CLK} = 65.00352MHz, f_{IN} = 175MHz)



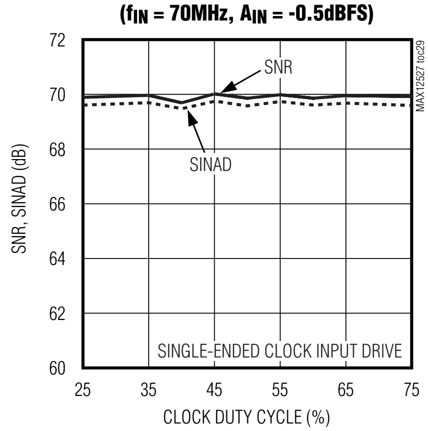
P_{DISS}, I_{VDD} (ANALOG) vs. ANALOG SUPPLY VOLTAGE (f_{CLK} = 65.00352MHz, f_{IN} = 175MHz)



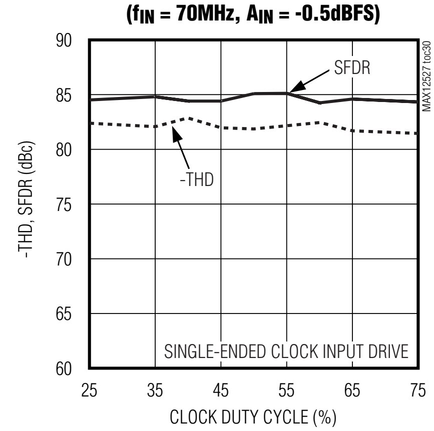
P_{DISS}, I_{OVDD} (DIGITAL) vs. DIGITAL SUPPLY VOLTAGE (f_{CLK} = 65.00352MHz, f_{IN} = 175MHz)



SNR, SINAD vs. CLOCK DUTY CYCLE (f_{IN} = 70MHz, A_{IN} = -0.5dBFS)

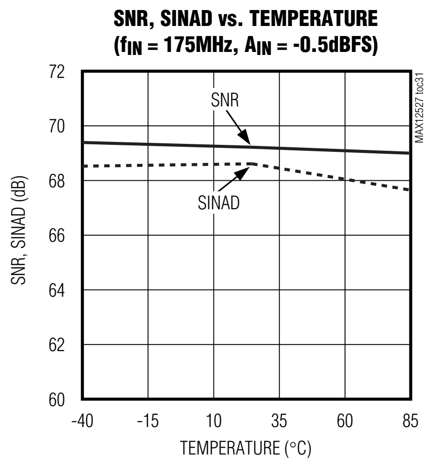


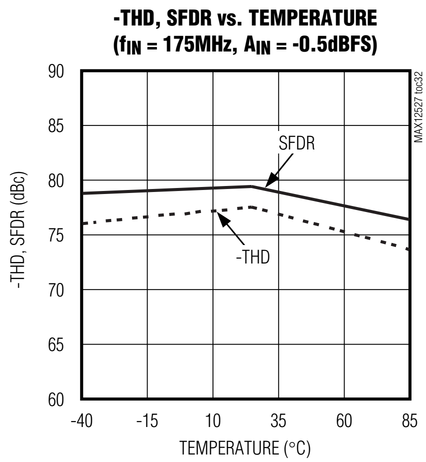
-THD, SFDR vs. CLOCK DUTY CYCLE (f_{IN} = 70MHz, A_{IN} = -0.5dBFS)

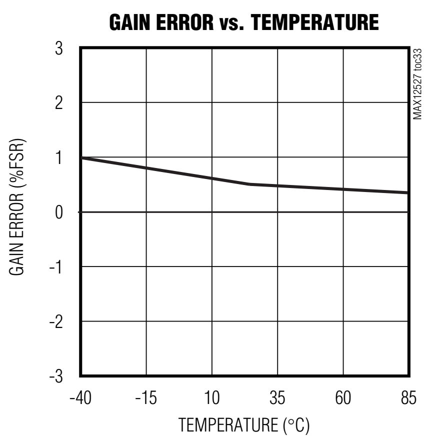


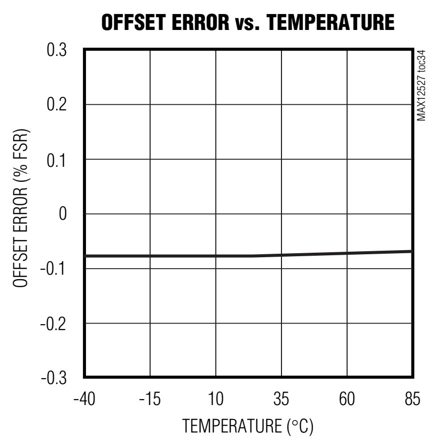
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference mode), $C_L \approx$ 5pF at digital outputs, V_{IN} = -0.5dBFS, DIFFCLK/$\overline{SECLK}$ = OV_{DD}, PD = GND, G/$\overline{T}$ = GND, f_{CLK} = 65MHz (50% duty cycle), T_A = +25°C, unless otherwise noted.)









Pin Description

PIN	NAME	FUNCTION
1, 4, 5, 9, 13, 14, 17	GND	Converter Ground. Connect all ground pins and the exposed paddle (EP) together.
2	INAP	Channel A Positive Analog Input
3	INAN	Channel A Negative Analog Input
6	COMA	Channel A Common-Mode Voltage I/O. Bypass COMA to GND with a 0.1µF capacitor.
7	REFAP	Channel A Positive Reference I/O. Channel A conversion range is ±2/3 x (V_{REFAP} - V_{REFAN}). Bypass REFAP with a 0.1µF capacitor to GND. Connect a 10µF and a 1µF bypass capacitor between REFAP and REFAN. **Place the 1µF REFAP-to-REFAN capacitor as close to the device as possible on the same side of the PC board.**
8	REFAN	Channel A Negative Reference I/O. Channel A conversion range is ±2/3 x (V_{REFAP} - V_{REFAN}). Bypass REFAN with a 0.1µF capacitor to GND. Connect a 10µF and a 1µF bypass capacitor between REFAP and REFAN. **Place the 1µF REFAP-to-REFAN capacitor as close to the device as possible on the same side of the PC board.**
10	REFBN	Channel B Negative Reference I/O. Channel B conversion range is ±2/3 x (V_{REFBP} - V_{REFBN}). Bypass REFBN with a 0.1µF capacitor to GND. Connect a 10µF and a 1µF bypass capacitor between REFBP and REFBN. **Place the 1µF REFBP-to-REFBN capacitor as close to the device as possible on the same side of the PC board.**
11	REFBP	Channel B Positive Reference I/O. Channel B conversion range is ±2/3 x (V_{REFBP} - V_{REFBN}). Bypass REFBP with a 0.1µF capacitor to GND. Connect a 10µF and a 1µF bypass capacitor between REFBP and REFBN. **Place the 1µF REFBP-to-REFBN capacitor as close to the device as possible on the same side of the PC board.**
12	COMB	Channel A Common-Mode Voltage I/O. Bypass COMB to GND with a 0.1µF capacitor.
15	INBN	Channel B Negative Analog Input
16	INBP	Channel B Positive Analog Input
18	DIFFCLK/$\overline{\text{SECLK}}$	Differential/Single-Ended Input Clock Drive. This input selects between single-ended or differential clock input drives. DIFFCLK/$\overline{\text{SECLK}}$ = GND: Selects single-ended clock input drive. DIFFCLK/$\overline{\text{SECLK}}$ = OV_{DD}: Selects differential clock input drive.
19	CLKN	Negative Clock Input. In differential clock input mode (DIFFCLK/$\overline{\text{SECLK}}$ = OV_{DD}), connect a differential clock signal between CLKP and CLKN. In single-ended clock mode (DIFFCLK/$\overline{\text{SECLK}}$ = GND), apply the clock signal to CLKP and connect CLKN to GND.
20	CLKP	Positive Clock Input. In differential clock input mode (DIFFCLK/$\overline{\text{SECLK}}$ = OV_{DD}), connect a differential clock signal between CLKP and CLKN. In single-ended clock mode (DIFFCLK/$\overline{\text{SECLK}}$ = GND), apply the single-ended clock signal to CLKP and connect CLKN to GND.
21	DIV2	Divide-by-Two Clock-Divider Digital Control Input. See Table 2 for details.
22	DIV4	Divide-by-Four Clock-Divider Digital Control Input. See Table 2 for details.
23–26, 61, 62, 63	V_{DD}	Analog Power Input. Connect V_{DD} to a 3.15V to 3.60V power supply. Bypass V_{DD} to GND with a parallel capacitor combination of ≥10µF and 0.1µF. Connect all V_{DD} pins to the same potential.
27, 43, 60	OV_{DD}	Output-Driver Power Input. Connect OV_{DD} to a 1.7V to V_{DD} power supply. Bypass OV_{DD} to GND with a parallel capacitor combination of ≥10µF and 0.1µF.
28, 29, 45, 46	N.C.	No Connection

Pin Description (continued)

PIN	NAME	FUNCTION
30	D0B	Channel B CMOS Digital Output, Bit 0 (LSB)
31	D1B	Channel B CMOS Digital Output, Bit 1
32	D2B	Channel B CMOS Digital Output, Bit 2
33	D3B	Channel B CMOS Digital Output, Bit 3
34	D4B	Channel B CMOS Digital Output, Bit 4
35	D5B	Channel B CMOS Digital Output, Bit 5
36	D6B	Channel B CMOS Digital Output, Bit 6
37	D7B	Channel B CMOS Digital Output, Bit 7
38	D8B	Channel B CMOS Digital Output, Bit 8
39	D9B	Channel B CMOS Digital Output, Bit 9
40	D10B	Channel B CMOS Digital Output, Bit 10
41	D11B	Channel B CMOS Digital Output, Bit 11 (MSB)
42	DORB	Channel B Data Out-of-Range Indicator. The DORB digital output indicates when the channel B analog input voltage is out of range. DORB = 1: Digital outputs exceed full-scale range. DORB = 0: Digital outputs are within full-scale range.
44	DAV	Data-Valid Digital Output. The rising edge of DAV indicates that data is present on the digital outputs. The MAX12527 evaluation kit (MAX12557 EV kit) utilizes DAV to latch data into any external back-end digital logic.
47	D0A	Channel A CMOS Digital Output, Bit 0 (LSB)
48	D1A	Channel A CMOS Digital Output, Bit 1
49	D2A	Channel A CMOS Digital Output, Bit 2
50	D3A	Channel A CMOS Digital Output, Bit 3
51	D4A	Channel A CMOS Digital Output, Bit 4
52	D5A	Channel A CMOS Digital Output, Bit 5
53	D6A	Channel A CMOS Digital Output, Bit 6
54	D7A	Channel A CMOS Digital Output, Bit 7
55	D8A	Channel A CMOS Digital Output, Bit 8
56	D9A	Channel A CMOS Digital Output, Bit 9
57	D10A	Channel A CMOS Digital Output, Bit 10
58	D11A	Channel A CMOS Digital Output, Bit 11 (MSB)
59	DORA	Channel A Data Out-of-Range Indicator. The DORA digital output indicates when the channel A analog input voltage is out of range. DORA = 1: Digital outputs exceed full-scale range. DORA = 0: Digital outputs are within full-scale range.
64	$G/\overline{T}$	Output Format Select Digital Input. $G/\overline{T}$ = GND: Two's-complement output format selected. $G/\overline{T}$ = OV_{DD}: Gray-code output format selected.
65	PD	Power-Down Digital Input. PD = GND: ADCs are fully operational. PD = OV_{DD}: ADCs are powered down.

Dual, 65Msps, 12-Bit, IF/Baseband ADC

Pin Description (continued)

PIN	NAME	FUNCTION
66	SHREF	Shared Reference Digital Input. SHREF = V_{DD}: Shared reference enabled. SHREF = GND: Shared reference disabled. When sharing the reference, externally connect REFAP and REFBP together to ensure that V_{REFAP} equals V_{REFBP}. Similarly, when sharing the reference, externally connect REFAN to REFBN together to ensure that $V_{REFAN} = V_{REFBN}$.
67	REFOUT	Internal Reference Voltage Output. The REFOUT output voltage is 2.048V and REFOUT can deliver 1mA. For internal reference operation, connect REFOUT directly to REFIN or use a resistive divider from REFOUT to set the voltage at REFIN. **Bypass REFOUT to GND with a ≥0.1µF capacitor.** For external reference operation, REFOUT is not required and must be bypassed to GND with a ≥0.1µF capacitor.
68	REFIN	Single-Ended Reference Analog Input. For internal reference and buffered external reference operation, apply a 0.7V to 2.3V DC reference voltage to REFIN. **Bypass REFIN to GND with a 4.7µF capacitor.** Within its specified operating voltage, REFIN has a >50MΩ input impedance, and the differential reference voltage (V_{REF_P} - V_{REF_N}) is generated from REFIN. For unbuffered external reference operation, connect REFIN to GND. In this mode REF_P, REF_N, and COM_ are high-impedance inputs that accept the external reference voltages.
—	EP	Exposed Paddle. EP is internally connected to GND. Externally connect EP to GND to achieve specified dynamic performance.

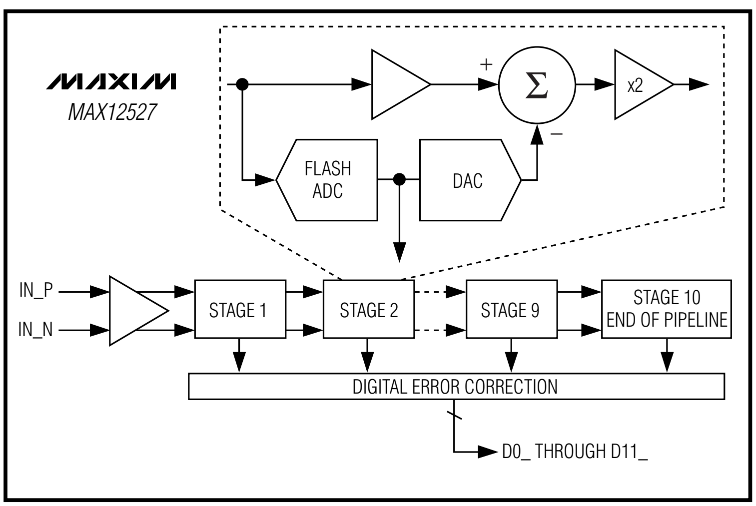


Figure 1. Pipeline Architecture—Stage Blocks

Detailed Description

The MAX12527 uses a 10-stage, fully differential, pipelined architecture (Figure 1) that allows for high-speed conversion while minimizing power consumption. Samples taken at the inputs move progressively through the pipeline stages every half clock cycle. From input to output the total latency is 8 clock cycles.

Each pipeline converter stage converts its input voltage to a digital output code. At every stage, except the last, the error between the input voltage and the digital output code is multiplied and passed along to the next pipeline stage. Digital error correction compensates for ADC comparator offsets in each pipeline stage and ensures no missing codes. Figure 2 shows the MAX12527 functional diagram.

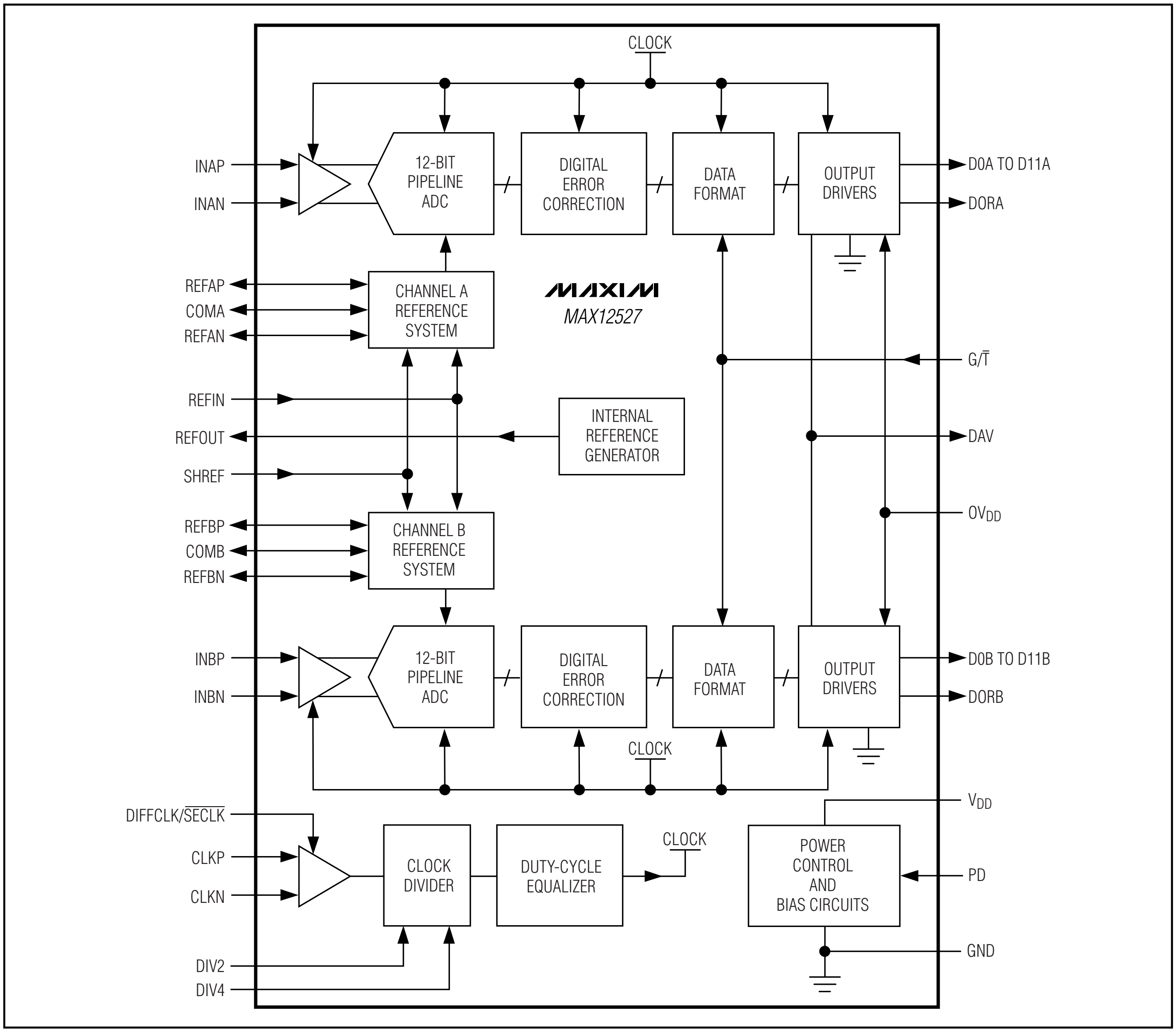


Figure 2. Functional Diagram

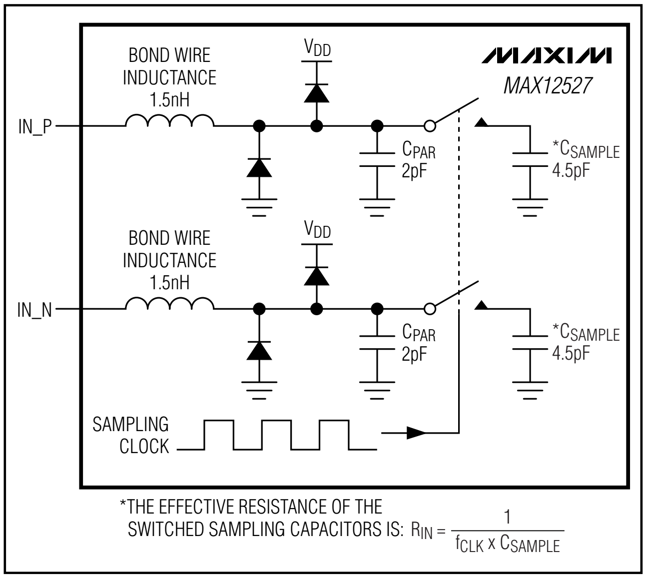


Figure 3. Internal T/H Circuit

Analog Inputs and Input Track-and-Hold (T/H) Amplifier

Figure 3 displays a simplified functional diagram of the input T/H circuit. This input T/H circuit allows for high analog input frequencies of 175MHz and beyond and supports a V_{DD} / 2 common-mode input voltage.

The MAX12527 sampling clock controls the switched-capacitor input T/H architecture (Figure 3) allowing the analog input signals to be stored as charge on the sampling capacitors. These switches are closed (track mode) when the sampling clock is high and open (hold mode) when the sampling clock is low (Figure 4). The analog input signal source must be able to provide the dynamic currents necessary to charge and discharge the sampling capacitors. To avoid signal degradation, these capacitors must be charged to one-half LSB accuracy within one-half of a clock cycle. The analog input of the MAX12527 supports differential or single-ended input drive. For optimum performance with differential inputs, balance the input impedance of IN_P and IN_N and set the common-mode voltage to mid-supply (V_{DD} / 2). The MAX12527 provides the optimum common-mode voltage of V_{DD} / 2 through the COM output when operating in internal reference mode and buffered external reference mode. This COM output voltage can be used to bias the input network as shown in Figures 9, 10, and 11.

Reference Output

An internal bandgap reference is the basis for all the internal voltages and bias currents used in the MAX12527. The power-down logic input (PD) enables and disables the reference circuit. REFOUT has approximately 17kΩ to GND when the MAX12527 is powered down. The reference circuit requires 10ms to power up and settle to its final value when power is applied to the MAX12527 or when PD transitions from high to low.

The internal bandgap reference produces a buffered reference voltage of 2.048V ±1% at the REFOUT pin with a ±50ppm/°C temperature coefficient. Connect an external ≥0.1µF bypass capacitor from REFOUT to GND for stability. REFOUT sources up to 1mA and sinks up to 0.1mA for external circuits with a 35mV/mA load regulation. Short-circuit protection limits I_{REFOUT} to a 2.1mA source current when shorted to GND and a 0.24mA sink current when shorted to V_{DD}. Similar to REFOUT, REFIN should be bypassed with a 4.7µF capacitor to GND.

Table 1. Reference Modes

V_{REFIN}	REFERENCE MODE
35% V_{REFOUT} to 100% V_{REFOUT}	Internal Reference Mode. REFIN is driven by REFOUT either through a direct short or a resistive divider. $V_{COM\_} = V_{DD} / 2$ $V_{REF\_P} = V_{DD} / 2 + 3/8 \times V_{REFIN}$ $V_{REF\_N} = V_{DD} / 2 - 3/8 \times V_{REFIN}$
0.7V to 2.3V	Buffered External Reference Mode. An external 0.7V to 2.3V reference voltage is applied to REFIN. $V_{COM\_} = V_{DD} / 2$ $V_{REF\_P} = V_{DD} / 2 + 3/8 \times V_{REFIN}$ $V_{REF\_N} = V_{DD} / 2 - 3/8 \times V_{REFIN}$
<0.5V	Unbuffered External Reference Mode. REF_P, REF_N, and COM_ are driven by external reference sources. The full-scale analog input range is $\pm(V_{REF\_P} - V_{REF\_N}) \times 2/3$.

Reference Configurations

The MAX12527 full-scale analog input range is ±2/3 x V_{REF} with a V_{DD} / 2 ±0.5V common-mode input range. V_{REF} is the voltage difference between REFAP (REFBP) and REFAN (REFBN). The MAX12527 provides three modes of reference operation. The voltage at REFIN (V_{REFIN}) selects the reference operation mode (Table 1).

Connect REFOUT to REFIN either with a direct short or through a resistive divider to enter internal reference mode. COM_, REF_P, and REF_N are low-impedance outputs with $V_{COM\_} = V_{DD} / 2$, $V_{REFP} = V_{DD} / 2 + 3/8 \times V_{REFIN}$, and $V_{REF\_N} = V_{DD} / 2 - 3/8 \times V_{REFIN}$. Bypass REF_P, REF_N, and COM_ each with a 0.1µF capacitor to GND. Bypass REF_P to REF_N with a 10µF capacitor.

Bypass REFIN and REFOUT to GND with a 0.1µF capacitor. The REFIN input impedance is very large (>50MΩ). When driving REFIN through a resistive divider, use resistances ≥10kΩ to avoid loading REFOUT.

Buffered external reference mode is virtually identical to the internal reference mode except that the reference source is derived from an external reference and not the MAX12527's internal bandgap reference. In buffered external reference mode, apply a stable reference voltage source between 0.7V to 2.3V at REFIN. Pins COM_, REF_P, and REF_N are low-impedance outputs with $V_{COM\_} = V_{DD} / 2$, $V_{REF\_P} = V_{DD} / 2 + 3/8 \times V_{REFIN}$, and $V_{REF\_N} = V_{DD} / 2 - 3/8 \times V_{REFIN}$. Bypass REF_P, REF_N, and COM_ each with a 0.1µF capacitor to GND. Bypass REF_P to REF_N with a 10µF capacitor.

Connect REFIN to GND to enter unbuffered external reference mode. Connecting REFIN to GND deactivates the on-chip reference buffers for COM_, REF_P, and REF_N. With their buffers deactivated, COM_, REF_P, and REF_N become high-impedance inputs and must be driven with separate, external reference sources. Drive $V_{COM\_}$ to V_{DD} / 2 ±5%, and drive REF_P and REF_N so $V_{COM\_} = (V_{REF\_P\_} + V_{REF\_N\_}) / 2$. The analog input range is $\pm(V_{REF\_P\_} - V_{REF\_N}) \times 2/3$. Bypass REF_P, REF_N, and COM_ each with a 0.1µF capacitor to GND. Bypass REF_P to REF_N with a 10µF capacitor.

For all reference modes, bypass REFOUT with a 0.1µF and REFIN with a 4.7µF capacitor to GND.

The MAX12527 also features a shared reference mode, in which the user can achieve better channel-to-channel matching. When sharing the reference (SHREF = V_{DD}), externally connect REFAP and REFBP together to ensure that $V_{REFAP} = V_{REFBP}$. Similarly, when sharing the reference, externally connect REFAN to REFBN together to ensure that $V_{REFAN} = V_{REFBN}$.

Connect SHREF to GND to disable the shared reference mode of the MAX12527. In this independent reference mode, a better channel-to-channel isolation is achieved.

For detailed circuit suggestions and how to drive the ADC in buffered/unbuffered external reference mode, see the *Applications Information* section.

Clock Duty-Cycle Equalizer

The MAX12527 has an internal clock duty-cycle equalizer, which makes the converter insensitive to the duty cycle of the signal applied to CLKP and CLKN. The converters allow clock duty-cycle variations from 25% to 75% without negatively impacting the dynamic performance.

The clock duty-cycle equalizer uses a delay-locked loop (DLL) to create internal timing signals that are duty-cycle independent. Due to this DLL, the MAX12527 requires approximately 100 clock cycles to acquire and lock to new clock frequencies.

Clock Input and Clock Control Lines

The MAX12527 accepts both differential and single-ended clock inputs with a wide 25% to 75% input clock duty cycle. For single-ended clock input operation, connect DIFFCLK/$\overline{\text{SECLK}}$ and CLKN to GND. Apply an external single-ended clock signal to CLKP. To reduce clock jitter, the external single-ended clock must have sharp falling edges. For differential clock input operation, connect DIFFCLK/$\overline{\text{SECLK}}$ to OV_{DD}. Apply an external differential clock signal to CLKP and CLKN. Consider the clock input as an analog input and route it away from any other analog inputs and digital signal lines. CLKP and CLKN enter high impedance when the MAX12527 is powered down (Figure 4).

Low clock jitter is required for the specified SNR performance of the MAX12527. The analog inputs are sampled on the falling (rising) edge of CLKP (CLKN), requiring this edge to have the lowest possible jitter. Jitter limits the maximum SNR performance of any ADC according to the following relationship:

$$SNR = 20 \times \log\left(\frac{1}{2 \times \pi \times f_{IN} \times t_J}\right)$$

where f_{IN} represents the analog input frequency and t_J is the total system clock jitter. Clock jitter is especially critical for undersampling applications. For instance, assuming that clock jitter is the only noise source, to obtain the specified 69.8dB of SNR with an input frequency of 175MHz the system must have less than 0.29ps of clock jitter. However, in reality there are other noise sources such as thermal noise and quantization noise that contribute to the system noise requiring the clock jitter to be less than 0.14ps to obtain the specified 69.8dB of SNR at 175MHz.

Clock-Divider Control Inputs (DIV2, DIV4)

The MAX12527 features three different modes of sampling/clock operation (see Table 2). Pulling both control lines low, the clock-divider function is disabled and the converters sample at full clock speed. Pulling DIV4 low and DIV2 high enables the divide-by-two feature, which sets the sampling speed to one-half the selected clock frequency. In divide-by-four mode, the converter sampling speed is set to one-fourth the clock speed of the MAX12527. Divide-by-four mode is achieved by applying a high level to DIV4 and a low level to DIV2. The option to select either one-half or one-fourth of the clock speed for

Dual, 65Msps, 12-Bit, IF/Baseband ADC

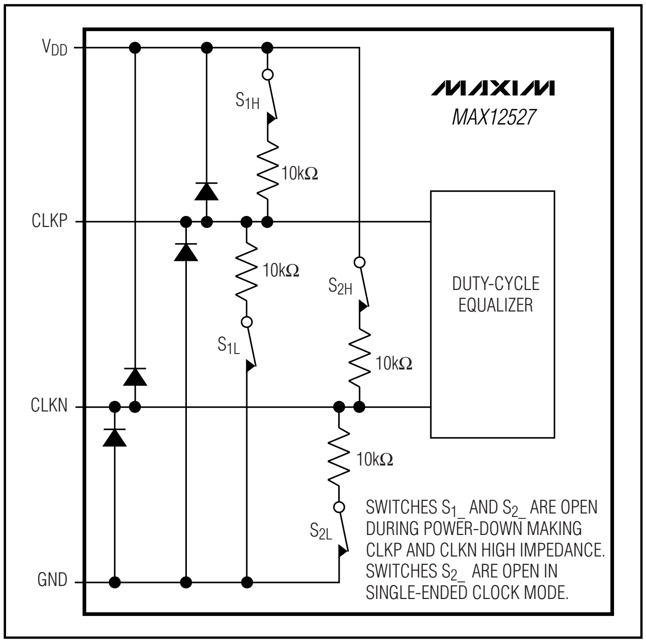


Figure 4. Siimplified Clock Input Circuit

sampling provides design flexibility, relaxes clock requirements, and can minimize clock jitter.

System Timing Requirements

Figure 5 shows the timing relationship between the clock, analog inputs, DAV indicator, DOR_ indicators, and the resulting output data. The analog input is sampled on the falling (rising) edge of CLKP (CLKN) and the resulting data appears at the digital outputs 8 clock cycles later.

The DAV indicator is synchronized with the digital output and optimized for use in latching data into digital back-end circuitry. Alternatively, digital back-end circuitry can be latched with the rising edge of the conversion clock (CLKP - CLKN).

Table 2. Clock-Divider Control Inputs

DIV4	DIV2	FUNCTION
0	0	Clock Divider Disabled $f_{SAMPLE} = f_{CLK}$
0	1	Divide-by-Two Clock Divider $f_{SAMPLE} = f_{CLK} / 2$
1	0	Divide-by-Four Clock Divider $f_{SAMPLE} = f_{CLK} / 4$
1	1	Not Allowed

Data-Valid Output

DAV is a single-ended version of the input clock that is compensated to correct for any input clock duty-cycle variations. The MAX12527 output data changes on the falling edge of DAV, and DAV rises once the output data is valid. The falling edge of DAV is synchronized to have a 5.4ns delay from the falling edge of the input clock. Output data at D0A/B–D11A/B and DORA/B are valid from 7ns before the rising edge of DAV to 7ns after the rising edge of DAV.

DAV enters high impedance when the MAX12527 is powered down (PD = OV_{DD}). DAV enters its high-impedance state 10ns after the rising edge of PD and becomes active again 10ns after PD transitions low.

DAV is capable of sinking and sourcing 600µA and has three times the driving capabilities of D0A/B–D11A/B and DORA/B. DAV is typically used to latch the MAX12527 output data into an external digital back-end circuit. Keep the capacitive load on DAV as low as possible (<15pF) to avoid large digital currents feeding back into the analog portion of the MAX12527, thereby degrading its dynamic performance. Buffering DAV

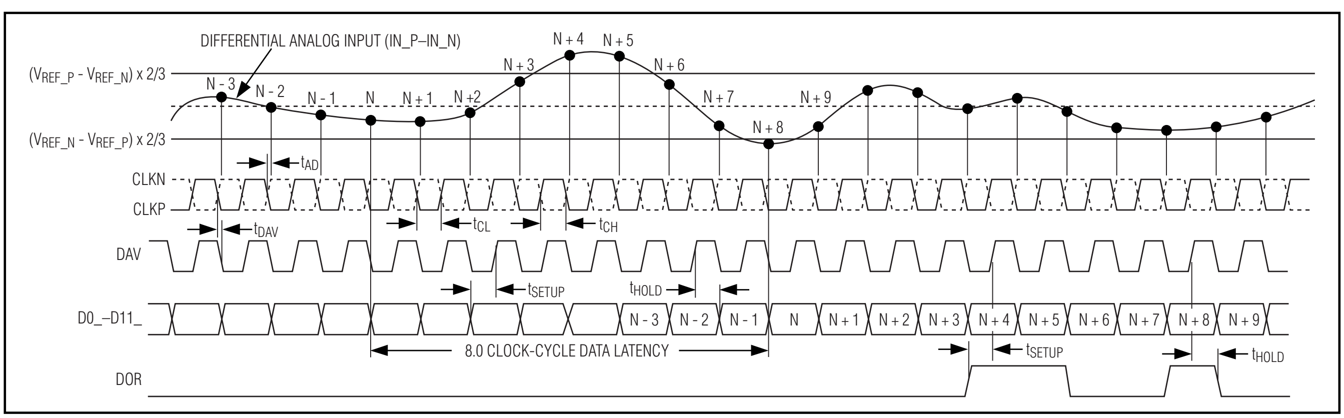


Figure 5. System Timing Diagram

externally isolates it from heavy capacitive loads. Refer to the MAX12527 EV Kit schematic for recommendations of how to drive the DAV signal through an external buffer.

Data Out-of-Range Indicator

The DORA and DORB digital outputs indicate when the analog input voltage is out of range. When DOR_ is high, the analog input is out of range. When DOR_ is low, the analog input is within range. The valid differential input range is from (V_{REF_P} - V_{REF_N}) x 2/3 to (V_{REF_N} - V_{REF_P}) x 2/3. Signals outside of this valid differential range cause DOR_ to assert high as shown in Table 1.

DOR is synchronized with DAV and transitions along with the output data D11–D0. There is an 8 clock-cycle latency in the DOR function as is with the output data (Figure 5). DOR_ is high impedance when the MAX12527 is in power-down (PD = high). DOR_ enters a high-impedance state within 10ns after the rising edge of PD and becomes active 10ns after PD's falling edge.

Digital Output Data and Output Format Selection

The MAX12527 provides two 12-bit, parallel, tri-state output buses. D0A/B–D11A/B and DORA/B update on the falling edge of DAV and are valid on the rising edge of DAV.

The MAX12527 output data format is either Gray code or two's complement depending on the logic input G/$\overline{T}$. With G/$\overline{T}$ high, the output data format is Gray code. With G/$\overline{T}$ low, the output data format is set to two's complement. See Figure 8 for a binary-to-Gray and Gray-to-binary code conversion example.

The following equations, Table 3, Figure 6, and Figure 7 define the relationship between the digital output and the analog input.

Gray Code (G/$\overline{T}$ = 1):

$$V_{IN\_P} - V_{IN\_N} = 2/3 \times (V_{REF\_P} - V_{REF\_N}) \times 2 \times (CODE_{10} - 2048) / 4096$$

Two's Complement (G/$\overline{T}$ = 0):

$$V_{IN\_P} - V_{IN\_N} = 2/3 \times (V_{REF\_P} - V_{REF\_N}) \times 2 \times CODE_{10} / 4096$$

where $CODE_{10}$ is the decimal equivalent of the digital output code as shown in Table 3.

Table 3. Output Codes vs. Input Voltage

GRAY-CODE OUTPUT CODE (G/$\overline{T}$ = 1)				TWO'S COMPLEMENT OUTPUT CODE (G/$\overline{T}$ = 0)				
BINARY D11A–D0A D11B–D0B	DOR	HEXADECIMAL EQUIVALENT OF D11A–D0A D11B–D0B	DECIMAL EQUIVALENT OF D11A–D0A D11B–D0B ($CODE_{10}$)	BINARY D11A–D0A D11B–D0B	DOR	HEXADECIMAL EQUIVALENT OF D11A–D0A D11B–D0B	DECIMAL EQUIVALENT OF D11A–D0A D11B–D0B ($CODE_{10}$)	V_{IN_P} - V_{IN_N} V_{REF_P} = 2.418V V_{REF_N} = 0.882V
1000 0000 0000	**1**	0x800	+4095	0111 1111 1111	**1**	0x7FF	+2047	>+1.0235V (DATA OUT OF RANGE)
1000 0000 0000	0	0x800	+4095	0111 1111 1111	0	0x7FF	+2047	+1.0235V
1000 0000 0001	0	0x801	+4094	0111 1111 1110	0	0x7FE	+2046	+1.0230V
1100 0000 0011	0	0xC03	+2050	0000 0000 0010	0	0x002	+2	+0.0010V
1100 0000 0001	0	0xC01	+2049	0000 0000 0001	0	0x001	+1	+0.0005V
1100 0000 0000	0	0xC00	+2048	0000 0000 0000	0	0x000	0	+0.0000V
0100 0000 0000	0	0x400	+2047	1111 1111 1111	0	0xFFF	-1	-0.0005V
0100 0000 0001	0	0x401	+2046	1111 1111 1110	0	0xFFE	-2	-0.0010V
0000 0000 0001	0	0x001	+1	1000 0000 0001	0	0x801	-2047	-1.0235V
0000 0000 0000	0	0x000	0	1000 0000 0000	0	0x800	-2048	-1.0240V
0000 0000 0000	**1**	0x000	0	1000 0000 0000	**1**	0x800	-2048	<-1.0240V (DATA OUT OF RANGE)

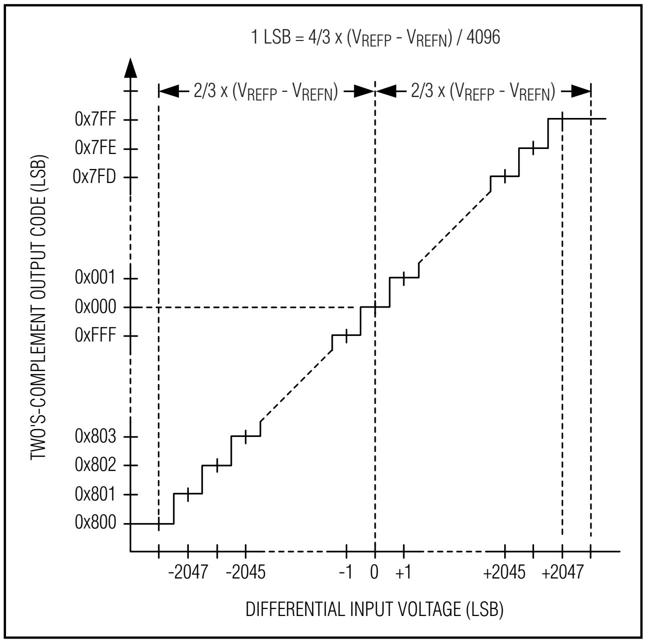


Figure 6. Two's-Complement Transfer Function (G/$\overline{T}$ = 0)

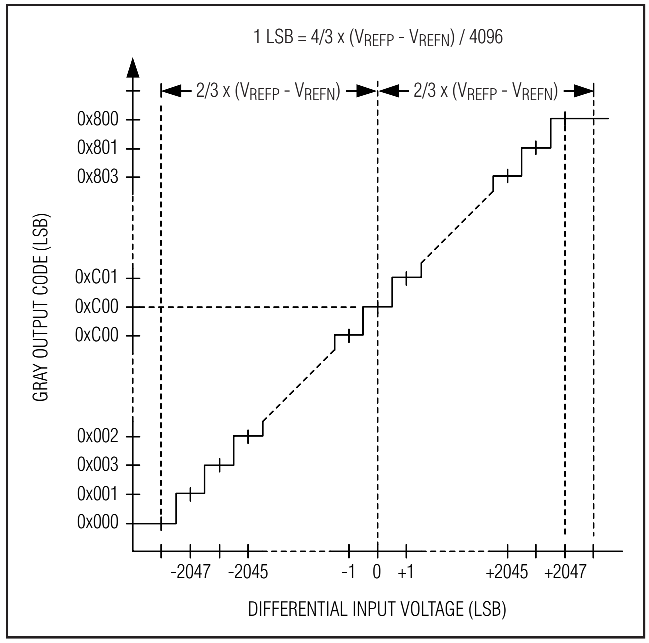


Figure 7. Gray-Code Transfer Function (G/$\overline{T}$ = 1)

The digital outputs D0A/B–D11A/B are high impedance when the MAX12527 is in power-down (PD = 1) mode. D0A/B–D11A/B enter this state 10ns after the rising edge of PD and become active again 10ns after PD transitions low.

Keep the capacitive load on the MAX12527 digital outputs D0A/B–D11A/B as low as possible (<15pF) to avoid large digital currents feeding back into the analog portion of the MAX12527 and degrading its dynamic performance. Adding external digital buffers on the digital outputs helps isolate the MAX12527 from heavy capacitive loads. To improve the dynamic performance of the MAX12527, add 220Ω resistors in series with the digital outputs close to the MAX12527. See the MAX12557 EV kit schematic for guidelines of how to drive the digital outputs through 220Ω series resistors and external digital output buffers.

Power-Down Input

The MAX12527 has two power modes that are controlled with a power-down digital input (PD). With PD low, the MAX12527 is in its normal operating mode. With PD high, the MAX12527 is in power-down mode.

The power-down mode allows the MAX12527 to efficiently use power by transitioning to a low-power state when conversions are not required. Additionally, the MAX12527 parallel output bus goes high-impedance in power-down mode, allowing other devices on the bus to be accessed.

In power-down mode all internal circuits are off, the analog supply current reduces to less than 50µA, and the digital supply current reduces to 1µA. The following list shows the state of the analog inputs and digital outputs in power-down mode.

1) INAP/B, INAN/B analog inputs are disconnected from the internal input amplifier (Figure 3).
2) REFOUT has approximately 17kΩ to GND.
3) REFAP/B, COMA/B, REFAN/B enter a high-impedance state with respect to V_{DD} and GND, but there is an internal 4kΩ resistor between REFAP/B and COMA/B as well as an internal 4kΩ resistor between REFAN/B and COMA/B.
4) D0A–D11A, D0B–D11B, DORA, and DORB enter a high-impedance state.
5) DAV enters a high-impedance state.
6) CLKP, CLKN clock inputs enter a high-impedance state (Figure 4).

The wake-up time from power-down mode is dominated by the time required to charge the capacitors at REF_P, REF_N, and COM. In internal reference mode and buffered external reference mode the wake-up time is typically 10ms. When operating in the unbuffered external reference mode the wake-up time is dependent on the external reference drivers.

MAXIM

BINARY-TO-GRAY CODE CONVERSION

1) THE MOST SIGNIFICANT GRAY-CODE BIT IS THE SAME AS THE MOST SIGNIFICANT BINARY BIT.

D11 → D7 → D3 → D0	BIT POSITION
0 1 1 1 0 1 0 0 1 1 0 0	BINARY
0	GRAY CODE

2) SUBSEQUENT GRAY-CODE BITS ARE FOUND ACCORDING TO THE FOLLOWING EQUATION:

$GRAY_X = BINARY_X \oplus BINARY_{X+1}$

WHERE $\oplus$ IS THE EXCLUSIVE OR FUNCTION (SEE TRUTH TABLE BELOW) AND X IS THE BIT POSITION:

$GRAY_{10} = BINARY_{10} \oplus BINARY_{11}$

$GRAY_{10} = 1 \oplus 0$

$GRAY_{10} = 1$

D11 → D7 → D3 → D0	BIT POSITION
0 $\oplus$ 1 1 1 0 1 0 0 1 1 0 0	BINARY
0 1	GRAY CODE

3) REPEAT STEP 2 UNTIL COMPLETE:

$GRAY_9 = BINARY_9 \oplus BINARY_{10}$

$GRAY_9 = 1 \oplus 1$

$GRAY_9 = 0$

D11 → D7 → D3 → D0	BIT POSITION
0 1 $\oplus$ 1 1 0 1 0 0 1 1 0 0	BINARY
0 1 0	GRAY CODE

4) THE FINAL GRAY-CODE CONVERSION IS:

D11 → D7 → D3 → D0	BIT POSITION
0 1 1 1 0 1 0 0 1 1 0 0	BINARY
0 1 0 0 1 1 1 0 1 0 1 0	GRAY CODE

GRAY-TO-BINARY CODE CONVERSION

1) THE MOST SIGNIFICANT BINARY BIT IS THE SAME AS THE MOST SIGNIFICANT GRAY-CODE BIT.

D11 → D7 → D3 → D0	BIT POSITION
0 1 0 0 1 1 1 0 1 0 1 0	GRAY CODE
0	BINARY

2) SUBSEQUENT BINARY BITS ARE FOUND ACCORDING TO THE FOLLOWING EQUATION:

$BINARY_X = BINARY_{X+1} \oplus GRAY_X$

WHERE $\oplus$ IS THE EXCLUSIVE OR FUNCTION (SEE TRUTH TABLE BELOW) AND X IS THE BIT POSITION:

$BINARY_{10} = BINARY_{11} \oplus GRAY_{10}$

$BINARY_{10} = 0 \oplus 1$

$BINARY_{10} = 1$

D11 → D7 → D3 → D0	BIT POSITION
0 1 0 0 1 1 1 0 1 0 1 0	GRAY CODE
0 $\oplus$ 1	BINARY

3) REPEAT STEP 2 UNTIL COMPLETE:

$BINARY_9 = BINARY_{10} \oplus GRAY_9$

$BINARY_9 = 1 \oplus 0$

$BINARY_9 = 1$

D11 → D7 → D3 → D0	BIT POSITION
0 1 0 0 1 1 1 0 1 0 1 0	GRAY CODE
0 1 $\oplus$ 1	BINARY

4) THE FINAL BINARY CONVERSION IS:

D11 → D7 → D3 → D0	BIT POSITION
0 1 0 0 1 1 1 0 1 0 1 0	GRAY CODE
0 1 1 1 0 1 0 0 1 1 0 0	BINARY

FIGURE 8 SHOWS THE GRAY-TO-BINARY AND BINARY-TO-GRAY CODE CONVERSION IN OFFSET BINARY FORMAT. THE OUTPUT FORMAT OF THE MAX12527 IS TWO'S-COMPLEMENT BINARY, HENCE EACH MSB OF THE TWO'S-COMPLEMENT OUTPUT CODE MUST BE INSERTED TO REFLECT TRUE OFFSET BINARY FORMAT.

EXCLUSIVE OR TRUTH TABLE

A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Figure 8. Binary-to-Gray and Gray-to-Binary Code Conversion

Applications Information

Using Transformer Coupling

In general, the MAX12527 provides better SFDR and THD with fully differential input signals than single-ended input drive, especially for input frequencies above 125MHz. In differential input mode, even-order harmonics are lower as both inputs are balanced, and each of the ADC inputs only requires half the signal swing compared to single-ended input mode.

An RF transformer (Figure 9) provides an excellent solution to convert a single-ended input source signal to a fully differential signal, required by the MAX12527 for optimum performance. Connecting the center tap of the transformer to COM provides a V_{DD} / 2 DC level shift to the input. Although a 1:1 transformer is shown, a step-up transformer can be selected to reduce the drive requirements. A reduced signal swing from the input driver, such as an op amp, can also improve the overall distortion. The configuration of Figure 9 is good for frequencies up to Nyquist (f_{CLK} / 2).

The circuit of Figure 10 converts a single-ended input signal to fully differential just as Figure 9. However, Figure 10 utilizes an additional transformer to improve the common-mode rejection allowing high-frequency signals beyond the Nyquist frequency. A set of 75Ω and 113Ω termination resistors provide an equivalent 50Ω termination to the signal source. The second set of termination resistors connects to COM_ providing the correct input common-mode voltage. Two 0Ω resistors in series with the analog inputs allow high IF input frequencies. These 0Ω resistors can be replaced with low-value resistors to limit the input bandwidth.

Single-Ended AC-Coupled Input Signal

Figure 11 shows an AC-coupled, single-ended input application. The MAX4108 provides high speed, high bandwidth, low noise, and low distortion to maintain the input signal integrity.

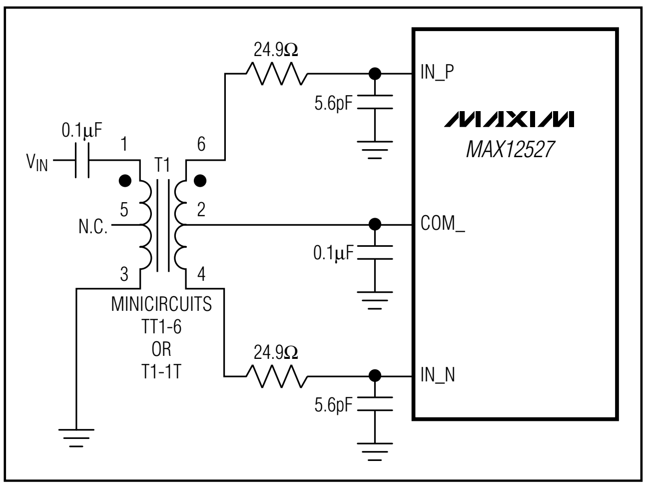


Figure 9. Transformer-Coupled Input Drive for Input Frequencies Up to Nyquist

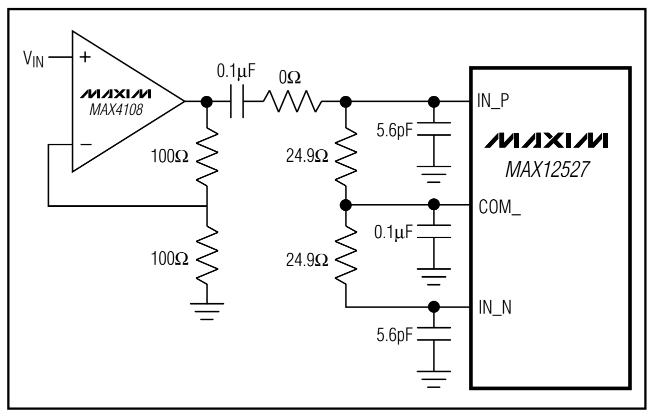


Figure 11. Single-Ended, AC-Coupled Input Drive

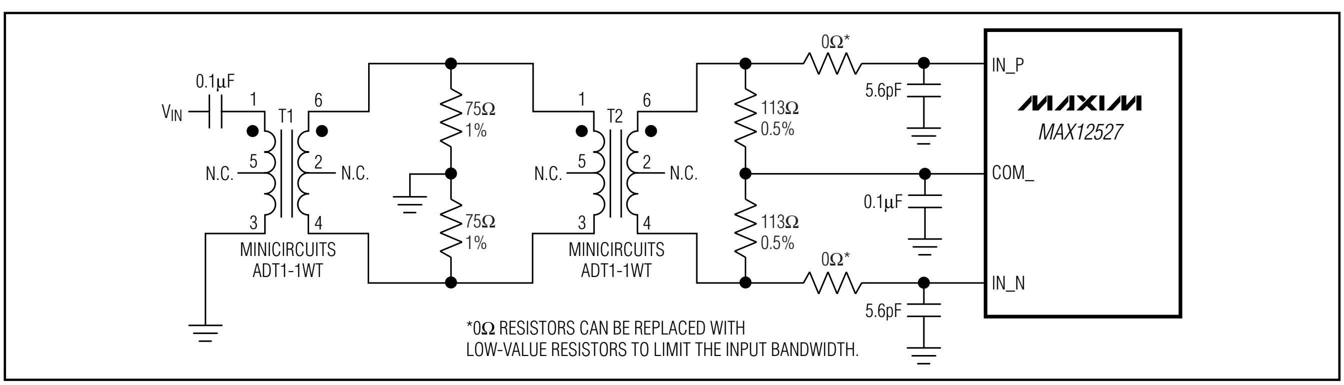


Figure 10. Transformer-Coupled Input Drive for Input Frequencies beyond Nyquist

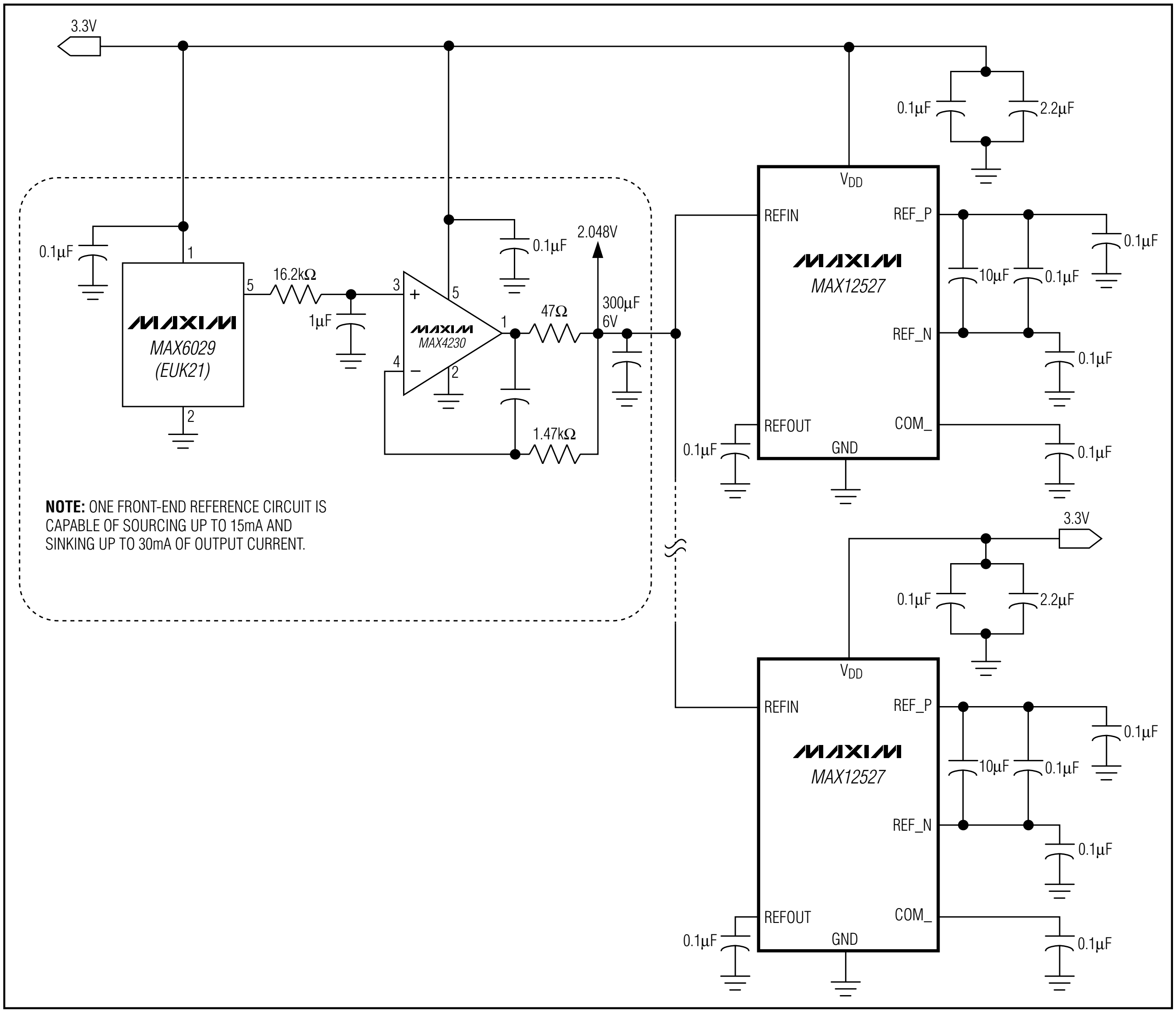


Figure 12. External Buffered (MAX4230) Reference Drive Using a MAX6029 Bandgap Reference

Buffered External Reference Drives Multiple ADCs

The buffered external reference mode allows for more control over the MAX12527 reference voltage and allows multiple converters to use a common reference. The REFIN input impedance is >50MΩ.

Figure 12 shows the MAX6029 precision 2.048V bandgap reference used as a common reference for multiple converters. The 2.048V output of the MAX6029 passes through a single-pole 10Hz LP filter to the MAX4230. The MAX4230 buffers the 2.048V reference and provides additional 10Hz LP filtering before its output is applied to the REFIN input of the MAX12527.

Unbuffered External Reference Drives Multiple ADCs

The unbuffered external reference mode allows for precise control over the MAX12527 reference and allows multiple converters to use a common reference. Connecting REFIN to GND disables the internal refer-

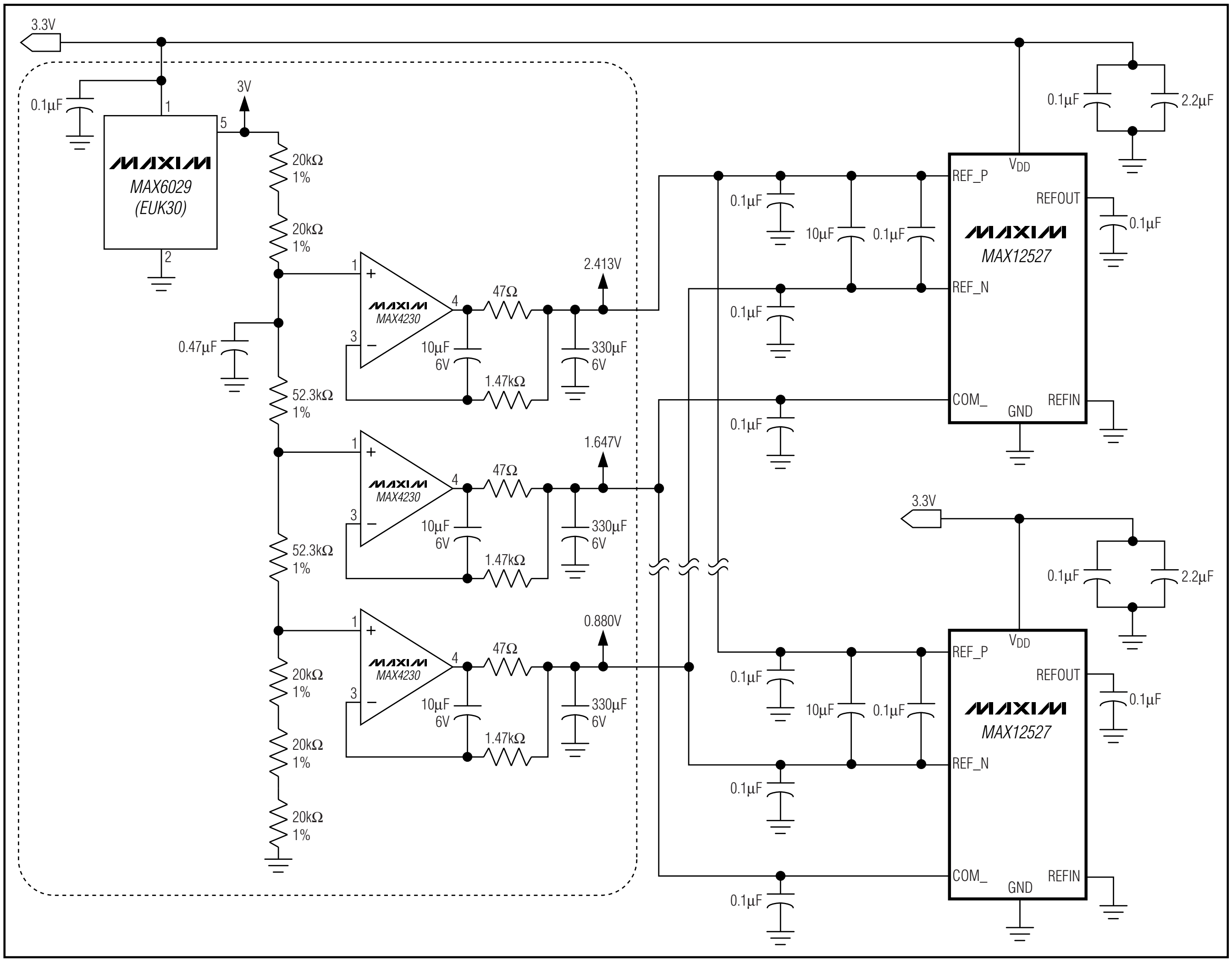


Figure 13. External Unbuffered Reference Driving Multiple ADCs

ence, allowing REF_P, REF_N, and COM_ to be driven directly by a set of external reference sources.

Figure 13 uses a MAX6029 precision 3.000V bandgap reference as a common reference for multiple converters. A seven-component resistive divider chain follows the MAX6029 voltage reference. The 0.47μF capacitor along this chain creates a 10Hz LP filter. Three MAX4230 amplifiers buffer taps along this resistor chain providing 2.413V, 1.647V, and 0.880V to the MAX12527 REF_P, REF_N, and COM_ reference inputs. The feedback around the MAX4230 op amps provides additional 10Hz LP filtering. Reference voltages 2.413V and 0.880V set the full-scale analog input range for the converter to ±1.022V (±[V_{REF_P} - V_{REF_N}] x 2/3).

Note that one single power supply for all active circuit components removes any concern regarding power-supply sequencing when powering up or down.

Grounding, Bypassing, and Board Layout

The MAX12527 requires high-speed board layout design techniques. Refer to the MAX12557 EV kit data sheet for a board layout reference. Locate all bypass capacitors as close to the device as possible, preferably on the same side as the ADC, using surfacemount devices for minimum inductance. Bypass V_{DD} to GND with a 220µF ceramic capacitor in parallel with at least one 10µF, one 4.7µF, and one 0.1µF ceramic capacitor. Bypass OV_{DD} to GND with a 220µF ceramic capacitor in parallel with at least one 10µF, one 4.7µF, and one 0.1µF ceramic capacitor. High-frequency bypassing/decoupling capacitors should be located as close as possible to the converter supply pins.

Multilayer boards with ample ground and power planes produce the highest level of signal integrity. All grounds and the exposed backside paddle of the MAX12527 must be connected to the same ground plane. The MAX12527 relies on the exposed backside paddle connection for a low-inductance ground connection. Isolate the ground plane from any noisy digital system ground planes such as a DSP or output buffer ground.

Route high-speed digital signal traces away from the sensitive analog traces. Keep all signal lines short and free of 90° turns.

Ensure that the differential, analog input network layout is symmetric and that all parasitic components are balanced equally. Refer to the MAX12557 EV kit data sheet for an example of symmetric input layout.

Parameter Definitions

Integral Nonlinearity (INL)

INL is the deviation of the values on an actual transfer function from a straight line. For the MAX12527, this straight line is between the endpoints of the transfer function, once offset and gain errors have been nullified. INL deviations are measured at every step of the transfer function and the worst-case deviation is reported in the *Electrical Characteristics* table.

Differential Nonlinearity (DNL)

DNL is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function. For the MAX12527, DNL deviations are measured at every step of the transfer function and the worst-case deviation is reported in the *Electrical Characteristics* table.

Offset Error

Offset error is a figure of merit that indicates how well the actual transfer function matches the ideal transfer function at a single point. Ideally, the midscale MAX12527 transition occurs at 0.5 LSB above midscale. The offset error is the amount of deviation between the measured midscale transition point and the ideal midscale transition point.

Gain Error

Gain error is a figure of merit that indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. The slope of the actual transfer function is measured between two data points: positive full scale and negative full scale. Ideally, the positive full-scale MAX12527 transition occurs at 1.5 LSBs below positive full scale, and the negative full-scale transition occurs at 0.5 LSB above negative full scale. The gain error is the difference of the measured transition points minus the difference of the ideal transition points.

Small-Signal Noise Floor (SSNF)

SSNF is the integrated noise and distortion power in the Nyquist band for small-signal inputs. The DC offset is excluded from this noise calculation. For this converter, a small signal is defined as a single tone with an amplitude of -35dBFS. This parameter captures the thermal and quantization noise characteristics of the data converter and can be used to help calculate the overall noise figure of a digital receiver signal path.

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{[max]} = 6.02 \times N + 1.76$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first six harmonics (HD2 through HD7), and the DC offset.

$$SNR = 20 \times \log (SIGNAL_{RMS} / NOISE_{RMS})$$

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to the RMS noise plus distortion. RMS noise plus distortion includes all spectral components to the Nyquist frequency excluding the fundamental and the DC offset.

Dual, 65Msps, 12-Bit, IF/Baseband ADC

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first six harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 + V_7^2}}{V_1}\right)$$

where V_1 is the fundamental amplitude, and V_2 through V_7 are the amplitudes of the 2nd- through 7th-order harmonics (HD2 through HD7).

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset.

Intermodulation Distortion (IMD)

IMD is the total power of the IM2 to IM5 intermodulation products to the Nyquist frequency relative to the total input power of the two input tones f_{IN1} and f_{IN2}. The individual input tone levels are at -7dBFS. The intermodulation products are as follows:

2nd-Order Intermodulation products (IM2):
$f_{IN1} = f_{IN2}$, $f_{IN2} - f_{IN1}$

3rd-Order Intermodulation products (IM3):
$2 \times f_{IN1} - f_{IN2}$, $2 \times f_{IN2} - f_{IN1}$, $2 \times f_{IN1} + f_{IN2}$,
$2 \times f_{IN2} + f_{IN1}$

4th-Order Intermodulation products (IM4):
$3 \times f_{IN1} - f_{IN2}$, $3 \times f_{IN2} - f_{IN1}$, $3 \times f_{IN1} + f_{IN2}$,
$3 \times f_{IN2} + f_{IN1}$, $2 \times f_{IN1} - 2 \times f_{IN2}$, $2 \times f_{IN1} + 2 \times f_{IN2}$,
$2 \times f_{IN2} - 2 \times f_{IN1}$

5th-Order Intermodulation products (IM5):
$3 \times f_{IN1} - 2 \times f_{IN2}$, $3 \times f_{IN2} - 2 \times f_{IN1}$, $3 \times f_{IN1} + 2 \times f_{IN2}$,
$3 \times f_{IN2} + 2 \times f_{IN1}$, $4 \times f_{IN1} - f_{IN2}$, $4 \times f_{IN2} - f_{IN1}$,
$4 \times f_{IN1} + f_{IN2}$, $4 \times f_{IN2} + f_{IN1}$

Note that the two-tone intermodulation distortion is measured with respect to a single-carrier amplitude and not the peak-to-average input power of both input tones.

3rd-Order Intermodulation (IM3)

IM3 is the total power of the 3rd-order intermodulation product to the Nyquist frequency relative to the total input power of the two input tones f_{IN1} and f_{IN2}. The individual input tone levels are at -7dBFS. The 3rd-order intermodulation products are $2 \times f_{IN1} - f_{IN2}$, $2 \times f_{IN2} - f_{IN1}$, $2 \times f_{IN1} + f_{IN2}$, $2 \times f_{IN2} + f_{IN1}$.

Aperture Jitter

Figure 14 shows the aperture jitter (t_{AJ}), which is the sample-to-sample variation in the aperture delay.

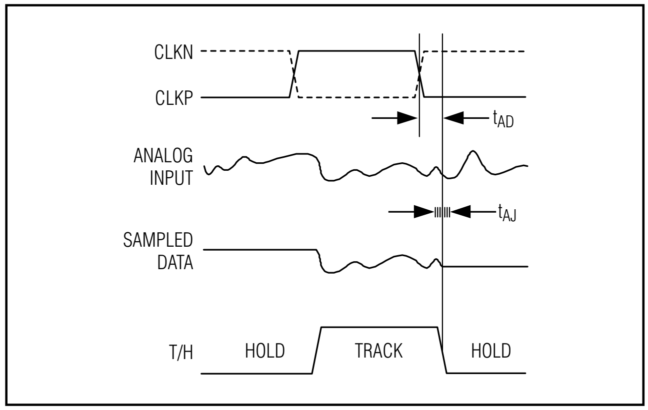


Figure 14. T/H Aperture Timing

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the rising edge of the sampling clock and the instant when an actual sample is taken (Figure 14).

Full-Power Bandwidth

A large -0.2dBFS analog input signal is applied to an ADC and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by -3dB. This point is defined as full-power input bandwidth frequency.

Output Noise (n_{OUT})

The output noise (n_{OUT}) parameter is similar to thermal plus quantization noise and is an indication of the converter's overall noise performance.

No fundamental input tone is used to test for n_{OUT}. IN_P, IN_N, and COM_ are connected together and 1024k data points are collected. n_{OUT} is computed by taking the RMS value of the collected data points after the mean is removed.

Overdrive Recovery Time

Overdrive recovery time is the time required for the ADC to recover from an input transient that exceeds the full-scale limits. The MAX12527 specifies overdrive recovery time using an input transient that exceeds the full-scale limits by ±10%. The MAX12527 requires one clock cycle to recover from the overdrive condition.

Crosstalk

Coupling onto one channel being driven by a (-0.5dBFS) signal when the adjacent interfering channel is driven by a full-scale signal. Measurement includes all spurs resulting from both direct coupling and mixing components.

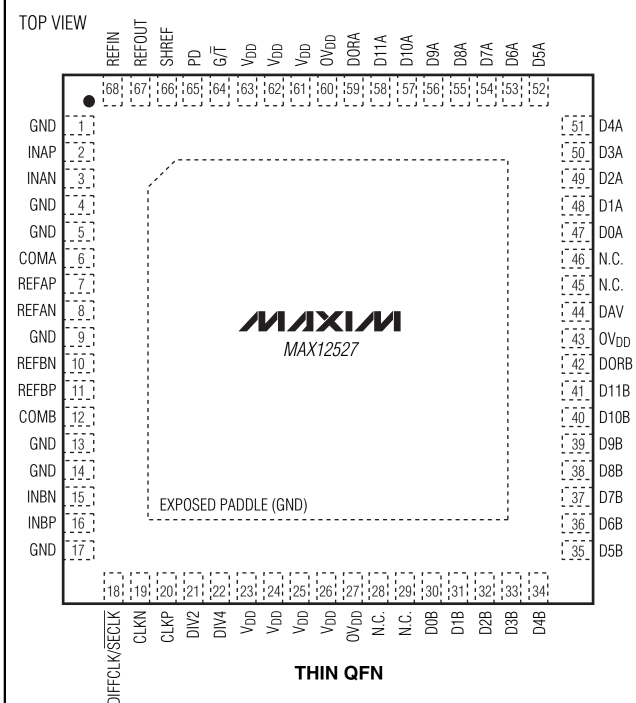
Gain Matching

Gain matching is a figure of merit that indicates how well the gains between the two channels are matched to each other. The same input signal is applied to both channels and the maximum deviation in gain is reported (typically in dB) as gain matching.

Offset Matching

Like gain matching, offset matching is a figure of merit that indicates how well the offsets between the two channels are matched to each other. The same input signal is applied to both channels and the maximum deviation in offset is reported (typically in %FSR) as offset matching.

Pin Configuration



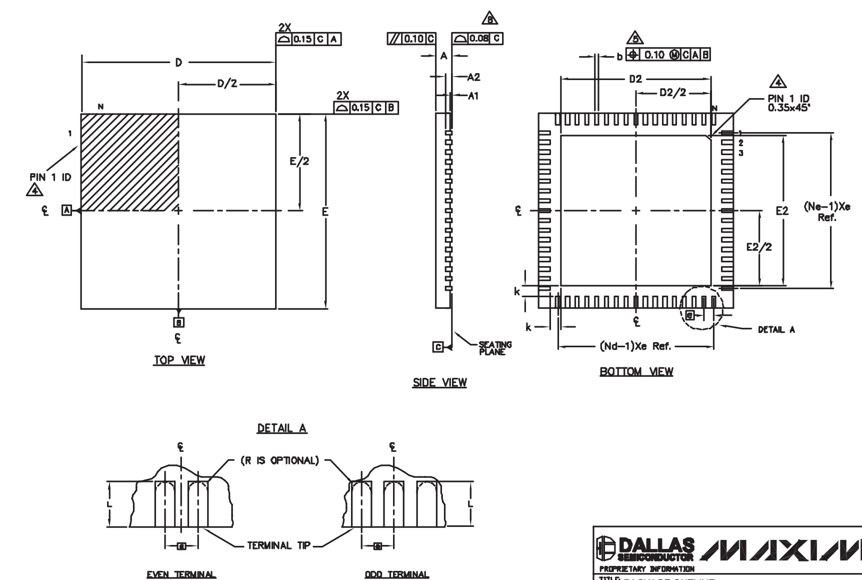
THIN QFN

Dual, 65Msps, 12-Bit, IF/Baseband ADC

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

68L QFN THIN.EPS



DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 68L THIN QFN, 10x10x0.8mm
APPROVAL | DOCUMENT CONTROL NO. 21-0142 | REV. C | 1/2

PKG	68L 10x10			NOTE
REF.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	
A1	0.00	0.01	0.05	
A2	0.20 REF			
b	0.20	0.25	0.30	
D	9.90	10.00	10.10	
E	9.90	10.00	10.10	
e	0.50 BSC.			
k	0.25	-	-	
L	0.45	0.55	0.65	
N	68			
ND	17			
NE	17			
JEDEC	WNND-2			

EXPOSED PAD VARIATIONS							
PKG. CODE	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T6800-1	7.60	7.70	7.80	7.60	7.70	7.80	NO
T6800-2	7.60	7.70	7.80	7.60	7.70	7.80	YES
T6800-3	7.60	7.70	7.80	7.60	7.70	7.80	NO
T6800-4	7.60	7.70	7.80	7.60	7.70	7.80	YES

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO-220.
10. WARPAGE SHALL NOT EXCEED 0.10mm.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 68L THIN QFN, 10x10x0.8mm
APPROVAL | DOCUMENT CONTROL NO. 21-0142 | REV. C | 2/2

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