KOPIN

A300 Display Driver

Part number: KCD-A300-QB

(August. 09, 2006)

General Description

The A300 is a driver for Kopin's CyberDisplay® 300M LV monochrome display. It is designed to accept a standard monochrome video signal (525 or 625 lines), and convert it for the display.

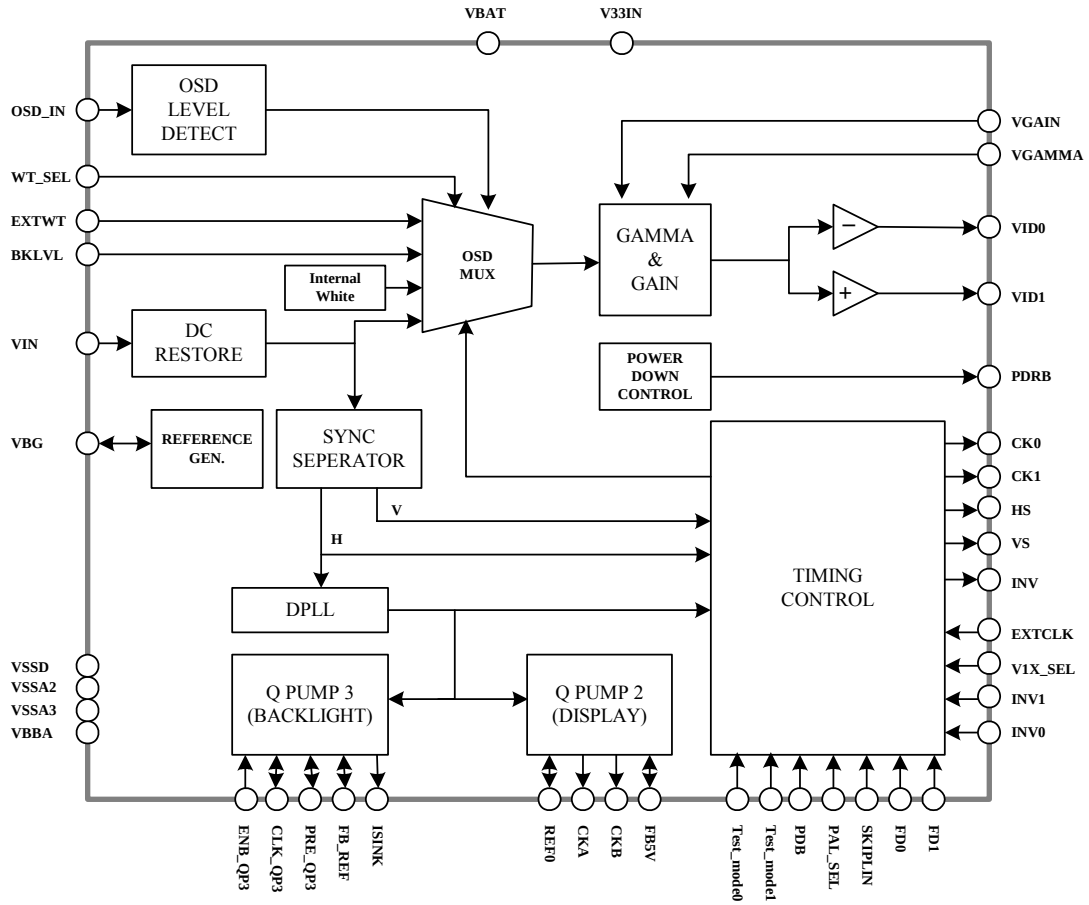
The A300 provides all necessary power supply voltages to the display panel by means of charge pump circuits. The input video signal is converted to appropriate differential video signals required by the LCD Display Panel.

A separate on screen display (OSD) input is provided. An on-chip sync separator, Digital PLL, and logic control section generate the appropriate horizontal and vertical timing signals for the LCD panel.

Features

- Support for 525 and 625 line Monochrome systems
- Integrated DC-DC converter provides all necessary voltages for the LCD display panel
- Internal sync separator, PLL, and Logic provide all necessary timing signals to the LCD display panel
- Gamma bias to adjust the video output characteristics
- Hsync Recovery
- Battery Voltage ; 2.5V ~ 3.6V
- Power down mode
- 48LQFP

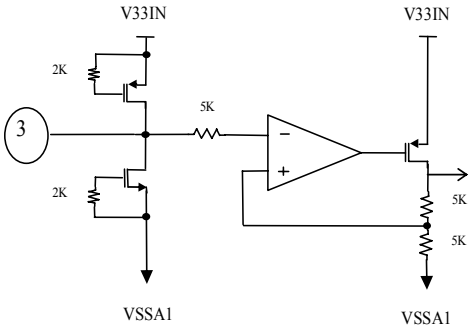
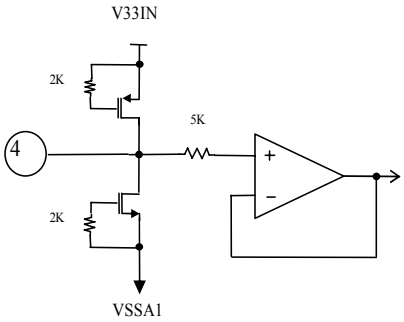
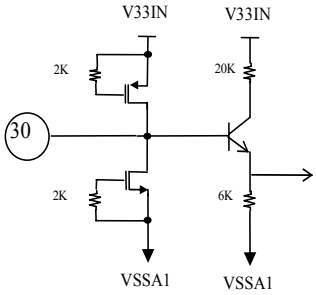
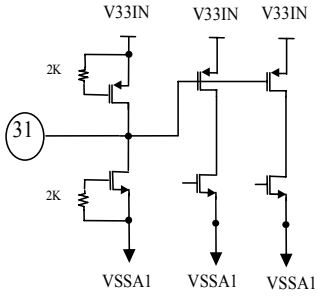
Block Diagram



Pin Descriptions

Pin	Symbol	Description
1	REFO	VREF Buffer Output
2	OSD_IN	Input for the OSD Signals
3	EXTWT	Input for External White Level
4	BKLVL	Black level input
5	VIN	Input for standard level monochrome video
6	VBG	Internally generated voltage reference
7	WT_SEL	Input for external (Low) or internal white level select
8	VSSA1	Analog ground
9	VBBA	Substrate power
10	PDB	Power down (Active low)
11	Test_mode 1	Test input pin
12	N.C	No Connection
13	VSSD	Digital ground
14,15	FD0, FD1	Field delay control, FD0: delay even field by one row FD1: delay odd field by one row
16	SKIPLIN	Line skipping mode for PAL vertical scaling
17	PAL_MODE	NTSC / PAL select, NTSC: low, PAL: high
18	Test_mode 0	Test input pin
19,20	INV0 / INV1	Inversion control, INV0 INV1 0 0 Frame mode 0 1 Pixel mode 1 0 Column mode 1 1 Row mode
21	V1X_SEL	Vertical 1x at ‘high’ state, 2x Inversion control at ‘low’ state
22	EXTCLK	Clock input pin for test
23	INV	Inversion control output
24	HS	Horizontal output signal
25	VS	Vertical output signal
26,27	CK0 / CK1	Pixel clock output 0/1
28	VSSA2	Analog ground
29	VID1	Upper video drive signal to the LCD panel
30	VGAMMA	Gamma bias adjust
31	VGAIN	Gain bias adjust
32	VID0	Lower video drive signal to the LCD panel
33	PDRB	Power down reset output to the LCD panel (Active low)
34	ISINK	LED current control
35	VSSA3	Analog ground
36	FB_REF	Sink current control
37	PRE_QP3	QPUMP3 clock buffer output
38	CLK_QP3	QPUMP3 clock buffer output
39	V33IN	3.3V regulated power supply
40	N.C	No Connection
41	N.C	No Connection
42	N.C	No Connection
43	ENB_QP3	QPUMP3 enable input (Active low)
44	VBAT	Battery input
45	CLKB	QPUMP2 clock buffer output
46	CLKA	QPUMP2 clock buffer output
47	N.C	No Connection
48	FB5V	QPUMP2 voltage feedback

Equivalent Circuit for Analog Inputs

Pin No.	Symbol	Equivalent Circuit	Function	Signal Waveform
3	EXTWT		White level input, CMOS buffer input	DC
4	BKLVL		Black level input, CMOS buffer input	DC
30	VGAM MA		Gamma control input, NPN bipolar transistor input with Beta=~45	DC
31	VGAIN		Gain Control input, CMOS gate input	DC

Absolute Maximum Ratings

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
VBAT	Supply Voltage	-0.5	4.0	V
V33IN	Supply Voltage	-0.5	4.0	V
VIND	Digital Input Pin Voltage	VSSD-0.3	V33IN+0.3	V
VINA	Analog Input Pin Voltage	VSSA-0.3	VBAT+0.3	V
Tstorage	Storage Temperature	-40	125	°C

Recommended Operating Conditions

Parameter	Conditions	MIN	TYP	MAX	UNIT
Power Supply Voltage	VBAT	2.5		3.6	V
Power Supply Voltage	V33IN	2.7		3.6	V
Video signal input level (Composite video-luma)		-	1.0	-	Vp-p
OSD input level		0	-	VBAT	V
Logic input level		0	-	VBAT	V
VGAIN bias range		1.2	-	2.0	V
VGAMMA bias range		1.2	-	2.0	V
External white level	Internal white level = 2*External White level	0	-	1.5	V
Operating temperature range		-20		70	°C

Electrical Characteristics

(All parameters are specified at Ta=25°C, V33IN=3.3V, unless otherwise noted.)

DC Characteristics

Parameter	Conditions	MIN	TYP	MAX	UNIT
Supply current	V33IN=3.3V		13		mA
Shutdown current	PDB=Low		100	-	μA

PLL/SYNC Separator / Video Amplifier

Parameter	Conditions	MIN	TYP	MAX	UNIT
VBG Bandgap Reference(Pin6)	VBAT=3.3V	1.15	1.23	1.3	V
Pixel Clock Output		-	24	-	MHz
PLL Lock Range		14.175	-	17.1875	kHz

Power_Down_Reset (PDR)

Parameter	Conditions	MIN	TYP	MAX	UNIT
RST threshold		2.2	2.3	2.4	V
Hysterisis			0.1		V

Display_Pump (QPUMP 2)

Parameter	Conditions	MIN	TYP	MAX	UNIT
Input voltage		2.5		3.6	V
Output voltage	IOUT≤5㎃, 2.5V≤VIN≤3.6V	-4.8	-5	-5.2	V
Output current			1	5	㎃
Oscillator frequency	During active period		375		kHz
Ripple voltage	IOUT=1㎃		60		mV
Quiescent current	IOUT=0㎃, VIN=2.5V to 3.6V		70	120	㎂
Shutdown current	PDB=Low			1	㎂
Line regulation	2.5V≤VIN≤3.6V		40	50	㎃
Load regulation	0㎃≤VLOAD≤1㎃		40	50	㎃

Backlight_Pump (QPUMP3)

Parameter	Conditions	MIN	TYP	MAX	UNIT
Input voltage		2.5		3.6	V
Output voltage	IOUT≤30㎃, 2.5V≤VIN≤3.6V	-	3.6	-	V
Output current				30	㎃
Oscillator frequency	During active period		375		kHz
Ripple voltage	ISINK=10㎃		60		㎃
Quiescent current	ISINK=0㎃, VIN=2.5V to 3.6V		70	120	㎂
Shutdown current	PDB=Low and/or ENB_QP3=Low			1	㎂

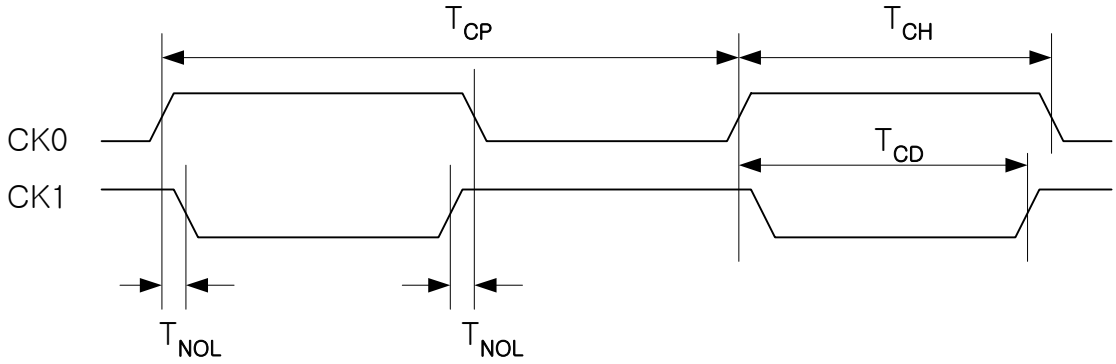
OSD_Detector

Parameter	Conditions	MIN	TYP	MAX	UNIT
Input voltage		0		VBAT	V
OSDWT threshold			2/3 VBAT		V
OSDBK threshold			1/3 VBAT		V
OSDWT delay			20	30	ns
OSDBK delay			20	30	ns

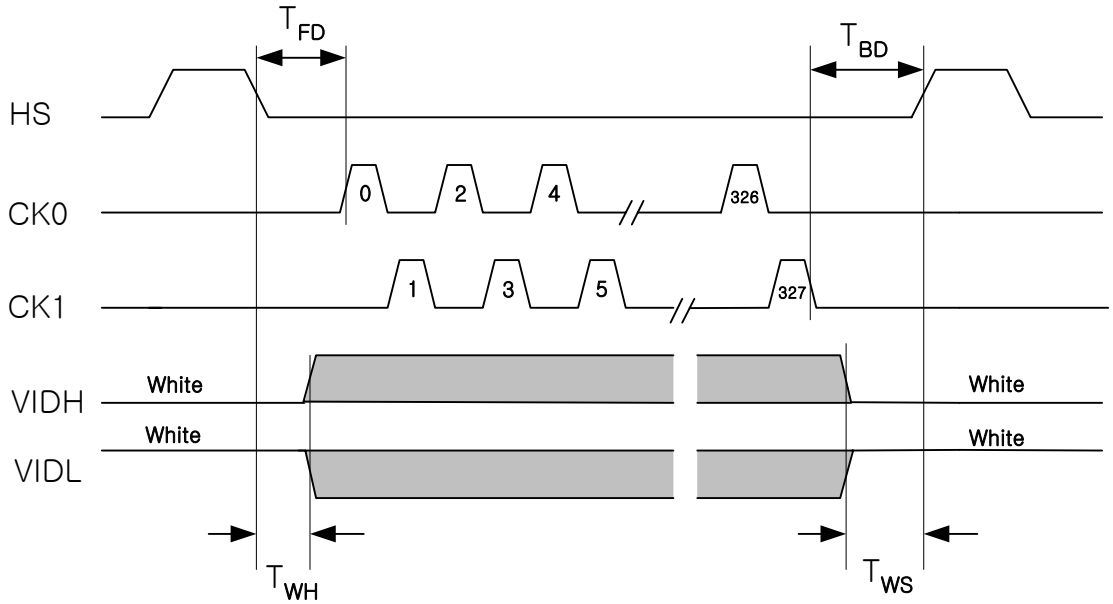
GAIN & GAMMA

Parameter	Conditions	MIN	TYP	MAX	UNIT
Input voltage		1.15		2.05	V
VGAIN bias range		1.2		2.0	V
VGAMMA bias		1.2		2.0	V
Gain under breakpoint	VIN=1.15V,VGAMMA=1.5V	3.4		8.5	dB
Gain upper breakpoint	VIN=1.85V,VGAMMA=1.5V	3.9		4.0	dB

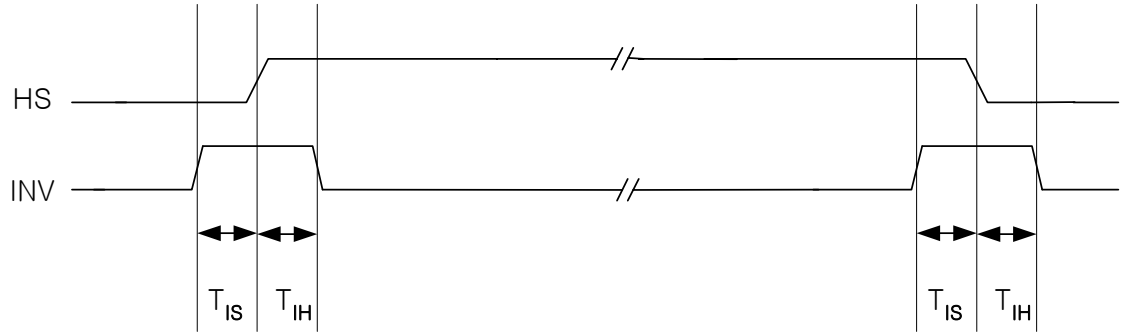
AC Characteristics



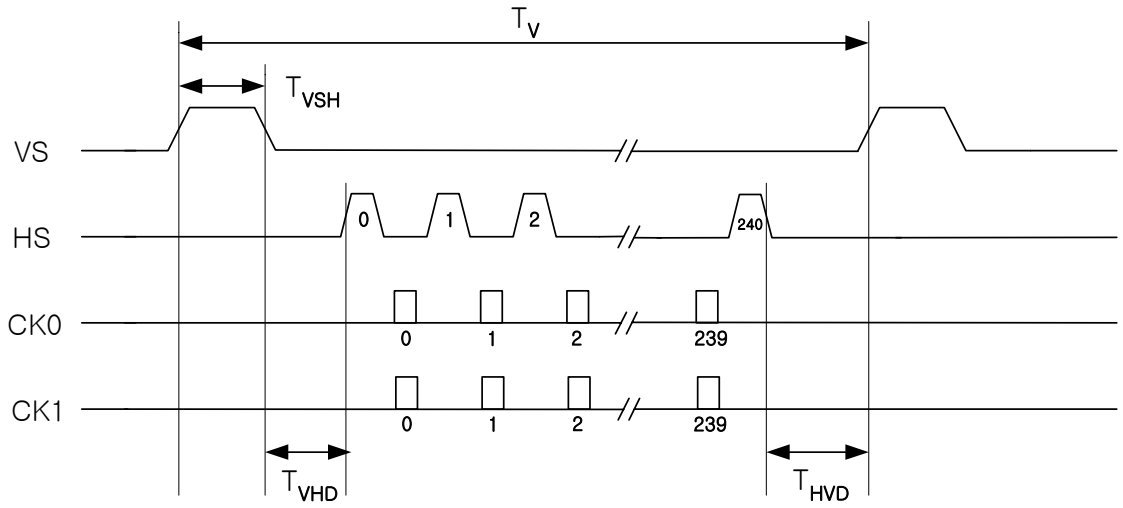
Symbol	Parameter	MIN	TYP	MAX	Unit
T_{NOL}	CK0 and CK1 Non-overlap Time	1	5	-	ns
T_{CP}	Clock Period	-	333	-	ns
$2/T_{CP}$	Pixel Rate	-	6	-	MHz
T_{CH}	Clock High Pulse Width	120	-	-	ns
T_{CD}	CK0 to CK1 Delay	$(T_{CP}/2)$-5	$T_{CP}/2$	$(T_{CP}/2)$+5	ns



Symbol	Parameter	MIN	TYP	MAX	Unit
T_{FD}	HS TO 1ST CK0 Delay	1.4		-	µs
T_{BD}	327th CK0 to HS Delay	1.4		-	µs
T_{WH}	White Hold After HS	500		-	ns
T_{WS}	White Setup Before HS	500		-	ns



Symbol	Parameter	MIN	TYP	MAX	Unit
T_{IS}	INV Setup Time	300		-	ns
T_{IH}	INV Hold Time	300		-	ns



Symbol	Parameter	MIN	TYP	MAX	Unit
T_V	Field Period		16.7 – 20.0	-	ms
$(1/T_V)$	Field Rate		50 - 60	-	Hz
T_{VSH}	VS High Pulse Width	10		-	µs
T_{VHD}	VS to HS Delay	10		-	µs
T_{HVD}	HS to VS Delay	10			µs

Application Information

Video Input

An AC coupled video signal is input to Video In pin 5 via capacitor, normally 0.1uF. When using PAL video signal, pin 17 tied to high. The standard horizontal video timing is shown Fig. 1.

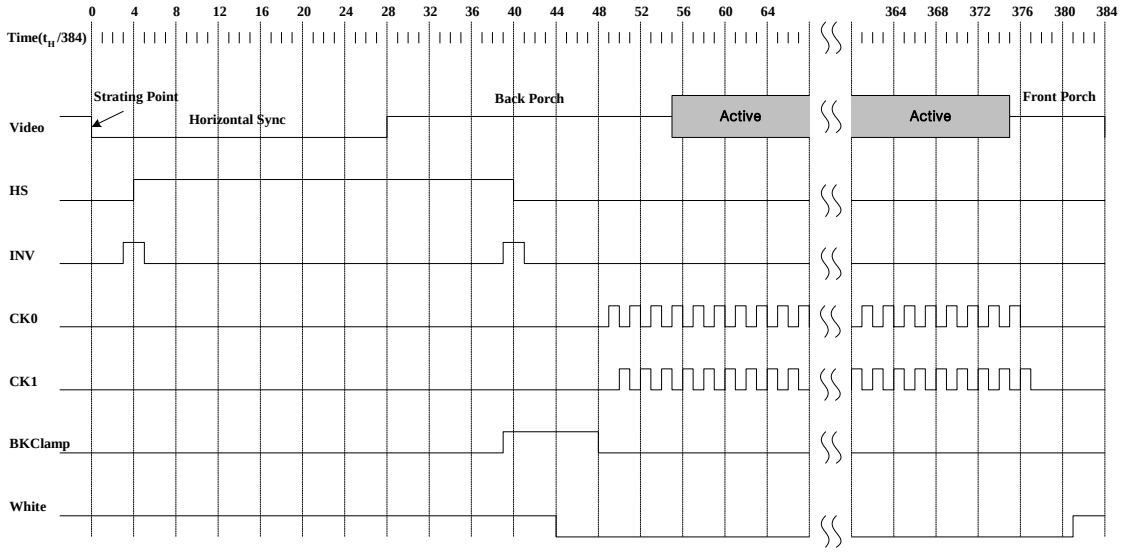
Inversion control

A liquid crystal display requires polarity inversion to maintain DC balance across the liquid crystal. The CyberDisplay 300M LV contains internal logic supporting four inversion modes: pixel, column, row, or frame (Table 2). The inversion mode is selected by two bits INV0 and INV1. The CyberDisplay 300M LV inverts polarity with every pulse of VS, normally once per field. This so-called "2X rate" is preferable for most applications. However, 1X inversion may be accomplished when the V1X_SEL pin is tied high.

Table 2: Inversion Control

INV0=low, INV1=low	Frame mode
INV0=low, INV1=high	Pixel mode
INV0=high, INV1=low	Column mode
INV0=high, INV1=high	Row mode

Fig. 1: Horizontal Video Timing



Field Delay Control (FD0, FD1)

The vertical start pulse can be delayed in even and/or odd field by 1 or 2 line. Start position is shown below in Figures 2 - 9.

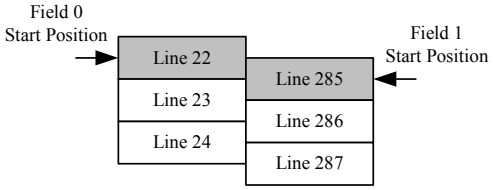


Fig. 2 NTSC Mode
FD0 = 0 , FD1 = 0

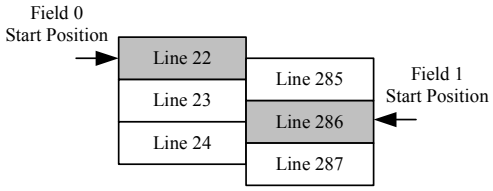


Fig. 3 NTSC Mode
FD0 = 0 , FD1 = 1

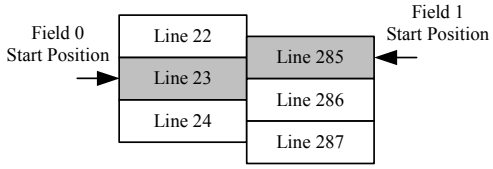


Fig. 4 NTSC Mode
FD0 = 1 , FD1 = 0

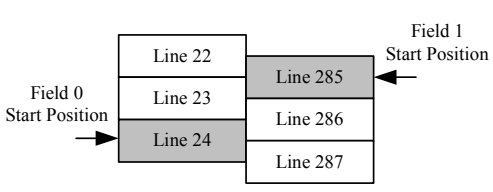


Fig. 5 NTSC Mode
FD0 = 1 , FD1 = 1

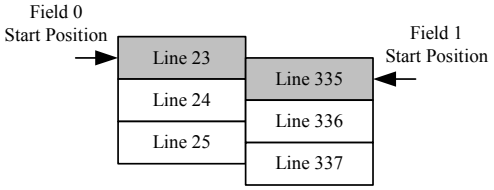


Fig. 6 PAL Mode
FD0 = 0 , FD1 = 0

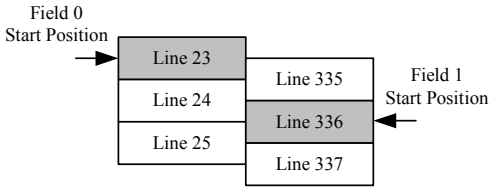


Fig. 7 PAL Mode
FD0 = 0 , FD1 = 1

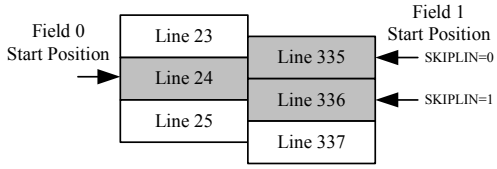


Fig. 8 PAL Mode
FD0 = 1 , FD1 = 0

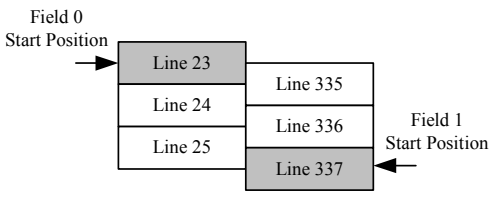


Fig. 9 PAL Mode
FD0 = 1 , FD1 = 1

Vertical Scaling in PAL Mode (SKIPLIN)

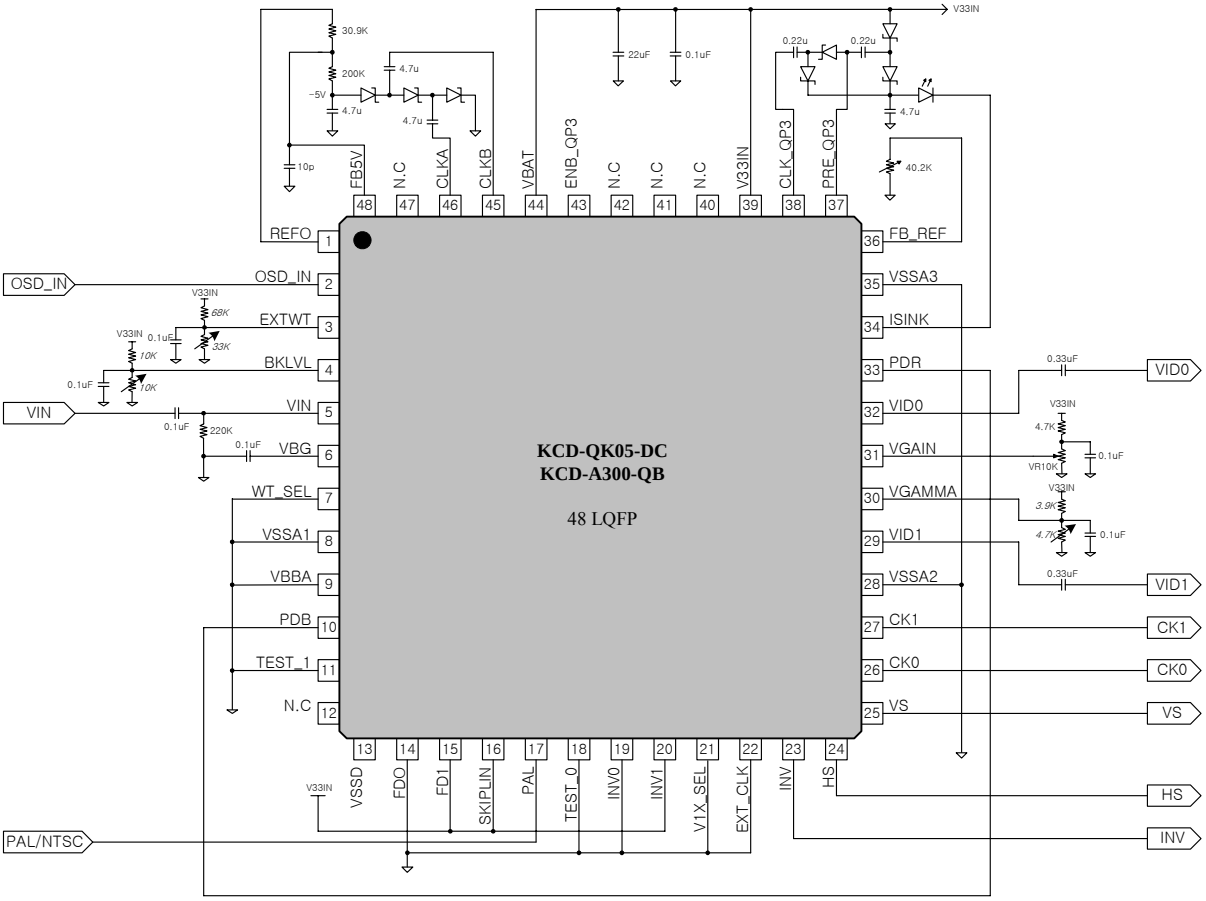
The PAL video format has 625 lines per frame, of which 576 are active. Vertical scaling must be performed to match 576÷2=288 lines per field to the display's 240 physical rows. Two 6:5 scaling modes may be selected by the LINESKP pin.

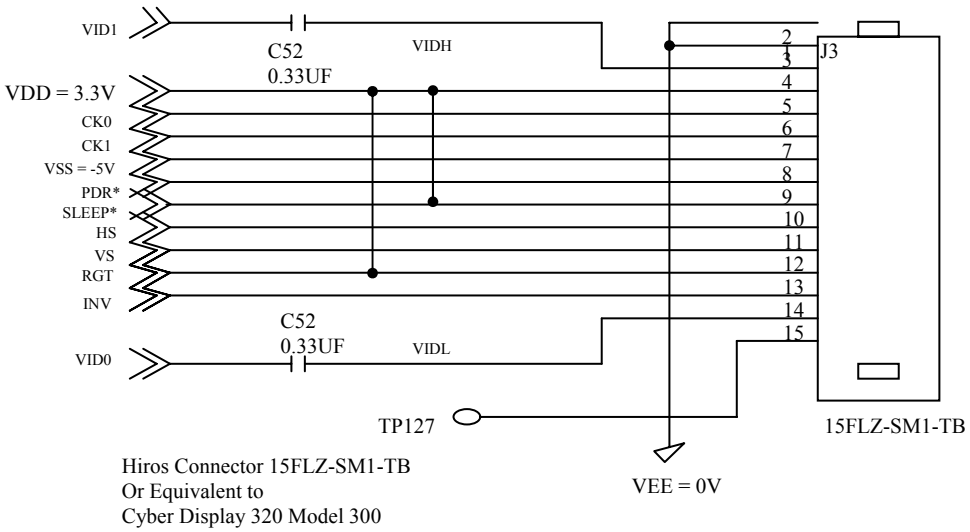
Skiplin	Fd0	Fd1	Field 0		Field 1	
			Start line number	Skip line number	Start line number	Skip line number
0	0	0	23	28 + 6N (n=0,1,2,…)	335	337 + 6N (n=0,1,2,…)
0	0	1	23	28 + 6N (n=0,1,2,…)	336	338 + 6N (n=0,1,2,…)
0	1	0	24	29 + 6N (n=0,1,2,…)	335	337 + 6N (n=0,1,2,…)
0	1	1	23	28 + 6N (n=0,1,2,…)	337	339 + 6N (n=0,1,2,…)
1	0	0	23	28 + 6N (n=0,1,2,…)	335	340 + 6N (n=0,1,2,…)
1	0	1	23	28 + 6N (n=0,1,2,…)	336	341+ 6N (n=0,1,2,…)
1	1	0	24	29 + 6N (n=0,1,2,…)	336	340 + 6N (n=0,1,2,…)
1	1	1	23	28 + 6N (n=0,1,2,…)	337	342 + 6N (n=0,1,2,…)

Digital PLL

The digital PLL will lock to the horizontal frequency of the incoming video so as to generate pixel clock. The timing generator provides all the timing signals to the display. When there is unstable horizontal frequency of the incoming video, the DPLL will be reset and try to lock it again. The PLL will be reset when the unstable condition persists for more than 2 frames (40 ms).

Application Example Circuit





Hiros Connector 15FLZ-SM1-TB
Or Equivalent to
Cyber Display 320 Model 300