

FAN8402D (KA3081D)

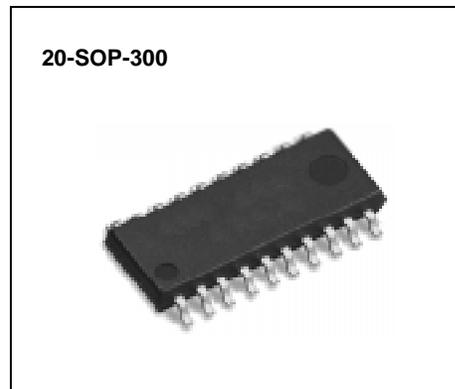
3-Phase BLDC Motor Driver

Features

- Commutation FG, PG is executed by 1-hall
- Soft switching at output terminal reduces switching impulse.
- 3-phase full wave BLDC motor driver.
- Voltage reference (Uses band gap circuit)
- Built-in thermal shut-down (TSD) circuit

Description

FAN8402D is a bipolar integrated circuit used to drive 3-phase brushless DC motor in full wave mode using 1-hall sensor. FAN8402D uses 1-hall for commutation and PG generation. It is a special circuit for soft switching using 1-hall reduces the EMI and eliminates snubber. The FG is generated by BEMF.



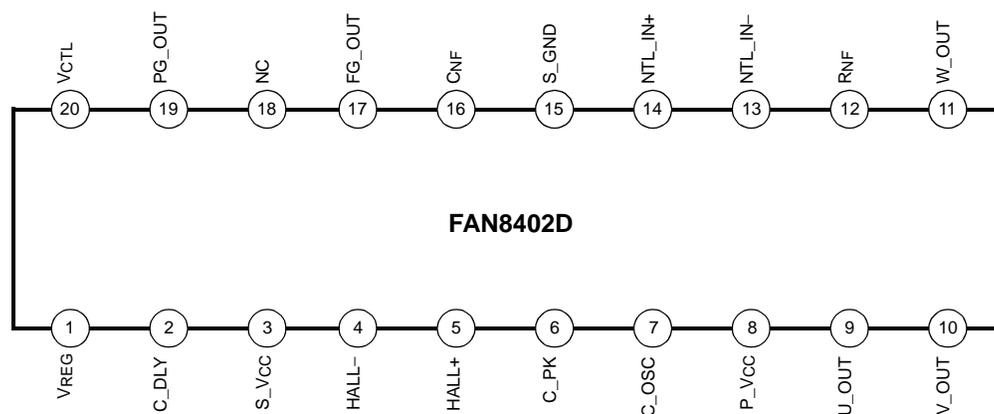
Typical Applications

- Video Cassette recorder (VCR) cylinder (drum) motor
- Other 3-phase BLDC motor

Ordering Information

Device	Package	Operating Temp.
FAN8402D	20-SOP-300	-25°C ~ +75°C
FAN8402DTF	20-SOP-300	-25°C ~ +75°C

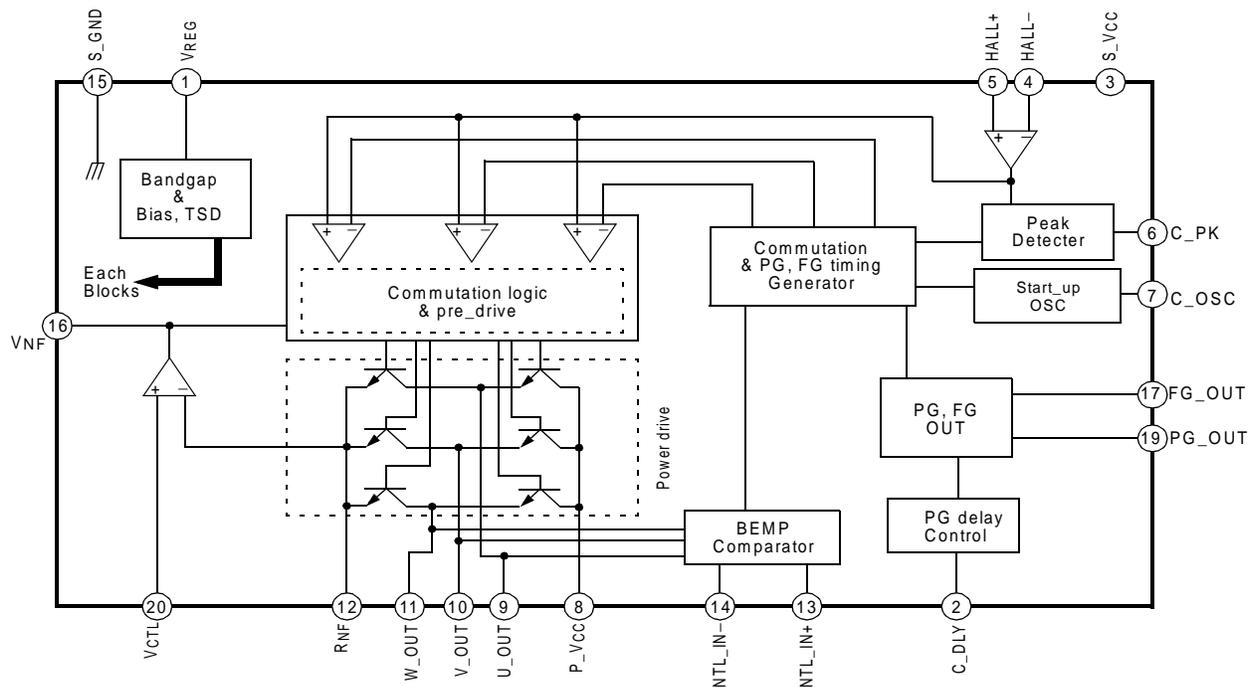
Pin Assignments



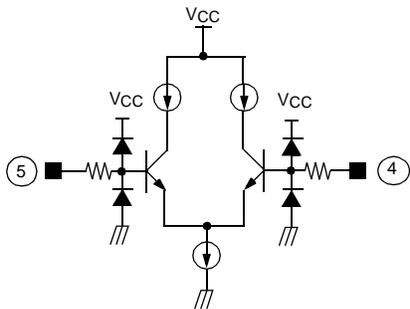
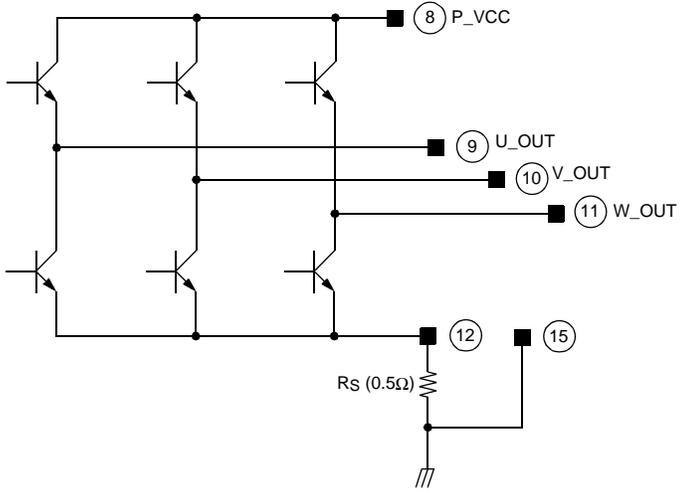
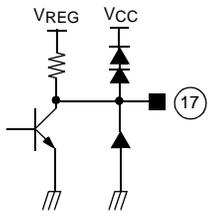
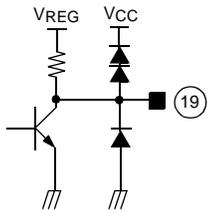
Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	VREG	Regurator output
2	C_DLY	PG. delay
3	S_VCC	Signal VCC
4	HALL-	Hall- input
5	HALL+	Hall+ input
6	C_PK	Peak detector of hall signal
7	C_OSC	Start-up oscillator
8	P_VCC	Power VCC
9	U_OUT	U-phase output
10	V_OUT	V-phase output
11	W_OUT	W-phase output
12	RNF	Output current sensing
13	NTL_IN-	Input from the neutral point of the motor coils.
14	NTL_IN+	Input from the neutral point of the motor coils.
15	S_GND	Signal ground
16	CNF	Phase compensation
17	FG_OUT	FG. output
18	NC	-
19	PG_OUT	PG. output
20	VCTL	Output current control

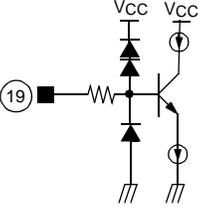
Internal Block Diagram



Equivalent Circuits

Description	Pin No.	Internal circuit
Hall input	5,4	
Output & Current detection	9,10,11 8,12	
FG Output	17	
PG Output	19	

Equivalent Circuits (Continued)

Description	Pin No.	Internal circuit
Voltage control reference	20	 <p>The diagram shows the internal circuit for pin 20. It consists of a resistor connected to pin 19. This resistor is connected to the base of a transistor. The emitter of the transistor is connected to ground. The collector of the transistor is connected to a diode, which is in turn connected to a VCC supply. There is also a diode connected from the VCC supply to the base of the transistor. A second VCC supply is shown connected to the collector of the transistor.</p>

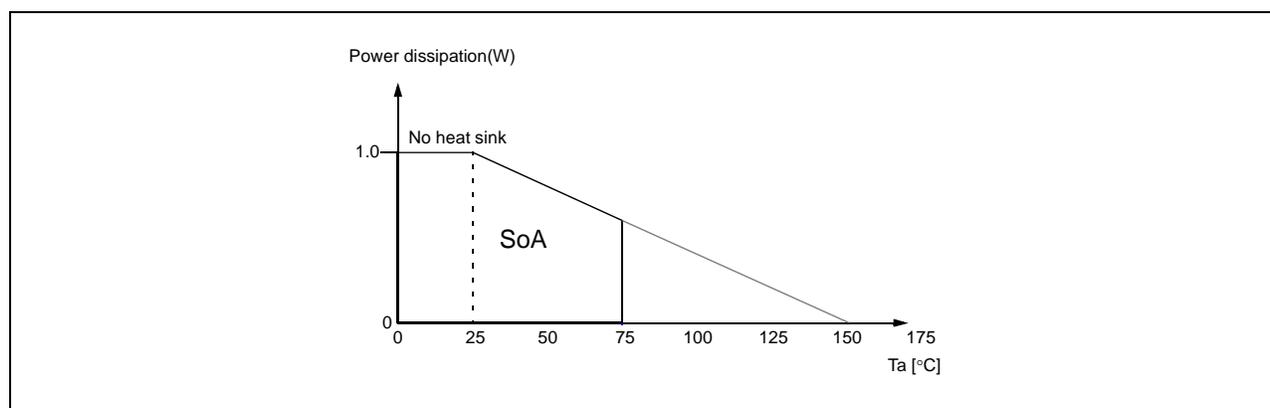
Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Value	Unit	Remark
Supply voltage (Signal)	VCCmax	20	V	-
Maxium Output current	I _{Omax}	1.0 ^{note1}	A / Phase	
Regulator output current	I _{REGmax}	10	mA	
Power dissipation	P _d	1.0 ^{note2}	W	No heat sink
Junction temperature	T _J	150	°C	-
Operating temperature	T _{OPR}	-20 ~ +75	°C	Ambient temperature (Ta)
Storage temperature	T _{STG}	-40 ~ +155	°C	

NOTES:

- Duty 1 / 100, pulse width 500μs
- 1) When mounted on glass epoxy PCB (76.2 × 114 × 1.57mm)
2) Power dissipation reduces 9.6mW / °C for using above Ta=25°C.
3) Do not exceed P_d and SOA(Safe Operating Area).

Power Dissipation Curve



Recommened Operating Conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max	Unit
Operating supply voltage(Signal)	S_VCC	4.5	5.0	5.5	V
Operating supply voltage(Power)	P_VCC	8	12	18	V

Electrical Characteristics

(Measured in test circuit, P_VCC=12V, Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	max.	Unit
TOTAL						
Supply voltage	VCC	-	8.0	-	18	V
Supply current (1)	ICC1	P_VCC=12V, VREG=open, VCTL=0V	-	11.2	17	mA
Supply current (2)	ICC2	P_VCC=12V, VREG=open, VCTL=0V	-	11.5	17	mA
REGULATOR						
VREG output voltage (2)	VREG2	P_VCC=12V, IREG=0mA	4.7	5.0	5.3	V
VREG output voltage (5)	VREG5	P_VCC=12V, IREG=10mA	4.7	5.0	5.3	V
START-UP OSCILLATOR						
C_OSC operation frequency	OSC_FEQ	C_OSC=47nF	6	8	10	Hz
C_OSC charging current	OSC_ICH	C_OSC=47nF	-0.5	-2	-3.5	μA
C_OSC discharging current	OSC_IDC	C_OSC=47nF	1	3	5	μA
C_OSC low threshold voltage	OSC_THL	C_OSC=47nF	0.2	0.5	0.8	V
C_OSC high threshold voltage	OSC_THH	C_OSC=47nF	2.7	3.0	3.3	V
VOLTAGE CONTROL						
VCTL start voltage	VCTL_ST	VCTL=0~2V When IO=25mA	1.01	1.26	1.51	V
VCTL input voltage range	VCTL_IN	VREG	0	-	VREF	V
VCTL input bias current	VCTL_BI	VCTL=2.0V	-	1.0	1.5	μA
Gain	GM	RNF=0.47Ω, VCTL=0~2V	0.38	0.45	0.52	A
HALL INPUT						
Input hall signal Min. voltage ^{note}	VH_MIN		300	-	-	mVp-p
PG hall 1'st Min. voltage ^{note}	VH_P1		60	-	-	mVo-p
PG hall 2'nd Min. voltage ^{note}	VH_P2		55	-	-	mVo-p
PG hall 3'rd Min. voltage ^{note}	VH_P3		75	-	-	mVo-p
PG hall 1'st-2'nd level ^{note}	ΔVH		5	-	-	mVo-p
FG (FREQUENCY GENERATOR), PG (PHASE GENERATOR)						
FG, PG high level	FG_PG_H	-	4.5	-	-	V
FG, PG low level	FG_PG_L	-	-	-	0.5	V

Notes:

The note in the chart means items calculated and approved in design not the items proven by actual test results.

Electrical Characteristics (Continued)

(Measured in test circuit, P_VCC=12V, Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	max.	Unit
TSD						
Temp. threshold ^{note}	TSD_T	-	130	150	-	°C
Temp. hysteresis ^{note}	TSD_H	-	20	30	-	°C
OUTPUT						
Output saturation voltage (Upper)	V _{SU1}	V _{CTL} =4V, I _O =600mA, R _{NF} =0.47Ω, R _L =10Ω	-	1.0	1.5	V
Output saturation voltage (Under)	V _{SD1}		-	0.4	0.7	V
N _{TL} _IN- input voltage range	V _{N_{TL}_IN-}	-	0	-	V _{CC}	V
C _{NF} voltage	V _{CNF}	V _{CTL} =2V	1	-	-	V
C _{PK} frequency	CPK_FRQ	C _{PK} =100Ω + 0.1μF	0.8	1	1.2	kHz
C _{CK} voltage level	CPK_V	C _{PK} =100Ω + 0.1μF HALL- =0.25V	0.4	-	-	V _{p-p}
C_DLY						
C _{DLY} charging current	I _{C_DLY}	C _{DLY} =4nF	-20	-30	-40	μA

Notes:

The note in the chart means items calculated and approved in design not the items proven by actual test results.

Application Information

1. SYSTEM BLOCK DIAGRAM

The figure 1 shows concept of soft switching for 3-phase output with a hall sensor.

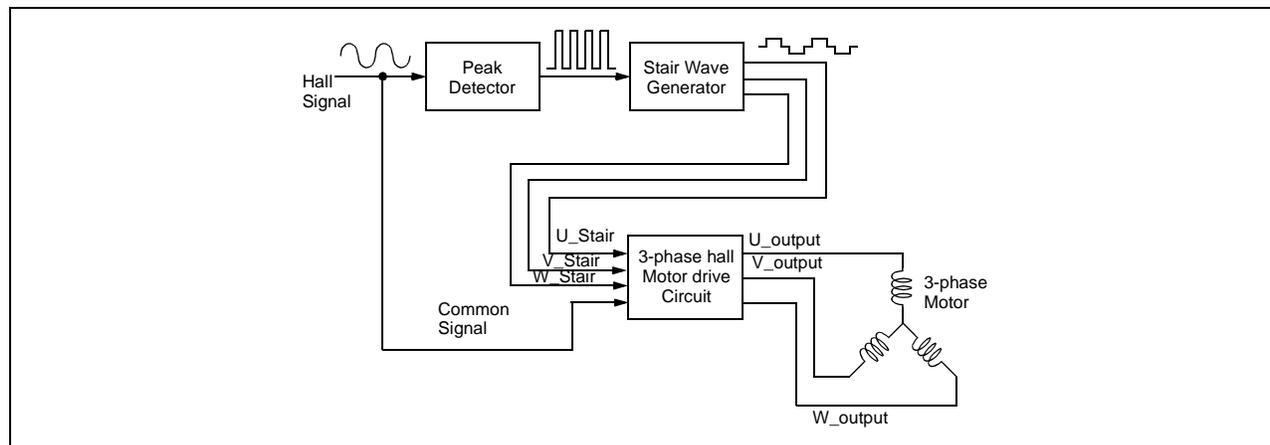


Figure 1.

- Peak detector
Generates clock pulses at the peak points of the hall signal.
- Stair wave generator
Generates 3 stair wave signals 120 degree apart from the clock pulses.
- 3-phase motor drive circuit
Controls output currents to operate 3-phase motor using the voltage difference between the 3 stair wave signals and FG hall signal.

2. STRUCTURE OF BLDC MOTOR

Consists of main and sub magnets. For every main magnet there are 3 submagnets as shown in Fig 2.

Sub-magnet takes hall signal and goes through 6 gradual filtering steps purifying in order to operate 3-phase motor with one hall sensor.

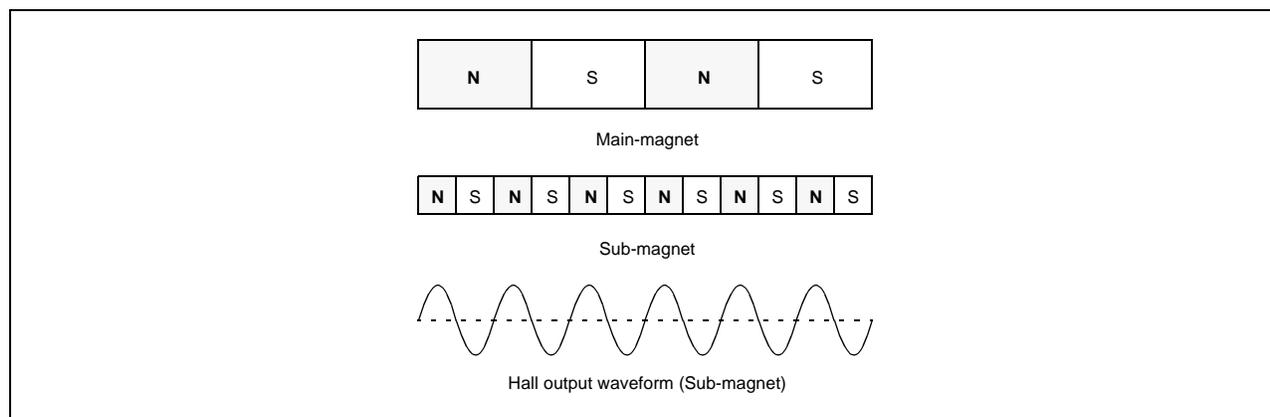


Figure 2.

3. PRINCIPLE OF OPERATION

Input circuit of 3-phase motor drive with soft-switching function is shown as the figure 3.

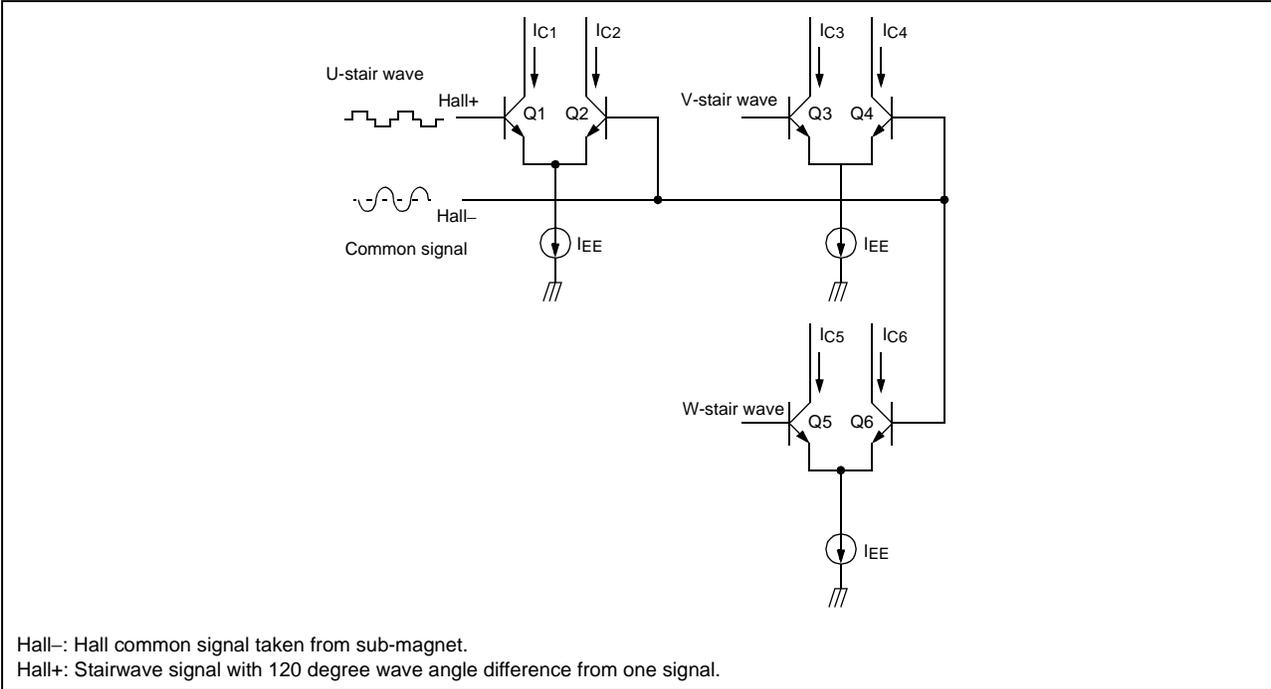


Figure 3.

Next the figure 4 shows common signal (Hall signal) and each individual stairwave at its own position.

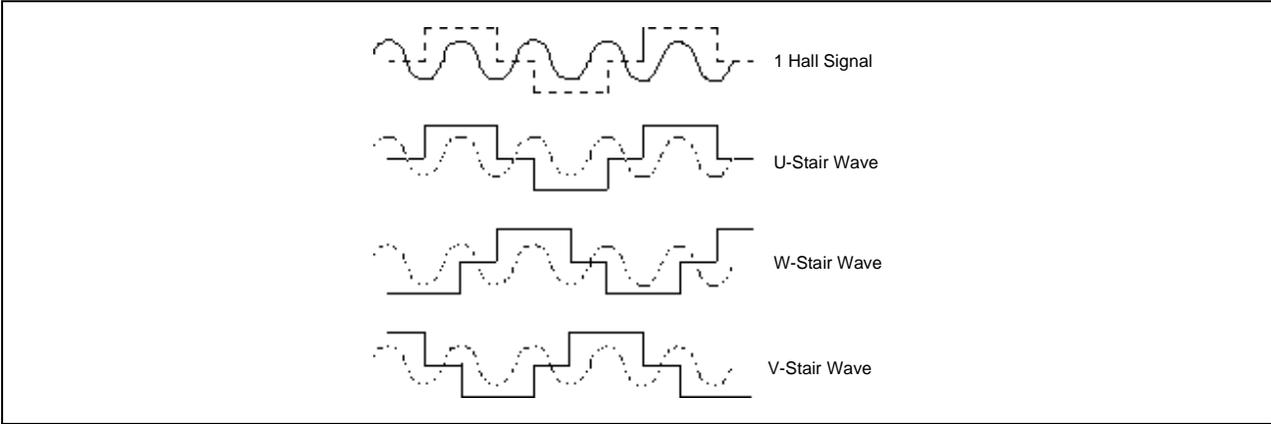


Figure 4.

Figure 5 shows hall signal and stairwave signal position. The section where the difference between hall signal and stairwave is within 100mV.

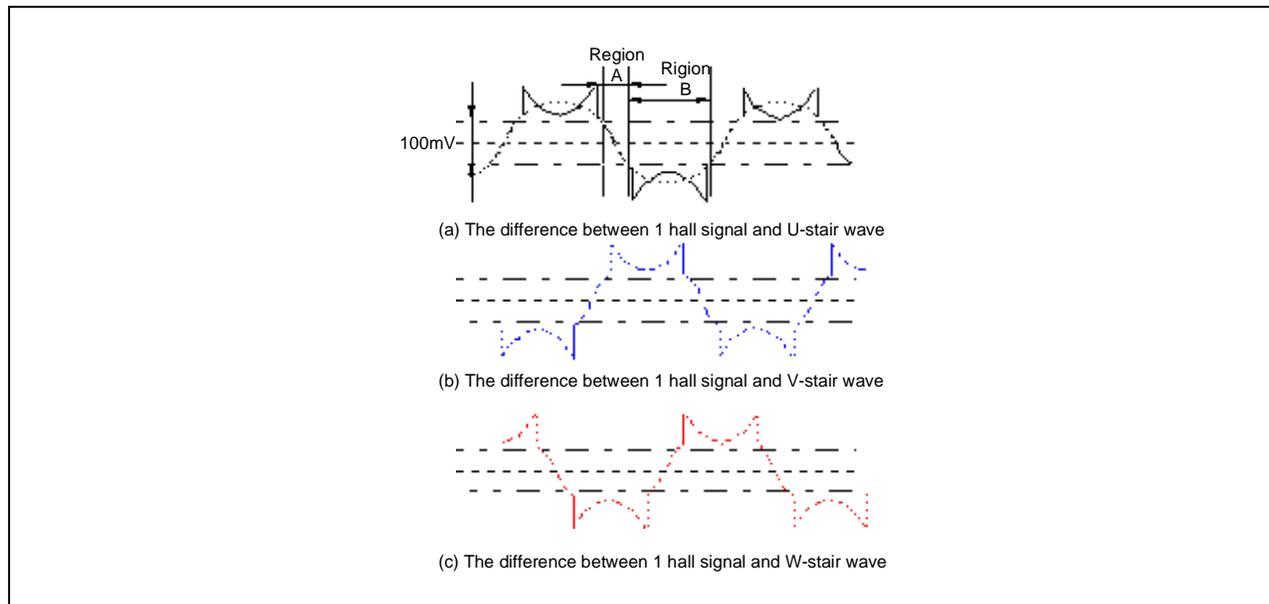


Figure 5.

4. PEAK DETECTOR

Hall signals and stairwave signals made from peak detectors's output rotate the motor.
The peak detector circuit is shown in Fig 6.

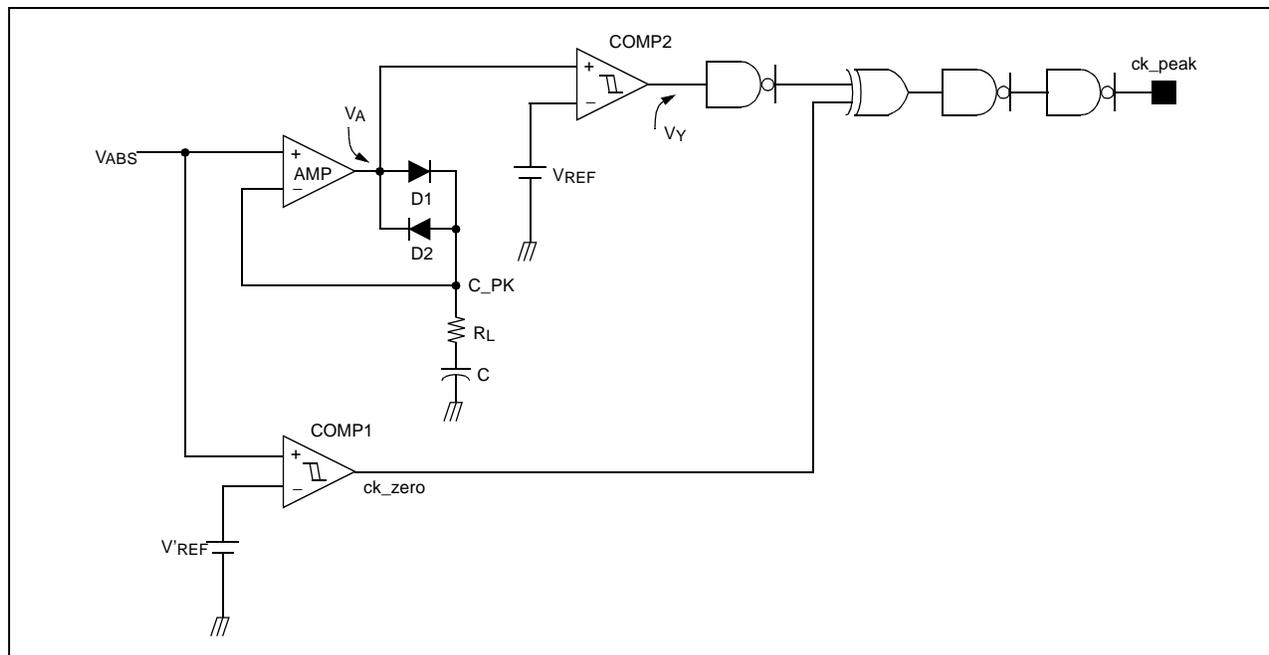


Figure 6.

VABS in the figure 6 is a signal from twice amplified hall signal and hall bias at 2.5 volt as standard voltage as you see in the figure 7.

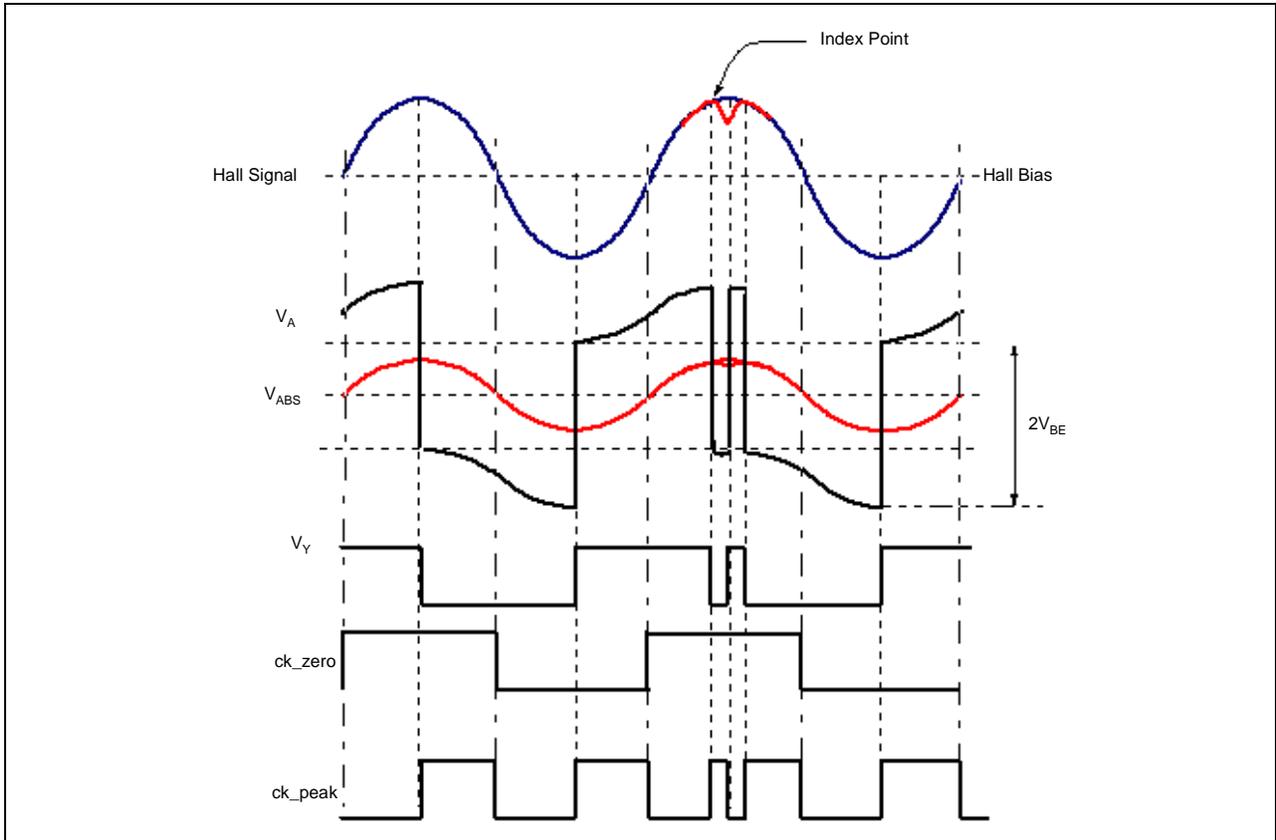


Figure 7.

5. DRIVE OUTPUT

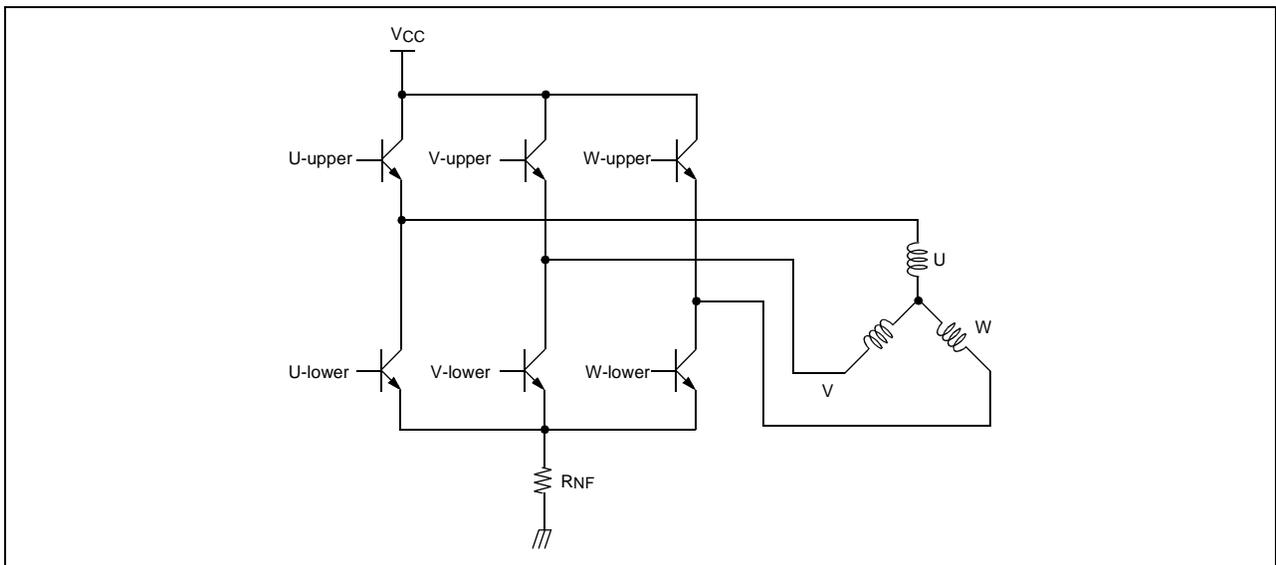


Figure 8.

The figure 8 shows the 3-phases of the BLDC motor.

The upper power TRs in output group operate in linear area and the lower group work in saturation area.

6. VOLTAGE CONTROL & CURRENT SENSING

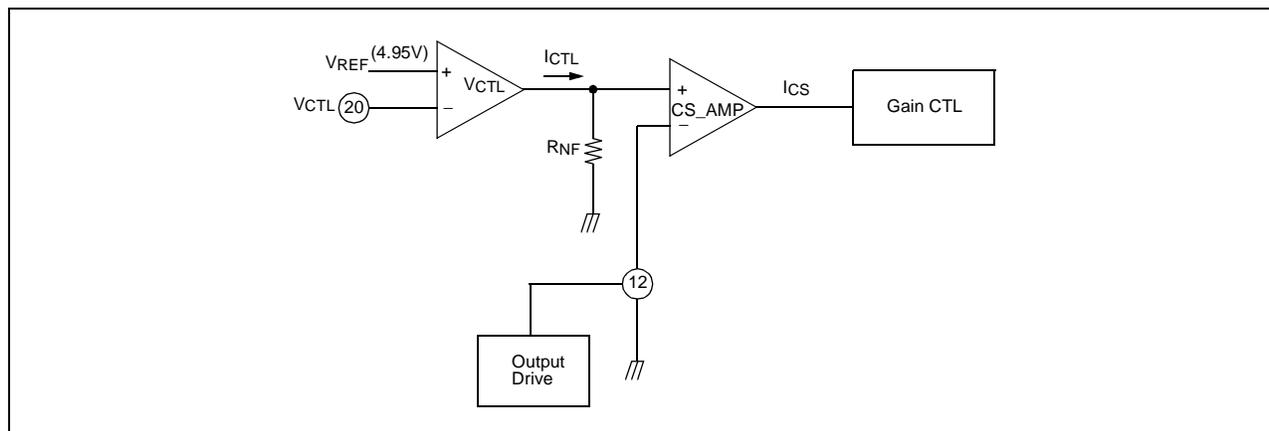


Figure 9.

The circuit in the figure 9 outputs I_{CTL} current when V_{CTL} (Control voltage from servo) is larger than the value of V_{REF} . The V-I characteristic of this circuit is shown in the figure 10.

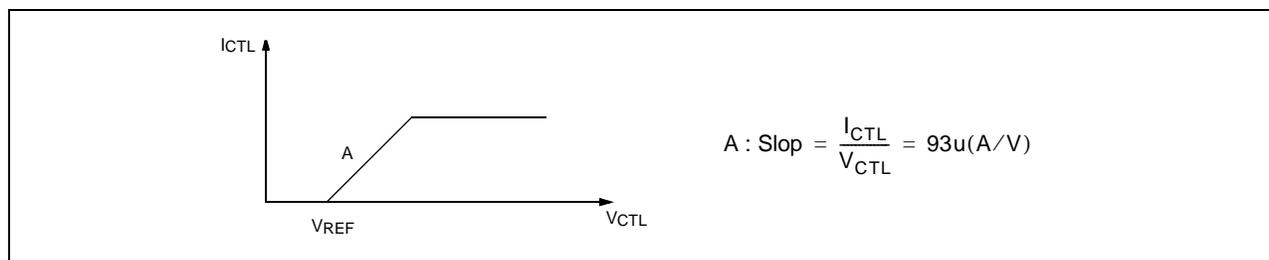
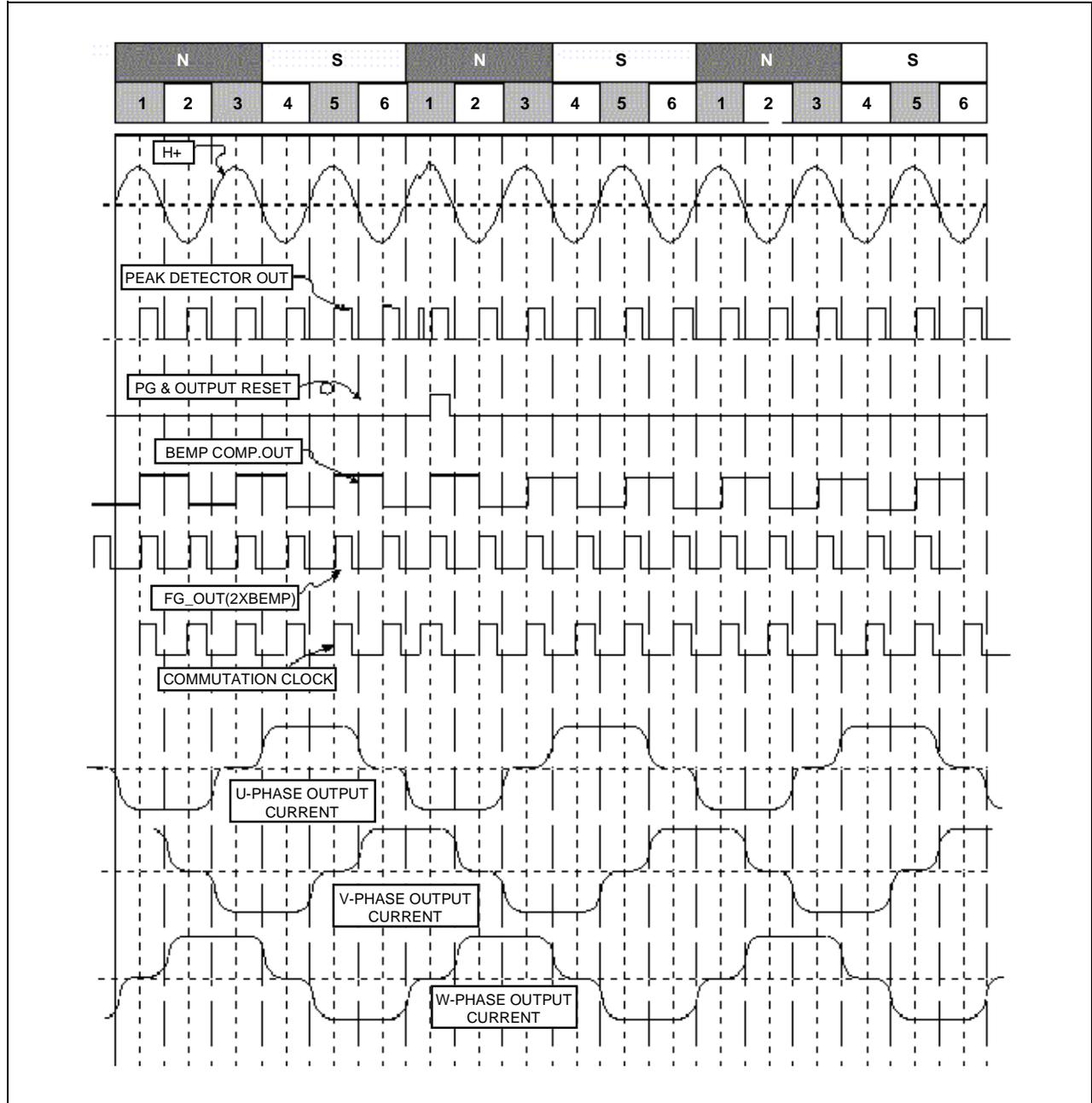


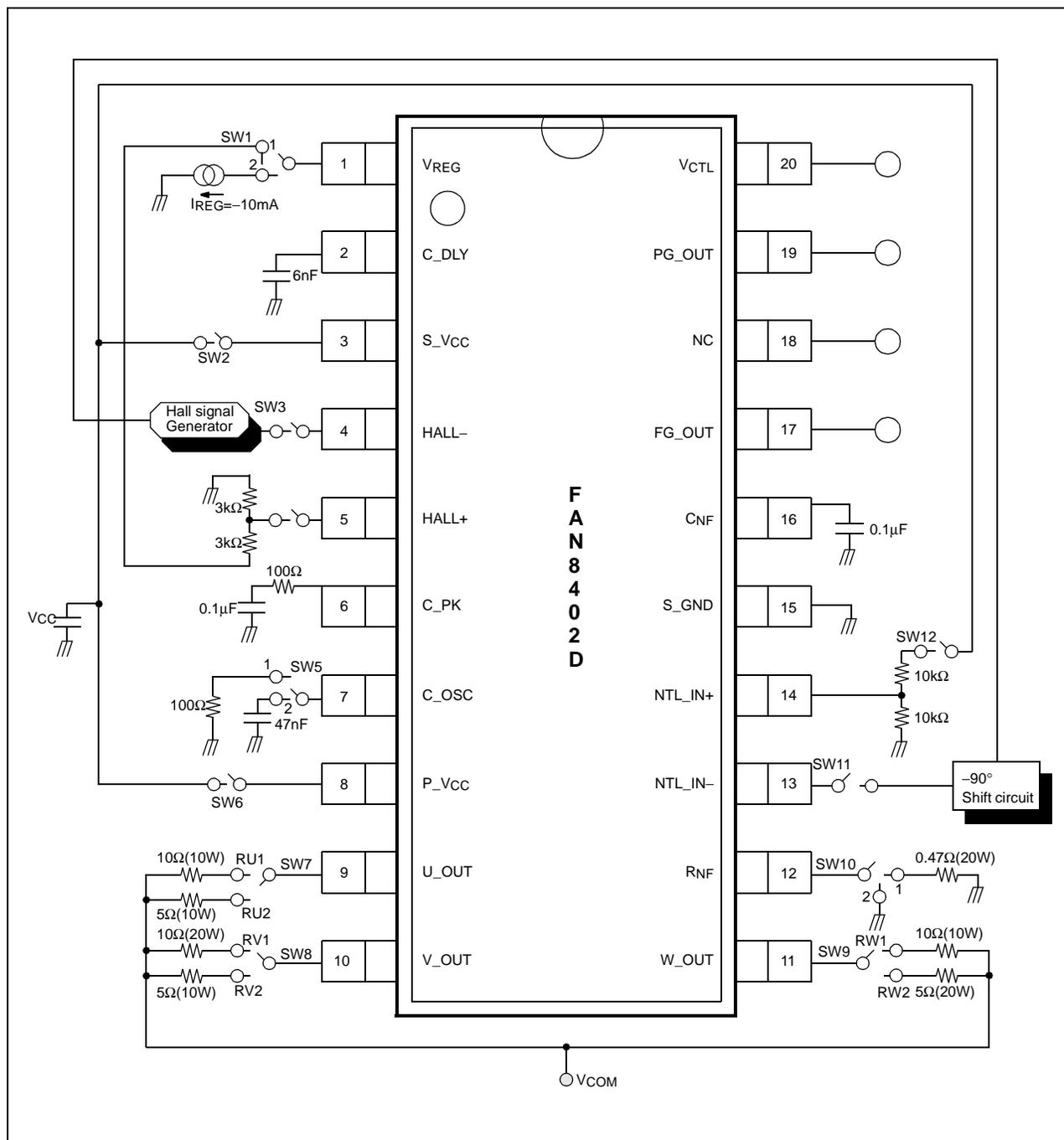
Figure 10.

The CS-AMP terminal amplifies by getting inputs from output terminal getting I_{CTL} and R_{NF} voltages. R_{NF} resistance feedbacks the current in output terminal.

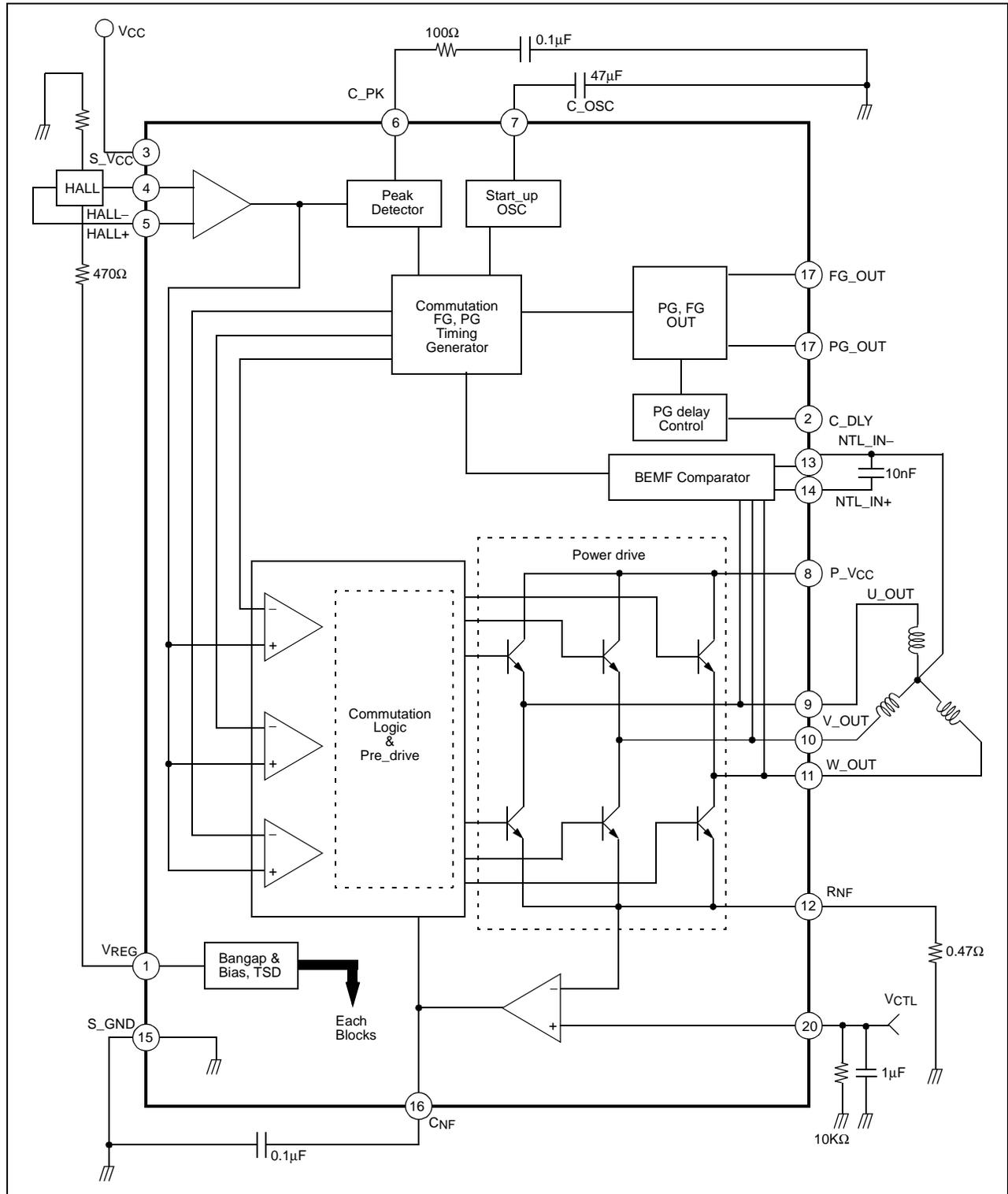
Timing Chart



Test Circuits



Typical Application Circuits



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