



HV02

T-52-13-05

16-Channel Matrix TFEL Panel Display Row Driver

Ordering Information

Device	Package Options					
	40-Pin Ceramic DIP	36-Pin Leadless Chip Carrier	36-Pin Leaded Chip Carrier Flat Leads	36-Pin Leaded Chip Carrier Std. Bent Leads	36-Pin Leaded Chip Carrier Reverse Bent Leads	Die
HV02	HV02C	HV02LC	HV02CF	HV02CS	HV02CR	HV02X

Features

- ☐ HVCMOS® Technology
- ☐ Up to 200V output voltage
- ☐ Can drive up to 1000 lines
- ☐ 250mA surge current sink capability
- ☐ TYP R_{ON} of 25 ohms
- ☐ High performance – up to 200 KHz scan rate
- ☐ Integrated high voltage DMOS and CMOS technology
- ☐ Available in 40-pin DIP, 36 Pin Ceramic Chip Carrier and Leaded Chip Carrier packages

Absolute Maximum Ratings

Low Voltage Supply V_{DD}	-0.5V to 14V
BV_{DS} Driver output transistor voltage	-0.5V to 250V
Total Drive Current (Unison Mode) I_{OLU}	1.6 AMP
Logic Input Voltage	-0.5V to $V_{DD} + 0.5V$
Storage Temperature	-65°C to 150°C
Power Dissipation ¹	1.6 Watt

Note 1: For operation above 25°C ambient derate linearly to 85°C at 15mW/°C.

General Description

The HV02 is a 16 Channel Row Drive IC designed for general purpose electroluminescent display use. The chip provides the scanning voltage to each row output in sequence and, in unison, generates the refresh pulse and two sinking pulses (scan and refresh sink) which are required for the operation of the TFEL panel. The intrinsic source-drain diodes on the outputs can handle surge currents up to 250mA for charging of the capacitive loads.

Serial Data is entered into a 16-bit shift register on the Hi to Low transition of the clock input. Data is outputted if enable is Hi and the "ALL ON" input is Low. If the "ALL ON" input goes Hi, all parallel outputs turn on in unison to refresh the Row lines on the panel. Expansion is possible by using the serial output (data out). This output is not controlled by the enable and "ALL ON" inputs. To make the system design versatile, the HV02 has an initialization feature which allows setting or resetting the first bit and resetting the other bits of the shift register.

Electrical Characteristics (over recommended operating conditions unless noted)

T-52-13-05

DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}	Input High Voltage	$V_{DD} - 1$			V	
V_{IL}	Input Low Voltage		1		V	
I_{DD}	V_{DD} Supply Current		1	6.5	mA	$V_{DD} = 13V, f_{SC} = 100KHz$
I_{OLH}	High Voltage Output Sink Current (Single Driver)	250	300		mA	$V_{DD} = 10.8V$ $V_O = 15V$
I_{IL}, I_{IH}	Input Leakage Current		± 1	± 50	μA	$V_{IN} = 0V$ or V_{DD}
R_{ON}	Output driver transistor On-resistance		25	60	Ω	$V_{DD} = 10.8V$
BV_{DS}	Output driver transistor Drain-Source Breakdown voltage	200	250		V	High Voltage Outputs Off $I_O = 200\mu A$
I_{OL}	Shift Register Data Out Source Current	50			μA	$V_{DD} = 10.8V$ $V_{OL} = 1.0V$
I_{OH}	Shift Register Data Out Source Current	-50			μA	$V_{DD} = 10.8$ $V_{OH} = V_{DD} - 1.0V$

AC Characteristics ($V_{DD} = 12V, T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_C	Max shift Clock Frequency	6	10		MHz	$V_{DD} = 10V$
S_R	Driver Ground Slew Rate			50	V/ μsec	

Recommended Operating Conditions

Parameter	Value
Low Voltage Supply V_{DD}	10.8V to 13.2V
Driver output transistor voltage	up to 200V
Logic Input Voltage	0V to V_{DD}
Operating Temperature (T_A)	-40°C to 85°C

Operation of the Row Driver

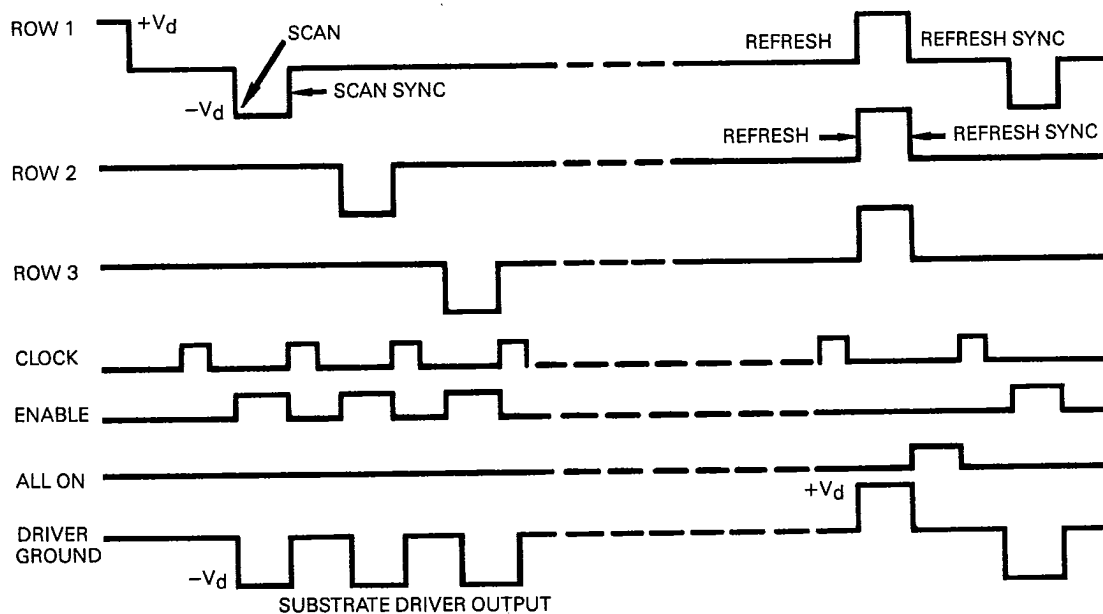
The operation of the row driver can be understood by looking at the Logic Diagram and Output Waveform states. In normal operation, a row driver selects out a single line on the electroluminescent panel by pulling it down to a negative voltage ($-V_d$). This selection is called scan. Since the EL panel has a large capacitance that was charged, eventually it has to be discharged. This operation is called refresh, and is performed by connecting these to a positive voltage ($+V_d$).

The driver ground (DR GND) is not tied to the system ground, but rather is a floating node. It is connected to the substrate driver, whose output varies as shown on the Waveform Diagram. The combination of the Row Drivers and the Substrate Drivers gives the required four functions which are called scan, scan sync, refresh and refresh sync. The first mode of the scan must be applied individually since it is by definition a single line selection. The refresh sync on the other hand, must be applied in unison. The other two modes, scan sync and refresh, can be applied either way according to the designer's discretion.

Serial data is entered into the registers on the Hi to Lo transition of the clock input. Normal operation calls for a single logic "high" to be clocked through the shift register via the serial output. To create a scan function, the enable must be pulsed at each time. For the refresh sync mode, the ALL ON input must be high, since this function has to be done in unison for all row lines.

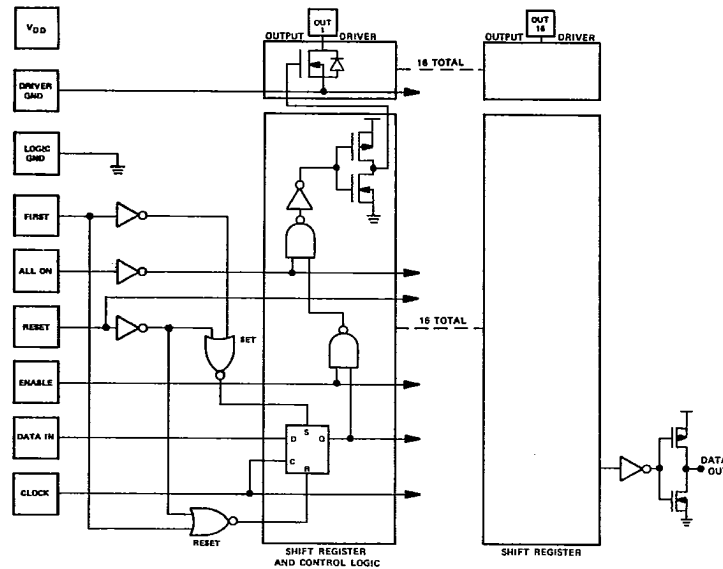
The Row Driver was designed with an added feature of a mode control input. The flip-flops of the shift registers are made with a reset control. By pulling the "RESET" input high, they will be reset to zero with the exception of the first. This stage can be high or low during the reset depending on the control input called "First." If this input is high, the "RESET" command will be interpreted as a "SET" command for the first flip-flop. This feature is important in the normal scanning function when a group of these row drivers are interconnected to form a long string of shift registers. By utilizing this function, a single "ONE" can be placed into any of the selected chips, and the row drivers in the system can be initialized in a very flexible way.

Switching Waveforms



Logic Diagram

T-52-13-05



Function Table

Function	Control Inputs					Internal Shift Registers		Outputs	
	First	Reset	Clock	Enable	All On	1	2-16	Serial Output	1-16 Parallel
First	H	H	X	X	X	Set to "1"	RESET to "0"	"0"	Determined by Enable and ALL ON
Reset	L	H	X	X	X	Reset to "0"		"0"	Determined by ALL ON
Load Data/Shift	X	L	↓	X	X	LOAD & SHIFT		R 16	Determined by ENABLE and ALL ON
Output Enable	X	L	X	H	L	X		R 16	Determined by R ₁ through R ₁₆
Output Disable	X	X	X	L	L	As determined above		R 16	All Parallel Outputs "OFF"
All On	X	X	X	X	H	As determined above		R 16	All Parallel Outputs are "ON"

L = Low level, H = High level, X = Irrelevant, ↓ = Hi to Low Transition, R 16 = State of register 16, R₁ = State of Register 1.

Pin Configurations

T-52-13-05

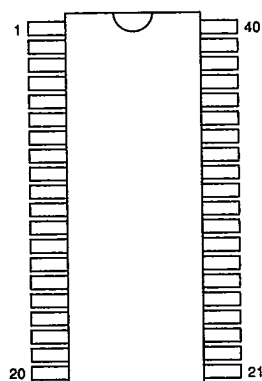
40-Pin DIP

Pin	Function	Pin	Function
1	N/C	21	HVout 8
2	All On	22	HVout 7
3	Enable	23	HVout 6
4	N/C	24	HVout 5
5	Data Out	25	N/C
6	L GND	26	N/C
7	DR GND	27	N/C
8	HVout 16	28	HVout 4
9	HVout 15	29	HVout 3
10	N/C	30	N/C
11	N/C	31	N/C
12	HVout 14	32	HVout 2
13	HVout 13	33	HVout 1
14	N/C	34	DR GND
15	N/C	35	L GND
16	N/C	36	Data In
17	HVout 12	37	Clock
18	HVout 11	38	Reset
19	HVout 10	39	V _{DD}
20	HVout 9	40	First

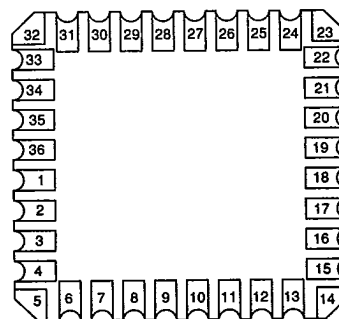
36-Pin LCC

Pin	Function	Pin	Function
1	First	19	HVout 8
2	All On	20	HVout 7
3	Enable	21	HVout 6
4	Data Out	22	HVout 5
5	L GND	23	N/C
6	DR GND	24	N/C
7	HVout 16	25	N/C
8	HVout 15	26	N/C
9	HVout 14	27	HVout 4
10	HVout 13	28	HVout 3
11	N/C	29	HVout 2
12	N/C	30	HVout 1
13	N/C	31	DR GND
14	N/C	32	L GND
15	HVout 12	33	Data In
16	HVout 11	34	Clock
17	HVout 10	35	Reset
18	HVout 9	36	V _{DD}

Package Outlines



top view
40-pin DIP



top view
36-pin LCC