

LZ2324AK

1/3 type B/W CCD Area Sensor for CCIR

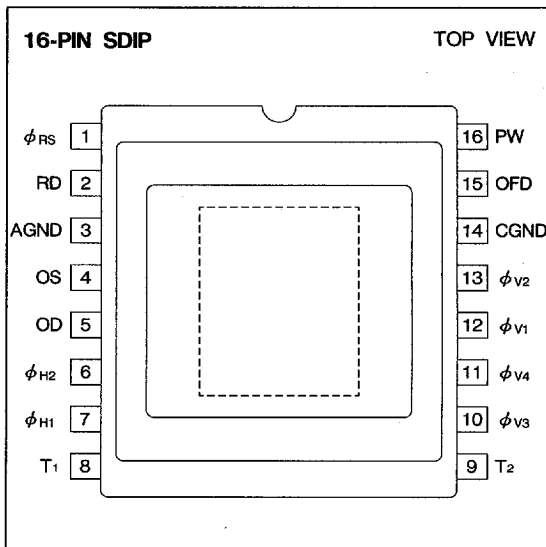
DESCRIPTION

LZ2324AK is a 1/3-type (6.0 mm) solid-state image sensor that consists of PN photo-diodes and CCDs (charge-coupled devices). Having approximately 0800 pixels (horizontal 542 × vertical 582), the sensor provides a high resolution stable B/W image.

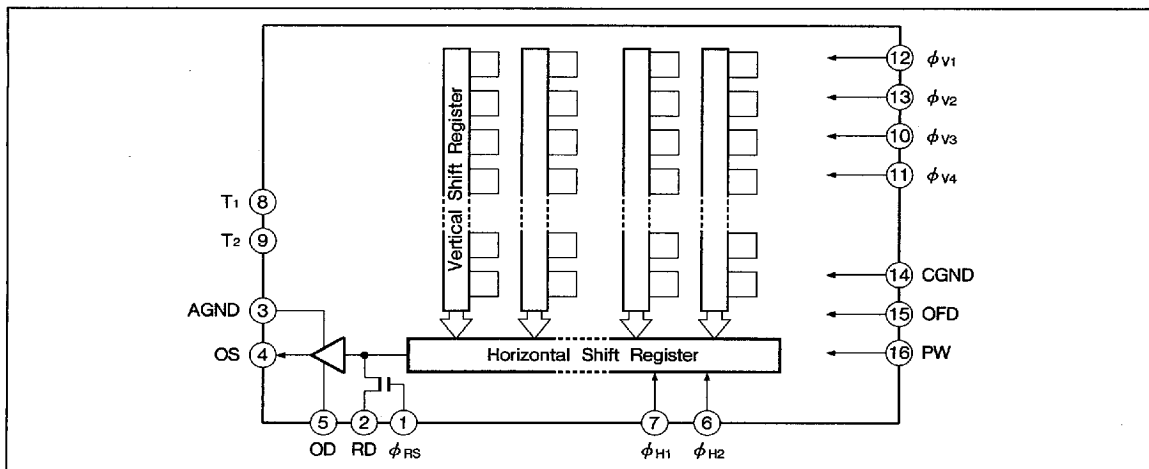
FEATURES

- Number of pixels : 512 (H) × 582 (V)
Pixel pitch : 9.6 μm (H) × 6.3 μm (V)
Number of optical black pixels
: Horizontal; front 2 and rear 28
- Low fixed pattern noise and lag
- No sticking and no image distortion
- Blooming suppression structure
- Built-in output amplifier
- Variable electronic shutter (1/50 to 1/10 000 s)
- Compatible with CCIR standard
- Package : 16-pin SDIP [CERDIP] (WDIP016-N-0500C)

PIN CONNECTIONS



BLOCK DIAGRAM



8180798 0013689 976

PIN DESCRIPTION

SYMBOL	PIN NAME
RD	Reset transistor drain
OD	Output transistor drain
OS	Video output
ϕ_{RS}	Reset transistor gate clock
$\phi_{V1}, \phi_{V2}, \phi_{V3}, \phi_{V4}$	Vertical shift register gate clock
ϕ_{H1}, ϕ_{H2}	Horizontal shift register gate clock
OFD	Overflow drain
PW	P type well
AGND	Analog part ground
CGND	Clock part ground
T1, T2	Test terminal

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

PARAMETER	SYMBOL	RATING	UNIT
Output transistor drain voltage	V _{OD}	0 to +18	V
Reset transistor drain voltage	V _{RD}	0 to +18	V
Overflow drain voltage	V _{OFD}	0 to +55	V
Test terminal, T1	V _{T1}	0 to +18	V
Test terminal, T2	V _{T2}	-0.3 to +18	V
Reset gate clock voltage	V ϕ_{RS}	-0.3 to +18	V
Vertical shift register clock voltage	V ϕ_V	-9.0 to +18	V
Horizontal shift register clock voltage	V ϕ_H	-0.3 to +18	V
Voltage difference between PW and vertical clock	V _{PW} - V ϕ_V	-27 to 0	V
Storage temperature	T _{stg}	-20 to +80	°C
Operating ambient temperature	T _{opr}	-20 to +70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Operating ambient temperature		T _{opr}		25.0		°C	
Output transistor drain voltage		V _{OD}	14.5	15.0	16.0	V	
Reset transistor drain voltage		V _{RD}		V _{OD}		V	
Overflow drain voltage	When DC is applied	V _{OFD}	5.0		19.0	V	1
	When pulse is applied p-p level	V _{φ OFD}	22.0			V	2
Analog part ground		AGND		0.0		V	
Clock part ground		CGND		0.0		V	
P-well voltage		V _{PW}	-9.0		V _{φ VL}	V	
Test terminal, T ₁		V _{T1}		V _{OD}		V	
Test terminal, T ₂		V _{T2}		0.0		V	
Vertical shift register clock	LOW level	V _{φ V1L} , V _{φ V2L} V _{φ V3L} , V _{φ V4L}	-8.5	-8.0	-7.5	V	
	INTERMEDIATE level	V _{φ V1I} , V _{φ V2I} V _{φ V3I} , V _{φ V4I}		0.0		V	
	HIGH level	V _{φ V1H} , V _{φ V3H}	16.0	16.5	17.0	V	
Horizontal shift register clock	LOW level	V _{φ H1L} , V _{φ H2L}	-0.05	0.0	0.05	V	
	HIGH level	V _{φ H1H} , V _{φ H2H}	4.7	5.0	6.0	V	
Reset gate clock	LOW level	V _{φ RSL}	0.0		V _{RD} -12.0	V	
	HIGH level	V _{φ RSH}	V _{RD} -7.5		9.5	V	
Vertical shift register clock frequency		f _{φ V1} , f _{φ V2} f _{φ V3} , f _{φ V4}		15.63		kHz	
Horizontal shift register clock frequency		f _{φ H1} , f _{φ H2}		9.66		MHz	
Reset gate clock frequency		f _{φ RS}		9.66		MHz	

NOTES :

1. When DC voltage is applied, shutter speed is 1/50 seconds.
2. When pulse is applied, shutter speed is less than 1/50 seconds.

ELECTRICAL CHARACTERISTICS (Drive method : Field Accumulation)

(T=25°C, Operating conditions : typical values for the recommended operating conditions, Color temperature of light source : 3200 K / IR cut-off filter (CM-500, 1 mm))

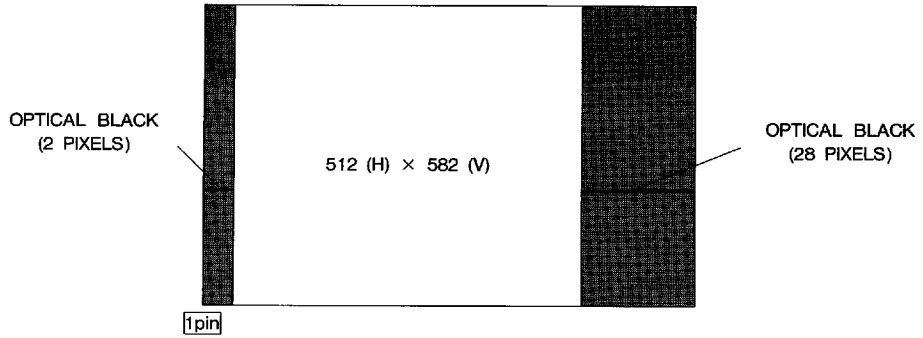
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Photo response non-uniformity	PRNU			10	%	2
Saturation signal	Vsat	550			mV	3
Saturation non-uniformity	SSUN			20	%	4
Dark output voltage	Vdark		0.3	3.0	mV	1, 5
Dark signal non-uniformity	DSNU		0.6	2.0	mV	1, 6
Sensitivity	R	360	500		mV	7
Gamma	γ		1			
Smear ratio	SMR		0.009	0.016	%	8
Image lag	AI			1.0	%	9
Blooming suppression ratio	ABL	1000				10
Output transistor drain current	I _{od}		4.0	8.0	mA	
Output impedance	R _o		300		Ω	
Dark noise	Vnoise		0.2	0.4	mV	11
OB difference in level				1.0	mV	12

- The standard output voltage is defined as 150 mV by the average output voltage under uniform illumination.
- The standard exposure level is defined when the average output voltage is 150 mV under uniform illumination.

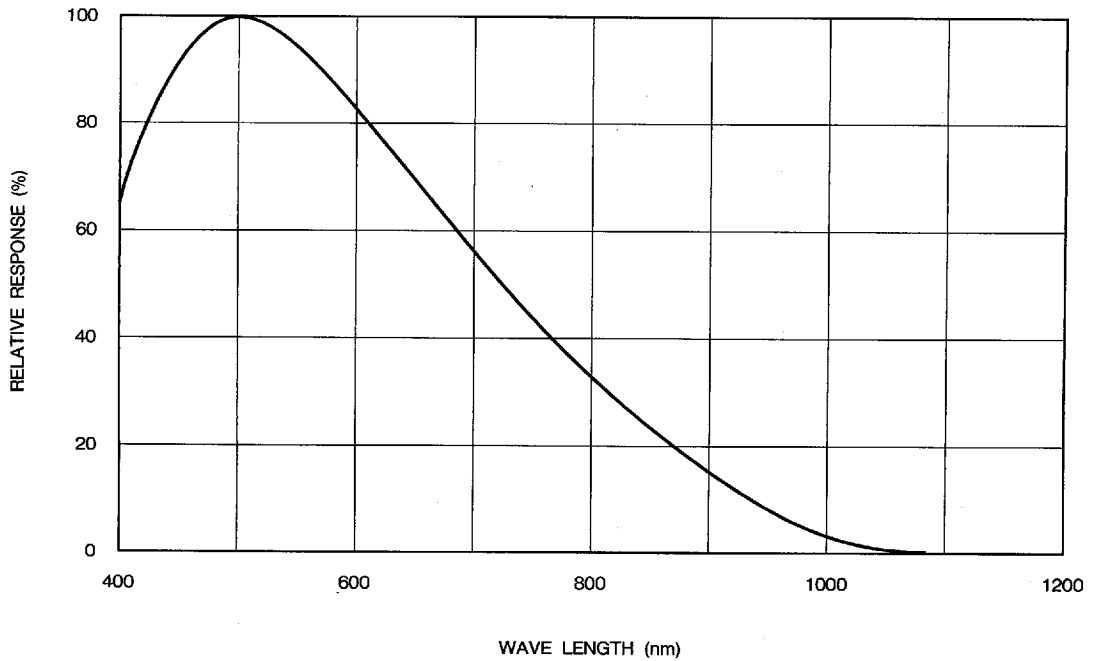
NOTES :

1. Ta : +60°C
2. The image area is divided into 10×10 segments. The segment's voltage is the average output voltage of all the pixels within the segment. PRNU is defined by $(V_{\max} - V_{\min})/V_o$, where V_{\max} and V_{\min} are the maximum and the minimum values of each segment's voltage respectively, when the average output voltage V_o is 150 mV.
3. The image area is divided into 10×10 segments.
The saturation signal is defined as the minimum of each segment's voltage which is the average output voltage of all the pixels within the segment, when the exposure level is set as 10 times, compared to standard level.
4. The image area is divided into 10×10 segments. The voltage of a segment is the saturation signal (V_s), when the exposure level is set as 10 times, compared to standard level. SSUN is defined by $(V_{\max} - V_{\min})/V_s$, when V_{\max} and V_{\min} are the maximum and minimum values of each segment's voltage respectively.
5. The average output voltage under a non-exposure condition.
6. The image area is divided into 10×10 segments. DSNU is defined by $(V_{\max} - V_{\min})$ under the non-exposure condition where V_{\max} and V_{\min} are the maximum and the minimum values of each segment's voltage, respectively, that is the average output voltage over all pixels in the segment.
7. The average output voltage when a 1000 lux light source attached with a 90% reflector is imaged by a lens of F4, f50 mm.
8. The sensor is adjusted to position a V/10 square at the center of image area where V is the vertical length of the image area. SMR is defined by the ratio of the output voltage detected during the vertical blanking period to the maximum of the pixel voltage in the V/10 square.
9. The sensor is exposed at the exposure level corresponding to the standard condition preceding non-exposure condition. AI is defined by the ratio between the output voltage measured at the 1st field during the non-exposure period and the standard output voltage.
10. The sensor is adjusted to position a V/10 square at the center of image area. ABL is the ratio between the exposure at the standard condition and the exposure at a point where a blooming is observed.
11. The RMS value of the dark noise (after CDS). The bandwidth range is from 100 kHz to 5.0 MHz.
12. The difference between the average output voltage of the effective area and the OB part under the non-exposure condition.

PIXEL STRUCTURE



SPECTRAL RESPONSE EXAMPLE

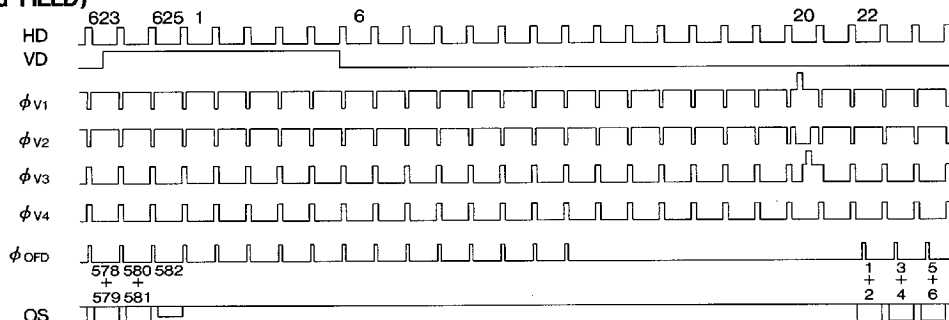


TIMING DIAGRAM EXAMPLE

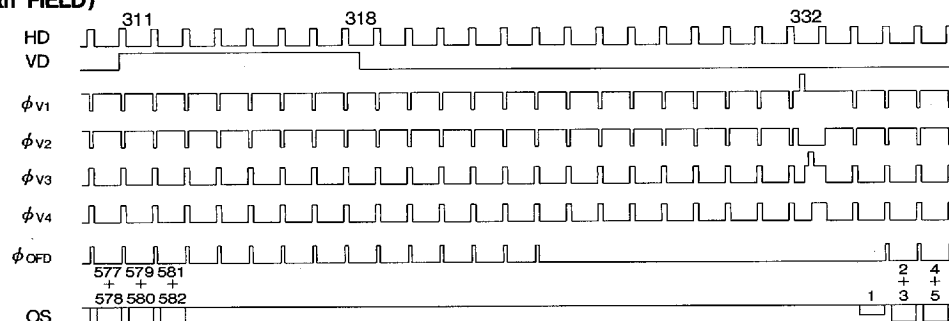
VERTICAL TRANSFER TIMING

Shutter speed
1/2000 s

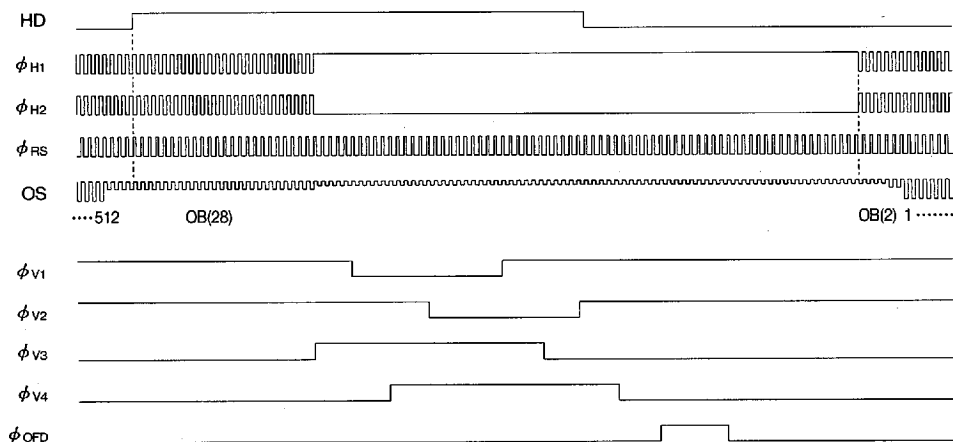
(1st, 3rd FIELD)



(2nd, 4th FIELD)

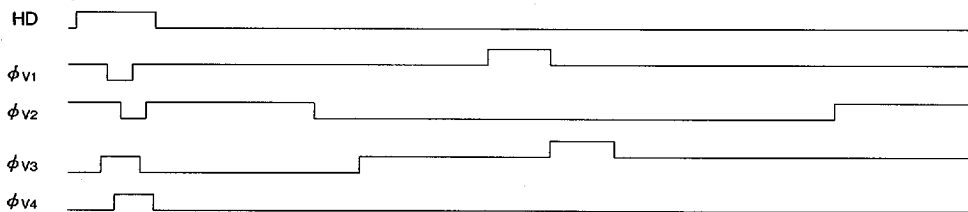


HORIZONTAL TRANSFER TIMING

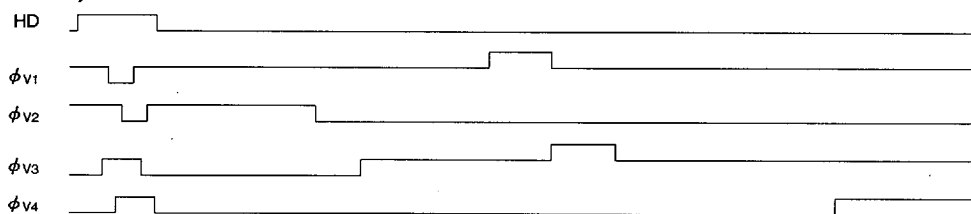


READOUT TIMING

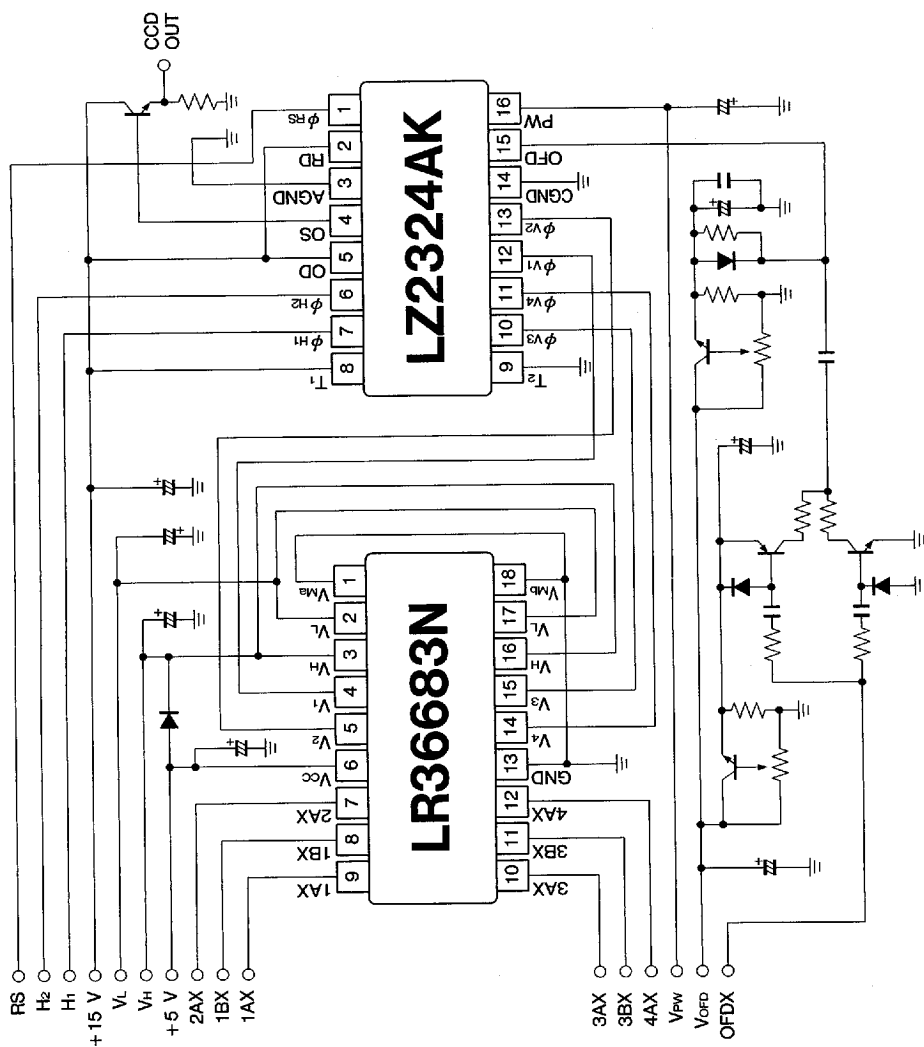
(1st, 3rd FIELD)



(2nd, 4th FIELD)



SYSTEM CONFIGURATION EXAMPLE



2 CCD AREA SENSORS