Integrated Device Technology, Inc.

32K X 8 CMOS DUAL-PORT STATIC RAM MODULE

IDT7M137

FEATURES:

- High-density 256K CMOS Dual-Port static RAM module
- 32K x 8 organization
- Fully asynchronous read/write operation from either port
- Fast access time
  - commercial: 30ns (max.)
  - military: 40ns (max.)
- Low power consumption
- Dual Vcc and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Single 5V (±10%) power supply

DESCRIPTION:

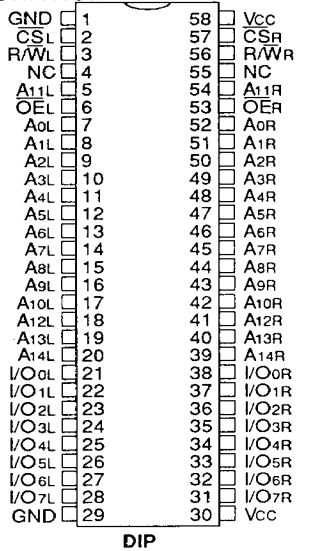
The IDT7M137 is a 256K high-speed CMOS Dual-Port static RAM module constructed on a multi-layered ceramic substrate using eight IDT7134 dual-port static RAMs in leadless chip carriers. The full 32K bytes of dual-port static RAM are directly addressable by utilization of the two on-board IDT54/IDT74FCT138 decoder circuits that interpret the higher order addresses A_{L12-14} and A_{R12-14} to select one of the eight 4K x 8 dual-port static RAMs. Extremely high speeds are achieved in this fashion due to the use of the IDT7134 dual-port static RAM, fabricated in IDT's high-performance CEMOS™ technology.

The IDT7M137 provides two ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in the memory. The IDT7M137 is designed to be used in systems where on-chip hardware port arbitration is not needed. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports.

The IDT7M137 is available with access times as fast as 30ns commercial and 40ns military temperature range. The module fits into a 58-pin sidebrazed DIP (Dual In-line Package).

All IDT7M137 military module semiconductor components are manufactured in compliance to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION[1]



2685 drw 01

DIP
TOP VIEW

NOTE:

1. For module dimensions, please refer to module drawing M12 in the packaging section.

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
Vcc	Vcc	Power
GND	GND	Ground
$\overline{CS}_L$	$\overline{CS}_R$	Chip Select
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L-14L}	A_{0R-14R}	Address
I/O_{0L-7L}	I/O_{0R-7R}	Data Input/Output
NC	NC	No Connect

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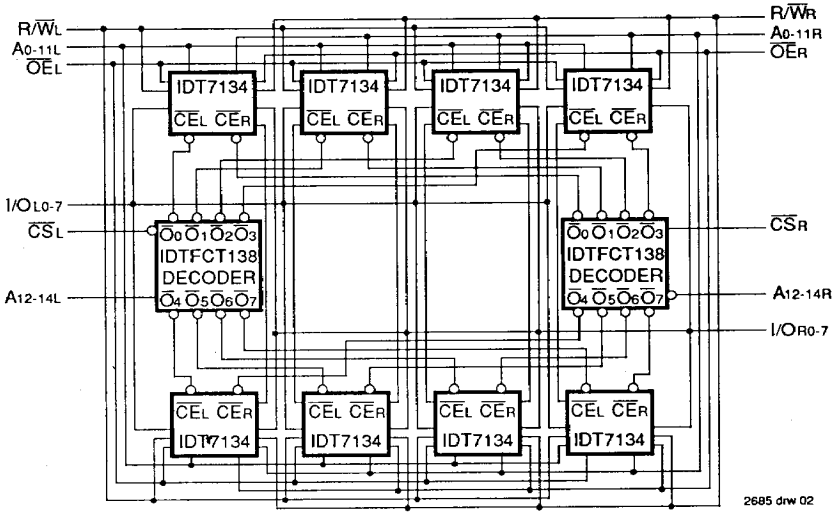

FUNCTIONAL DESCRIPTION:

The IDT7M137 provides two ports with separate controls, address and I/O that permit independent access for reads or writes to any location in memory. The IDT7M137 has an automatic power down feature controlled by $\overline{CS}$. The $\overline{CS}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CS}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

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NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

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RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2685 tbl 04

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

CAPACITANCE (1) (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{OUT}	Output Capacitance	V_{IN} = 0V	120	pF
C_{IN}	Input Capacitance	V_{OUT} = 0V	50	pF

2685 tbl 09

NOTE:
1. This parameter is guaranteed by design, but not tested.

DC ELECTRICAL CHARACTERISTICS (4)

(Vcc = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7M137 Min.	Typ.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	Vcc = 5.5V, V_{IN} = 0V to Vcc	—	—	20	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to Vcc	—	—	20	µA
V_{IH}	Input High Voltage		2.2	—	6.0	V
V_{IL}	Input Low Voltage		-1.0(2)	—	0.8	V
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CS}$= V_{IL}, Outputs Open	—	275	730	mA
I_{SB}	Standby Current (Both Ports Standby)	$\overline{CS}_L$ and $\overline{CS}_R$ ≥ V_{IH}, Vcc = Max., Both Ports Outputs Open	—	200	560	mA
I_{SB1}	Standby Current (One Port Standby)	$\overline{CS}_L$ or $\overline{CS}_R$ ≥ V_{IH}, Vcc = Max., Active Port Outputs Open	—	225	650	mA
I_{SB2}	Full Standby Current (Both Ports Full Standby)	Both Ports $\overline{CS}_L$ and $\overline{CS}_R$ ≥ Vcc -0.2V V_{IN} ≥ Vcc -0.2V or V_{IN} ≤ 0.2V	—	8	240(3)	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA I_{OL} = 10mA	— —	— —	0.4 0.5	V V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	—	V

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NOTES:
1. Vcc = 5V, T_A = +25°C
2. V_{IL} min. = -3.0V for pulse width less than 30ns.
3. I_{SB2} max. of IDTM137 at commercial temperature = 150mA.4. For tAA = 30, 35, 40, 45ns versions all DC parameters are preliminary only.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1,2 and 3

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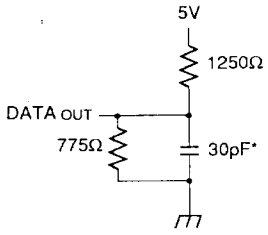

Figure 1.
Output Load

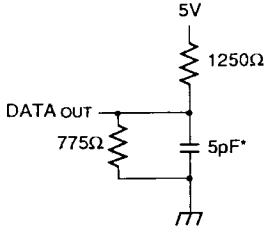

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Figure 2.
Output Load
(for tHZ, tLZ, twz, and tow)

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(Vcc = 5.0V ±10%, TA = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	7M137S30 (Com'l. Only) Min.	Max.	7M137S35 (Com'l. Only) Min.	Max.	7M137S40 Min.	Max.	7M137S45 Min.	Max.	Unit
READ CYCLE										
tRC	Read Cycle Time	30	—	35	—	40	—	45	—	ns
tAA	Address Access Time	—	30	—	35	—	40	—	45	ns
tACS	Chip Select Access Time	—	30	—	35	—	40	—	45	ns
tOE	Output Enable Access Time	—	15	—	20	—	25	—	30	ns
tOH	Output Hold From Address Change	0	—	0	—	0	—	0	—	ns
tCLZ(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
tCHZ(1)	Chip Select to Output in High Z	—	10	—	15	—	15	—	25	ns
tOHZ(1)	Output Enable to Output in High Z	—	10	—	15	—	15	—	25	ns
tOLZ(1)	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	ns
tPU(1)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
tPD(1)	Chip Deselect to Power Down Time	—	50	—	50	—	50	—	60	ns
WRITE CYCLE										
twc	Write Cycle Time	30	—	35	—	40	—	45	—	ns
tCW	Chip Select to End of Write	25	—	30	—	35	—	40	—	ns
tAW	Address Valid to End of Write	25	—	30	—	35	—	40	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	25	—	30	—	40	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	20	—	20	—	22	—	22	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tOHZ(1)	Output Enable to Output in High Z	—	10	—	15	—	15	—	20	ns
twHZ(1)	Write Enabled to Output in High Z	—	10	—	15	—	15	—	20	ns
tOW(1)	Output Active From End of Write	0	—	0	—	0	—	0	—	ns

2685 tbl 06

NOTES:
1. This parameter is guaranteed by design, but not tested.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V± 10%, T_A = -55°C to + 125°C and 0°C to + 70°C) (Continued)

Symbol	Parameter	IDTM137S55 Min.	IDTM137S55 Max.	IDTM137S60 Min.	IDTM137S60 Max.	IDTM137S70 (Mil. Only) Min.	IDTM137S70 (Mil. Only) Max.	IDTM137S90 (Mil. Only) Min.	IDTM137S90 (Mil. Only) Max.	IDTM137S100 (Mil. Only) Min.	IDTM137S100 (Mil. Only) Max.	Unit
READ CYCLE												
t_{RC}	Read Cycle Time	55	—	60	—	70	—	90	—	100	—	ns
t_{AA}	Address Access Time	—	55	—	60	—	70	—	90	—	100	ns
t_{ACS}	Chip Select Access Time	—	55	—	60	—	70	—	90	—	100	ns
t_{OE}	Output Enable Access Time	—	35	—	35	—	40	—	40	—	40	ns
t_{OH}	Output Hold From Address Change	0	—	0	—	0	—	10	—	10	—	ns
t_{CLZ} (1)	Chip Select to Output in Low Z	15	—	15	—	15	—	15	—	15	—	ns
t_{CHZ} (1)	Chip Select to Output in High Z	—	35	—	40	—	40	—	40	—	40	ns
t_{OLZ} (1)	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OHZ} (1)	Output Enable to Output in High Z	—	30	—	35	—	40	—	40	—	40	ns
t_{PU} (1)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD} (1)	Chip Deselect to Power Down Time	—	60	—	60	—	60	—	60	—	60	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	55	—	60	—	70	—	90	—	100	—	ns
t_{CW}	Chip Select to End of Write	50	—	55	—	60	—	80	—	90	—	ns
t_{AW}	Address Valid to End of Write	50	—	55	—	60	—	80	—	90	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	45	—	50	—	55	—	70	—	80	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	5	—	10	—	10	—	ns
t_{DW}	Data Valid to End of Write	25	—	30	—	35	—	45	—	50	—	ns
t_{DH}	Data Hold Time	5	—	5	—	5	—	10	—	10	—	ns
t_{OHZ} (1)	Output Enable to Output in High Z	—	35	—	40	—	40	—	40	—	50	ns
t_{WHZ} (1)	Write Enabled to Output in High Z	0	35	0	40	0	40	0	40	0	50	ns
t_{OW} (1)	Output Active From End of Write	0	—	0	—	0	—	0	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.

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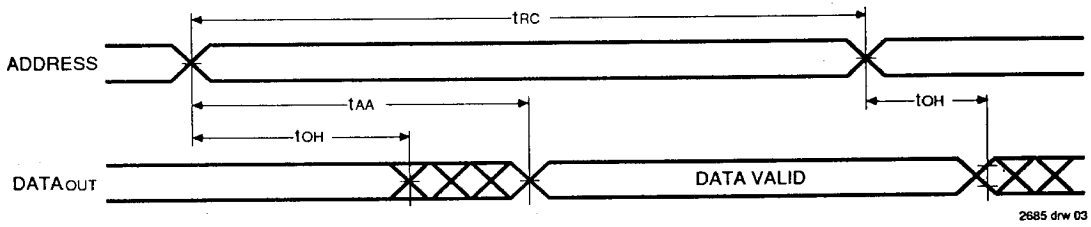
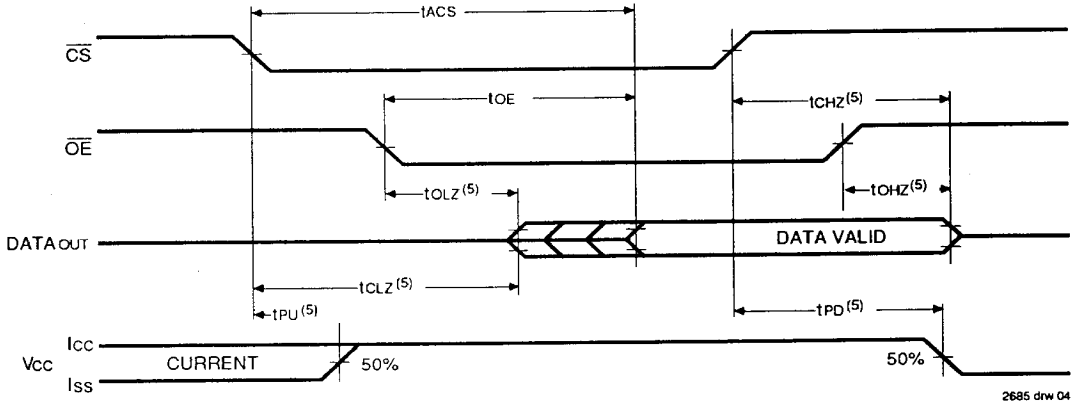
TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1, 2, 4)

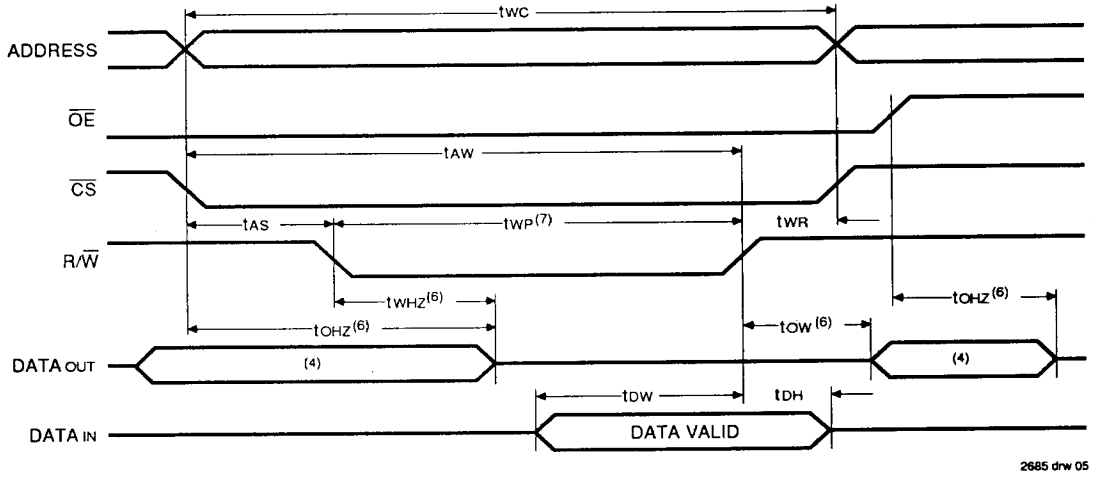


TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1, 3)

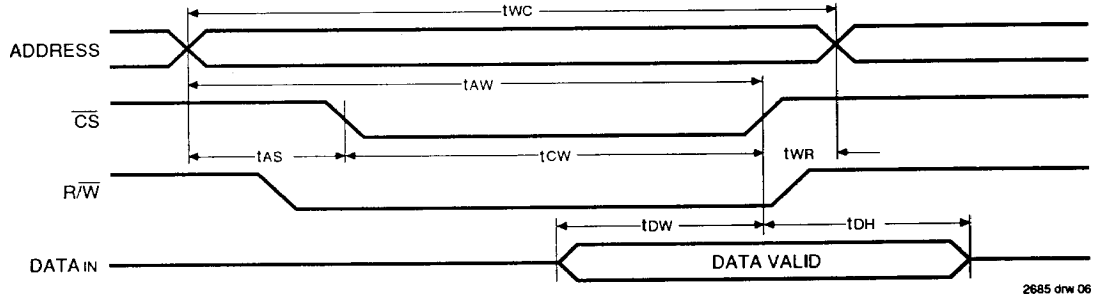


NOTES:
1. R/$\overline{W}$ is High for Read Cycles.
2. Device is continuously enabled, $\overline{CS}$ = VIL.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)(1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. R/$\overline{W}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a R/$\overline{W}$ controlled write cycle, write pulse (tWP) > (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

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