32 kHz Standard Watch CMOS IC

Features

- 32 kHz oscillator
- 1.3 to 1.8 V operating voltage range
- 200 nA typical current consumption
- Voltage regulator
- Integrated capacitors, mask-selectable
- Mask options for pad designation, motor period and motor pulse width
- Low resistance outputs for bipolar stepping motor
- Motor fast-test function

Pad Configuration

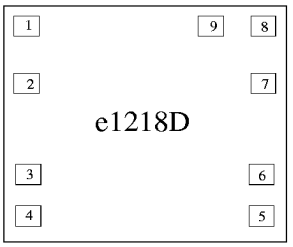

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Figure 1.

Chip size: 1.47 x 1.27 mm^2

General Description

The e1218D is an integrated circuit in CMOS Silicon-Gate Technology for analog watches. It consists of a 32 kHz oscillator, frequency dividers down to 1/64 Hz, output pulse formers and push-pull motor drivers. Capacitors are provided (selectable mask option) for tuning the crystal. Low current consumption and high oscillator stability are achieved by an on-chip voltage regulator.

Pin	Symbol	Function
1 to 4	V_{SS}	Negative supply voltage
1 to 8	V_{DD}	Positive supply voltage
(1/2) or (3/4)	OSCIN/ OSCOUT	Oscillator input/ output
(3/5), (3/6), (7/5) or (7/6)	MOT 1/2	Motor drive outputs
1 to 8	RESET	Reset input
1 to 9	TEST	Test input/ output

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage	V_{SS}	–0.3 to +5 V	V
Input voltage range, all inputs	V_{IN}	(V_{SS} – 0.3 V) V_{IN}, (V_{DD} + 0.3 V)	V
Output short-circuit duration		indefinite	
Power dissipation (DIL package)	P_{tot}	125 mW	mW
Operating ambient temperature range	T_{amb}	–20 to +70	°C
Storage temperature range	T_{stg}	–40 to +125	°C
Lead temperature during soldering at 2 mm distance, 10 seconds	T_{sld}	260	°C

Absolute maximum ratings define parameter limits which, if exceeded, may permanently change or damage the device.

All inputs and outputs in TEMIC Semiconductors circuits are protected against electrostatic discharges. However, precautions to minimize the build-up of electrostatic charges during handling are recommended.

This circuit is protected against supply voltage reversal for typically 5 minutes.

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Functional Description

Voltage Regulator

An integrated voltage regulator provides the oscillator with a well controlled negative supply voltage V_{REG}. This improves the stability of the oscillator. Due to this reduced supply voltage, the total power consumption of the circuit will decrease.

Oscillator

An oscillator inverter with feedback resistor is provided for generation of the 32768 Hz clock frequency. A total capacitance of 38 pF is integrated, which can be selected for C_{OSCIN} and C_{OSCOUT} in 2 pF increments by a mask option.

Frequency Divider

A 21-bit binary counter is provided, dividing the oscillator frequency down to 1/64 Hz. The leading six stages are connected to V_{DD} and V_{REG}, while the remaining 15 stages are connected to V_{DD} and V_{SS}.

Motor Drive Output

The e1218D contains two push-pull output buffers for driving bipolar stepping motors. During a motor pulse the n-channel device of one buffer and the p-channel device of the other buffer will be activeted. Between two pulses the n-channel devices of both buffers are active (figure 3).

Cycle time and pulse width can be chosen from various options by the interconnection mask (table 1).

RESET

A debounced RESET input is provided. Connecting the RESET input to V_{DD} resets the low order 12 stages of the frequency divider, thus disabling further motor pulses. Motor pulses in progress when the reset function is applied are then completed. After releasing the RESET pad from V_{DD}, the next motor pulse appears with a delay of one half motor cycle on the drive output opposed to the former (figure 4). Due to the debounce circuitry on the RESET input, V_{DD} must be applied for at least 23.4 ms. During RESET the input current at the pad is limited to 8 nA typical.

TEST

A test frequency of 512 Hz is output to this pad and can be measured with a high resistance probe (R 10 M , C 20 pF). This signal can be used for testing and tuning the oscillator. Connecting TEST to V_{DD} for at least 4 ms changes the motor cycle time from the selected value to the test cycle time (mask-options), while the motor pulse width remains unchanged (figure 5).

This feature can be used to reduce the amount of time required for testing the mechanical parts of the watch.

Table 1. Motor options

Cycle time T_M	=	2, 4, 6, 8, 10, 12, 20, 24, 30, 40, 60, 120 sec
Motor pulse width t_M	=	0.98 to 14.65 msec in increments of 0.98 msec
Motor test cycle time T_{MT}	=	250, 125, 62.5 msec

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Operating Characteristics

V_{DD} = 0, V_{SS} = –1.5 V, T_{amb} = +25°C; unless otherwise specified. All voltage levels are measured with reference to V_{DD}. Test crystal as specified below.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Operating voltage	Functional test (figure 1)	V_{SS}	–1.3		–1.8	V
Operating current	C_{OUT} = 5 pF, C_{TR} = 15 pF, R_L = ∞ C_{OUT} = 16 pF, C_{TR} = 15 pF R_L = ∞	I_{SS}		–150 –200	 –380	nA nA
RESET input current	RESET = V_{DD}	I_R		8		nA
Motor outputs						
Motor output current	R_L = 2 k , V_{SS} = –1.55 V	I_M	± 0.7			mA
Motor period		T_M	Mask option			sec
Motor pulse width		t_M	Mask option			
Oscillator						
Stability	ΔV_{SS} = 100 mV, C_{TR} = 5 pF,	$\Delta f/f$		0.1		ppm
Start-up voltage	within 2 sec	V_{ST}	–1.3			V
Integrated input capacitance		C_{OSCIN}	Mask option			
Integrated output capacitance	$(C_{OSCIN} + C_{OSCOUT})_{max.}$ = 38 pF	C_{OSCOUT}	Mask option			

Note 1: Typical parameters represent the statistical mean values

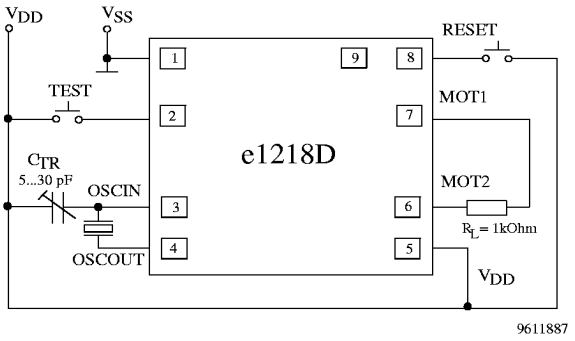

Figure 2. Functional test

Test Crystal Specification

Frequency	f = 32768 Hz
Series resistance	R_S = 30 k
Static capacitance	C_O = 1.5 pF
Dynamic capacitance	C_1 = 3 fF
Load capacitance	C_L = 8 pF

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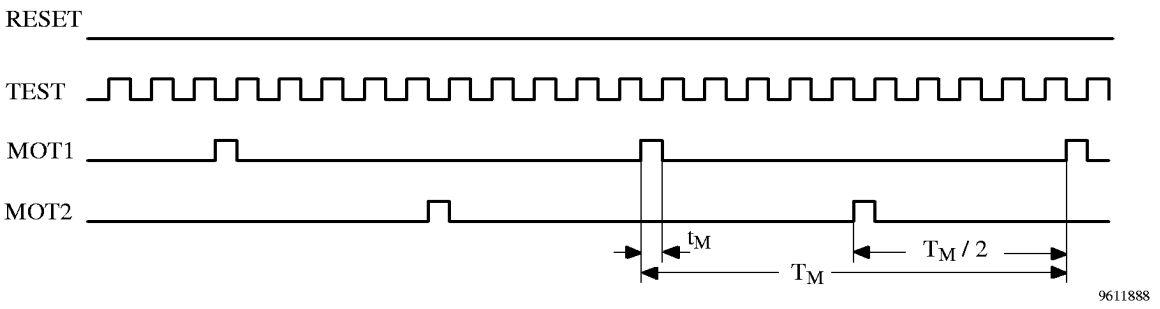

Figure 3. Motor drive output during normal mode

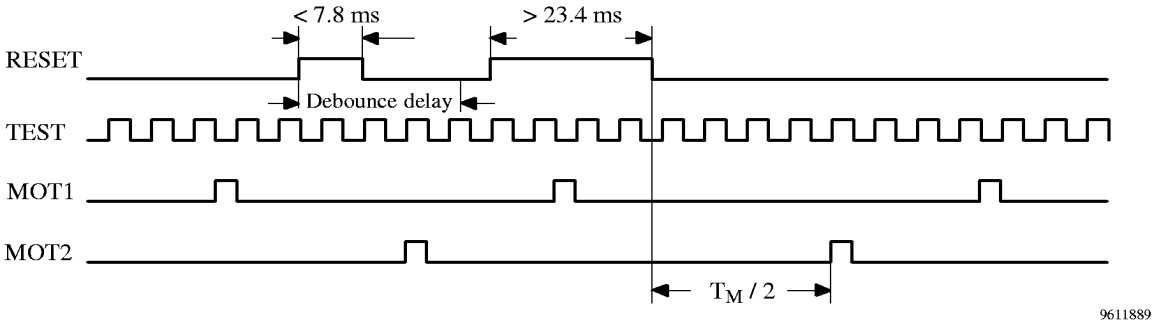

Figure 4. Motor drive output and RESET

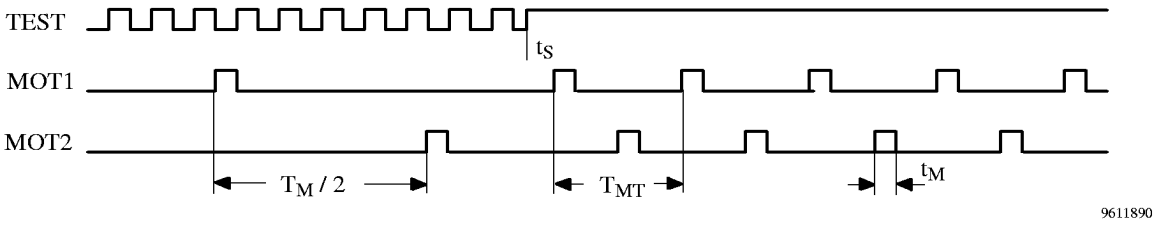

Figure 5. TEST mode: V_{DD} applied to TEST at time $t = t_s$

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