

GaAs MMIC Power Amplifier, 1.4 W 14.0-14.5 GHz

AM42-0002-DIE

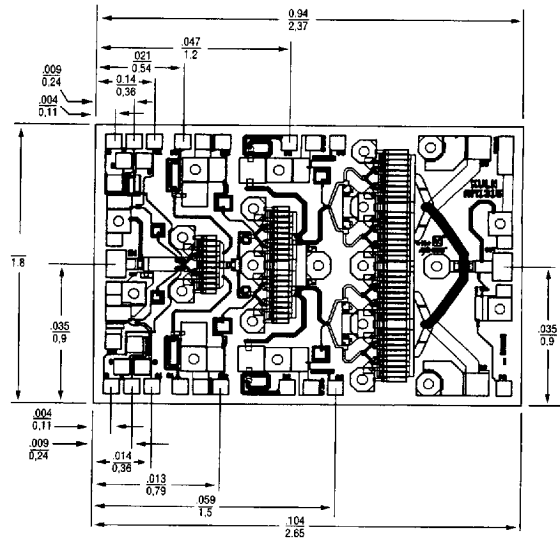
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Features

- High Linear Gain: 22 dB Typ.
- High Saturated Output Power: 31.5 dBm Typ.
- High Power Added Efficiency: 22% Typ.
- 50Ω Input/Output Broadband Matched
- Integrated Output Power Detector
- High Performance Ceramic Bolt Down Package

Description

M/A-COM's AM42-0002-DIE is a three-stage MMIC power amplifier fabricated on a mature 0.5-micron MBE based GaAs process. The AM42-0002-DIE employs a fully matched chip with integral bias networks and output power detector. This GaAs MMIC power amplifier is ideally suited for use as an output stage or driver in applications for VSAT systems.



1. Dimensions are inches/mm.

Ordering Information

Part Number	Package
AM42-0002-DIE	MMIC

Electrical Specifications¹, $T_B = +25^\circ\text{C}$, $V_{DD} = +9\text{ V}$, $V_{GG} = -1.2\text{ V}$, $Z_0 = 50\Omega$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Linear Gain	$P_{IN} \leq 0\text{ dBm}$ 14.0 - 14.5 GHz	dB		22	
Input VSWR	14.0 - 14.5 GHz			2.5:1	
Output VSWR	14.0 - 14.5 GHz			2.7:1	
Saturated Output Power	$P_{IN} = +14\text{ dBm}$ 14.0 - 14.5 GHz	dBm	30.5	31.5	
Output Power @ 1 dB Compression	14.0 - 14.5 GHz	dBm		30.5	
Output IP_3	14.0 - 14.5 GHz	dBm		40	
Power Added Efficiency (PAE)	$P_{IN} = +14\text{ dBm}$ 14.0 - 14.5 GHz	%		22	
Bias Current	I_{DD} (No RF) I_{GG} (No RF)	mA		800	0.1
Thermal Resistance	θ_{CB^2}	$^\circ\text{C/W}$		7.5	
Detector Output Voltage (Vdet)	$R_L = 10\text{ K}\Omega$, $P_{OUT} = +31\text{ dBm}$ 14.0 - 14.5 GHz	V		+3.5	

1. 100% on-wafer tested (50- μs pulse width, 20% duty factor) without resistor network on gates.
2. Channel to die backside.

Specifications Subject to Change Without Notice.

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M/A-COM, Inc.

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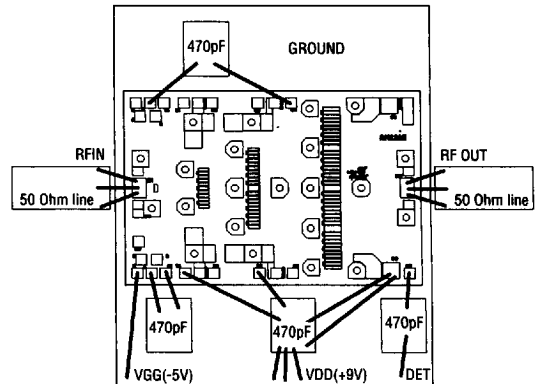
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Absolute Maximum Ratings^{1,2}

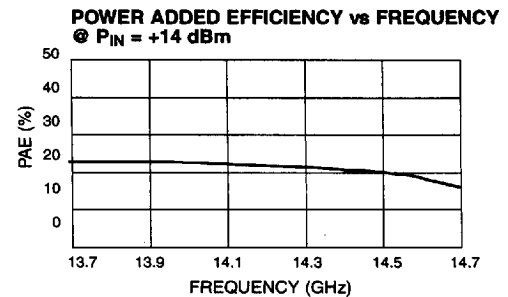
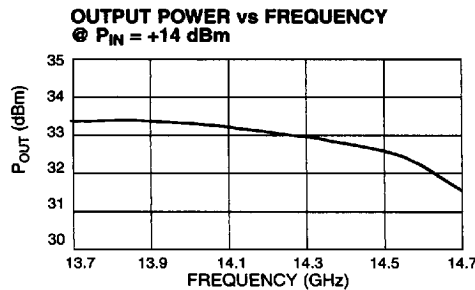
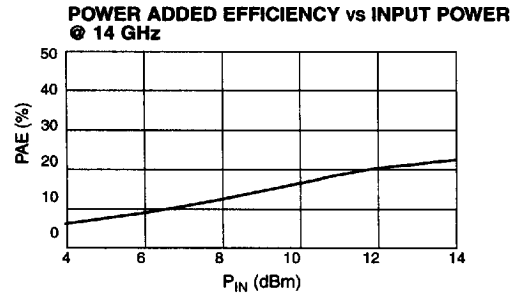
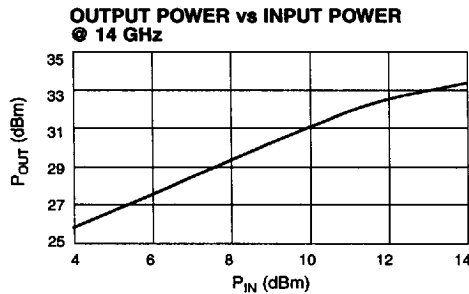
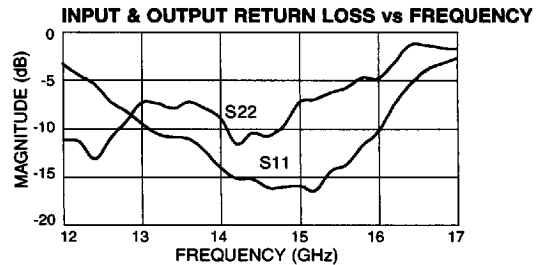
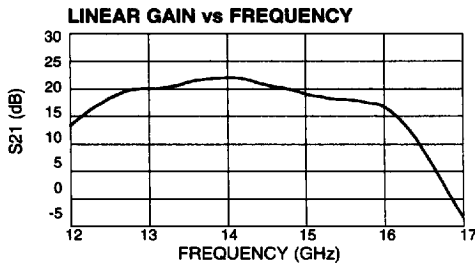
Parameter	Absolute Maximum
V _{DD}	12 Volts
V _{GG}	-10 Volts
Power Dissipation	16.7 W
RF Input Power	+23 dBm
Channel Temperature	150°C
Storage Temperature	-65°C to +150°C

1. Operation of this device outside any one of these limits may cause permanent damage.
2. Back of die temperature (T_B) = +25°C
3. Nominal bias is obtained by first connecting -5 volts to pin V_{GG} (resistor network used) followed by connecting +9 volts to pin V_{DD}. Note sequence.
4. It is recommended that the die be mounted with Au/Sn eutectic preforms for good RF ground and thermal interface.

Typical Bias Configuration^{3,4}



Typical Performance @ +25°C



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