4GB-2x256Mx72 DDR SDRAM REGISTERED ECC

FEATURES

- Double data rate architecture
- DDR200 and DDR266
  - JEDEC design specifications
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2, 2.5 (clock)
- Programmable Burst Length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto and self refresh
- Serial presence detect
- JEDEC standard 184 pin DIMM package
- Power supply: V_{DD}: 2.5V ± 0.2V
- Package Option JD3 30.46 (1.20") and AJD3 28.68 (1.13")

DESCRIPTION

The WED3EG72512SXX-JD3 is a 2x256Mx72 Double Data Rate SDRAM memory module based on 1 GB DDR SDRAM components. The module consists of thirtysix 1GB stacked DDR SDRAMs in 66 pin TSOP packages mounted on a 184 pin FR4 substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

OPERATING FREQUENCIES

	262JD3 DDR266 @CL=2	265JD3 DDR266 @CL=2.5	202JD3 DDR200 @CL=2
Speed @ CS=2	133MHz	133MHz	100MHz
Speed @ CS=2.5	133MHz	133MHz	———
CL-t_{RCD}-t_{RP}	2-3-3	2.5-3-3	2-2-2

PIN CONFIGURATION

PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	V_{REF}	47	DQS8	93	V_{SS}	139	V_{SS}
2	DQ0	48	A0	94	DQ4	140	DQS17
3	V_{SS}	48	A0	95	DQ5	141	A10
4	DQ1	50	V_{SS}	96	V_{DDQ}	142	CB6
5	DQS0	51	CB3	97	DQS9	143	V_{DDQ}
6	DQ2	52	BA1	98	DQ6	144	CB7
7	V_{DD}	53	DQ32	99	DQ7	145	V_{SS}
8	DQ3	54	V_{DDQ}	100	V_{SS}	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	RESET#	56	DQS4	102	NC	148	V_{DD}
11	V_{SS}	57	DQ34	103	NC	149	DQS13
12	DQ8	58	V_{SS}	104	V_{DDQ}	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	V_{SS}
15	V_{DDQ}	61	DQ40	107	DQS10	153	DQ44
16	NC	62	V_{DDQ}	108	V_{DD}	154	RAS#
17	NC	63	WE#	109	DQ14	155	DQ45
18	V_{SS}	64	DQ41	110	DQ15	156	V_{DDQ}
19	DQ10	65	CAS#	111	NC	157	CS0#
20	DQ11	66	V_{SS}	112	V_{DDQ}	158	NC
21	CKE0	67	DQS5	113	NC	159	DQS14
22	V_{DDQ}	68	DQ42	114	DQ20	160	V_{SS}
23	DQ16	69	DQ43	115	A12	161	DQ46
24	DQ17	70	V_{DD}	116	V_{SS}	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC
26	V_{SS}	72	DQ48	118	A11	164	V_{DDQ}
27	A9	73	DQ49	119	DQS11	165	DQ52
28	DQ18	74	V_{SS}	120	V_{DD}	166	DQ53
29	A7	75	NC	121	DQ22	167	A13
30	V_{DDQ}	76	NC	122	A8	168	V_{DD}
31	DQ19	77	V_{DDQ}	123	DQ23	169	DQS15
32	A5	78	DQS6	124	V_{SS}	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	V_{SS}	80	DQ51	126	DQ28	172	V_{DDQ}
35	DQ25	81	V_{SS}	127	DQ29	173	NC
36	DQS3	82	V_{DDID}	128	V_{DDQ}	174	DQ60
37	A4	83	DQ56	129	DQS12	175	DQ61
38	V_{DD}	84	DQ57	130	A3	176	V_{SS}
39	DQ26	85	V_{DD}	131	DQ30	177	DQS16
40	DQ27	86	DQS7	132	V_{SS}	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	V_{SS}	88	DQ59	134	CB4	180	V_{DDQ}
43	A1	89	V_{SS}	135	CB5	181	SA0
44	CB0	90	NC	136	V_{DDQ}	182	SA1
45	CB1	91	SDA	137	CK0	183	SA2
46	V_{DD}	92	SCL	138	CK0#	184	V_{DDSPD}

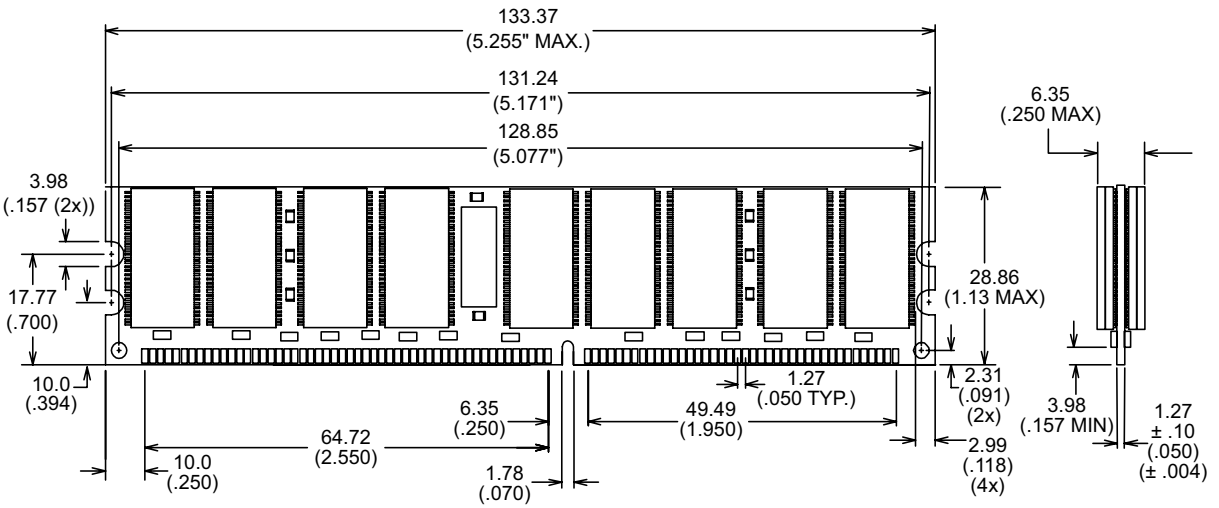
PIN NAMES

A0 ~ A13	Address Input (Multiplexed)
BA0 ~ BA1	Bank Select Address
DQ0 ~ DQ63	Data Input/Output
CB0 ~ CB7	Check Bits
DQS0 ~ DQS17	Data Strobe Input/Output
CK0	Clock Input
CK0#	Clock Input
CKE0, CKE1	Clock Enable Input
CS0#, CS1#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
V_{DD}	Power Supply (2.5V)
V_{DDQ}	Power Supply for DQS (2.5V)
V_{SS}	Ground
V_{REF}	Power Supply for Reference
V_{DDSPD}	Serial EEPROM Power/Supply (2.3V to 3.6V)
SDA	Serial Data I/O
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
V_{DDID}	V_{DD} Identification Flag
NC	No Connection
Reset	RESET ENABLE

ORDERING INFORMATION FOR AJD3

Part Number	Density	Speed	CAS Latency	Organization	Height*
WED3EG72512S262AJD3	4GB	133MHz/266Mbps	2	2 x 256M x 72	28.68 (1.13")
WED3EG72512S265AJD3	4GB	133MHz/266Mbps	2.5	2 x 256M x 72	28.68 (1.13")
WED3EG72512S202AJD3	4GB	100MHz/200Mbps	2	2 x 256M x 72	28.68 (1.13")

PACKAGE DIMENSIONS FOR AJD3



All Dimensions are in millimeters and (inches)

MAX / MIN or typical where noted