

Description

The μPD8086 is a 16-bit microprocessor that has both 8-bit and 16-bit attributes. It has a 16-bit wide physical path to memory for high performance. Its architecture allows higher throughput than the 5 MHz μPD8085A-2.

The maximum operating frequency of the μPD8086 is 5 MHz. The μPD8086-2 is an 8-MHz version.

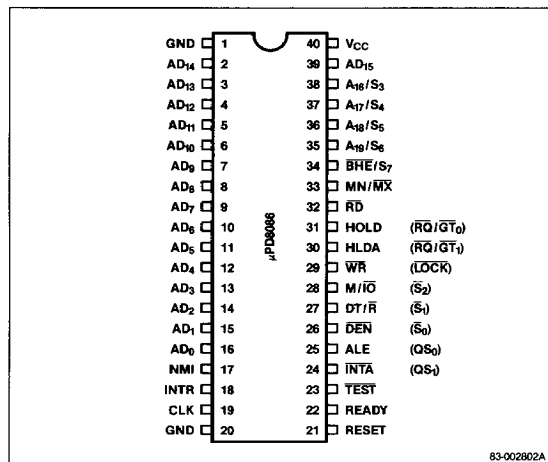
Features

- ☐ Can directly address 1 megabyte of memory
- ☐ Fourteen 16-bit registers with symmetrical operations
- ☐ Bit, byte, word, and block operations
- ☐ 8- and 16-bit signed and unsigned binary or decimal arithmetic operations
- ☐ Multiply and divide instructions
- ☐ 24 operand addressing modes
- ☐ Assembly language compatible with the μPD8080/8085
- ☐ Complete family of components for design flexibility

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD8086D	40-pin ceramic DIP	5 MHz
μPD8086D	40-pin cerdip	5 MHz
μPD8086D-2	40-pin cerdip	8 MHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1, 20	GND	Ground
2-16, 39	AD ₀ -AD ₁₅	Address / data bus
17	NMI	Non-maskable interrupt
18	INTR	Interrupt request
19	CLK	Clock
21	RESET	Reset
22	READY	Ready
23	TEST	Test
24	INTA	Interrupt acknowledge
25	ALE	Address latch enable
26	DEN	Data enable
27	DT / R	Data transmit / receive
28	M / IO	Memory / IO status
29	WR	Write
30	HLDA	Hold acknowledge
31	HOLD	Hold
32	RD	Read
33	MN / MX	Minimum / maximum
34	BHE / S ₇	Bus / high enable
35-38	A ₁₆ -A ₁₉	Most significant address bits
26-28, 34-38	S ₀ -S ₇	Status outputs
24, 25	QS ₁ , QS ₀	Queue status
29	LOCK	Lock
30, 31	RQ / GT ₀ RQ / GT ₁	Request / grant
40	V _{CC}	Power supply

Pin Functions

Ground

Ground.

Address/Data Bus

Multiplexed address (T1) and data (T2, T3, TW, T4) bus. 8-bit peripherals tied to the lower 8 bits use A₀ to condition chip select functions. These lines are three-state during interrupt acknowledge and hold states.

Non-Maskable Interrupt

This is an edge-triggered input causing a type 2 interrupt. A look-up table is used by the processor for vectoring information.

Interrupt Request

A level-triggered input sampled on the last clock cycle of each instruction. Vectoring is via an interrupt look-up table. INTR can mask in software by resetting the interrupt enable bit.

Clock

The clock input is a 1/3 duty cycle input basic timing for the processor and bus controller.

Reset

This active high signal must be high for 4 clock cycles. When it returns low, the processor restarts execution.

Ready

An acknowledgement from memory or I/O that data will be transferred. Synchronization is done by the μPD8284 clock generator.

Test

This input is examined by the WAIT instruction, and if low, execution continues. Otherwise the processor waits in an idle state. Synchronized by the processor on the leading edge of CLK.

Interrupt Acknowledge

This is a read strobe for reading vectoring information. During T₂, T₃, and TW of each interrupt acknowledge cycle it is low.

Address Latch Enable

This is used in conjunction with the μPD8282/8283 latches to latch the address, during T₁ of any bus cycle.

Data Enable

This is the output enable for the μPD8282/8287 transceivers. It is active low during each memory and I/O access and INTA cycles.

Data Transmit/Receive

Used to control the direction of data flow through the transceivers.

Memory/I/O Status

This is used to separate memory access from I/O access.

Write

Depending on the state of the M/ $\overline{\text{IO}}$ line, the processor is either writing to I/O or memory.

Hold Acknowledge

A response to the HOLD input, causing the processor to three-state the local bus. The bus becomes active one cycle after HOLD goes low again.

Hold

When another device requests the local bus, driving HOLD high will cause the μPD8086 to issue a HLDA.

Read

Depending on the state of the M/ $\overline{\text{IO}}$ line, the processor is reading from either memory or I/O.

Minimum/Maximum

This input is to tell the processor which mode it is to be used in. This effects some of the pin descriptions.

Bus/High Enable

This is used in conjunction with the most significant half of the data bus. Peripheral devices on this half of the bus use BHE to condition chip select functions.

Most Significant Address Bits

These are the four most significant address bits for memory operations. Low during I/O operations.

Status Outputs

These are the status outputs from the processor. They are used by the μPD8288 to generate bus control signals.

Queue Status

Used to track the internal μPD8086 instruction queue.

Lock

This output is set by the LOCK instruction to prevent other system bus masters from gaining control.

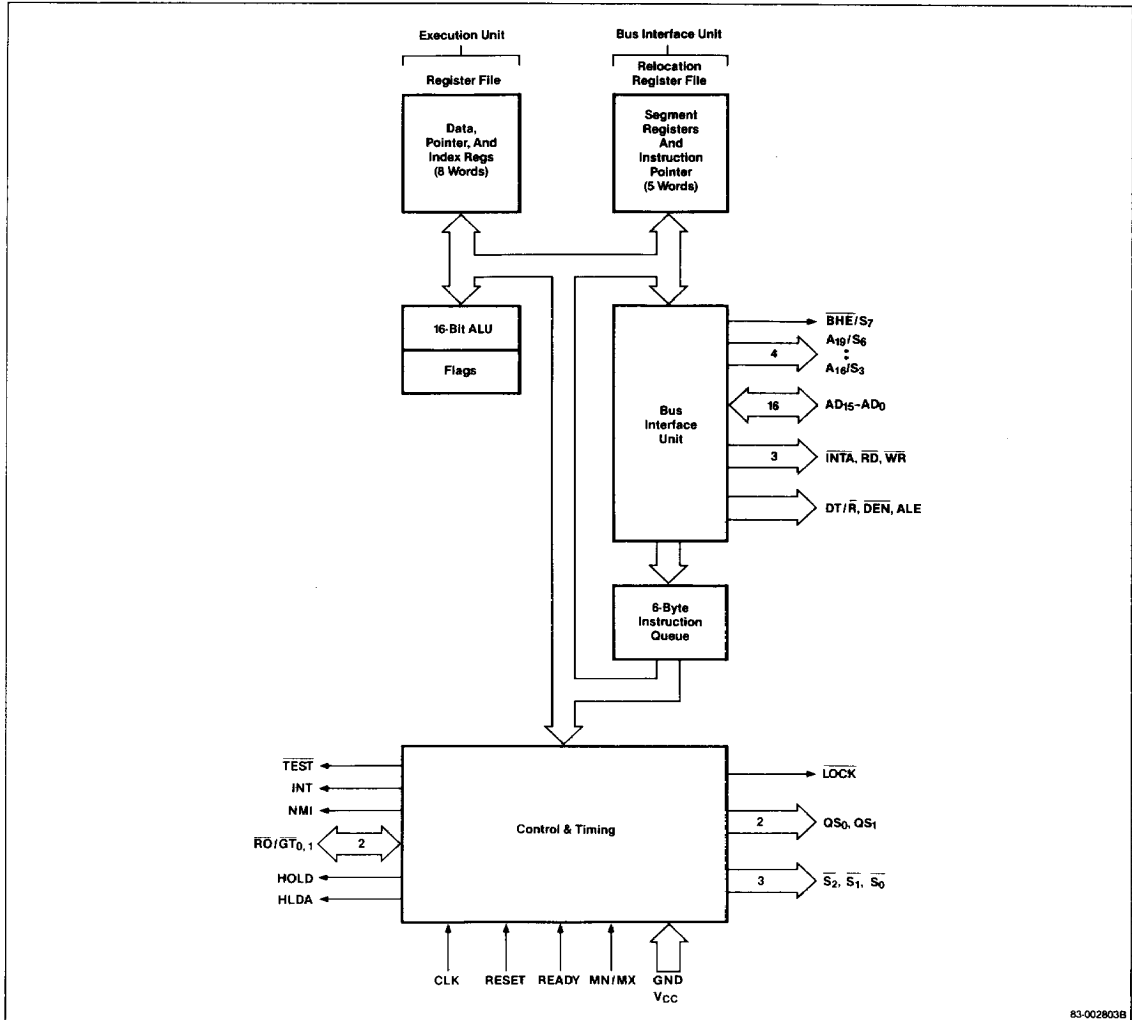
Request/Grant

Other local bus masters can force the processor to rebase the local bus at the end of the current bus cycle.

V_{CC}

This is the +5 V power supply.

Block Diagram



Absolute Maximum Ratings

T_A = 25°C

Power supply voltage, V _{CC}	-1.0 V to +7 V
Operating temperature, T _{OPT}	0°C to +70°C
Storage temperature, T _{STG}	-65°C to +150°C
Power dissipation, P _D	2.5 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

f_c = 1.0 MHz

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input capacitance	C _I			15	pF	(Note 1)
I/O capacitance	C _{IO}			15	pF	(Note 2)

Note:

- (1) All input pins except AD₀-AD₁₅ and $\overline{RQ}/\overline{GT}$.
 (2) Only input pins AD₀-AD₁₅ and $\overline{RQ}/\overline{GT}$.

AC Characteristics

Minimum Complexity System

μPD8086: T_A = 0°C to +70°C, V_{CC} = 5 V ± 10%

Parameter	Symbol	Limits				Unit	Test Conditions
		μPD8086		μPD8086-2			
		Min	Max	Min	Max		
CLK cycle period	t _{CLCL}	200	500	125	500	ns	
CLK low time	t _{CLCH}	(2/3 t _{CLCL}) – 15		(2/3 t _{CLCL}) – 15		ns	
CLK high time	t _{CHCL}	(1/3 t _{CLCL}) + 2		(1/3 t _{CLCL}) + 2		ns	
CLK rise time	t _{CH1CH2}		10		10	ns	From 1.0 V to 3.5 V
CLK fall time	t _{CL2CL1}		10		10	ns	From 3.5 V to 1.0 V
Data in setup time	t _{DVCL}	30		20		ns	
Data in hold time	t _{CLDX}	10		10		ns	
READY setup time into μPD8284	t _{R1VCL}	35		35		ns	(Notes 1 & 2)
READY hold time into μPD8284	t _{CLR1X}	0		0		ns	(Notes 1 & 2)
READY setup time into μPD8086	t _{RYHCH}	(2/3 t _{CLCL}) – 15		(2/3 t _{CLCL}) – 15		ns	
READY hold time into μPD8086	t _{CHRYX}	30		20		ns	
READY inactive to CLK	t _{RYLCL}	– 8		– 8		ns	(Note 3)
HOLD setup time	t _{HVCH}	35		20		ns	
INTR, NM _I , TEST setup time	t _{INVCH}	30		15		ns	(Note 2)
Input rise time	t _{ILIH}		20		20	ns	From 0.8 V to 2.0 V
Input fall time	t _{IIL}		12		12	ns	From 2.0 V to 0.8 V

DC Characteristics

T_A = 0°C to +70°C, V_{CC} = +5 V ± 10%

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input voltage low	V _{IL}	-0.5		+0.8	V	
Input voltage high	V _{IH}	2		V _{CC} + 0.5	V	
Output voltage low	V _{OL}			+0.45	V	I _{OL} = 2.5 mA
Output voltage high	V _{OH}	2.4			V	I _{OH} = -400 μA
Input clock voltage low	V _{CL}	-0.5		+0.6	V	
Output clock voltage high	V _{CH}	3.9		V _{CC} + 1.0	V	
Input leakage current	I _{LI}			±10	μA	0 V < V _{IN} < V _{CC}
Output leakage current	I _{LO}			±10	μA	0.45 V ≤ V _{OUT} ≤ V _{CC}
Power supply current	I _{CC}					
μPD8086 /				340	mA	T _A = 25°C
μPD8086-2				350	mA	T _A = 25°C

AC Characteristics (cont)

Timing Responses

μPD8086: T_A = 0°C to +70°C, V_{CC} = 5 V ± 10%

Parameter	Symbol	Limits				Unit	Test Conditions
		μPD8086		μPD8086-2			
		Min	Max	Min	Max		
Address valid delay	t _{CLAV}	10	110	10	60	ns	(Note 4)
Address hold time	t _{CLAX}	10		10		ns	(Note 4)
Address float delay	t _{CLAZ}	t _{CLAX}	80	t _{CLAX}	50	ns	(Note 4)
ALE width	t _{LHLL}	t _{CLCH} − 20		t _{CLCH} − 10		ns	(Note 4)
ALE active delay	t _{CLLH}		80		50	ns	(Note 4)
ALE inactive delay	t _{CHLL}		85		55	ns	(Note 4)
Address hold time to ALE inactive	t _{LLAX}	t _{CHCL} − 10		t _{CHCL} − 10		ns	(Note 4)
Data valid delay	t _{CLOV}	10	110	10	60	ns	(Note 4)
Data hold time	t _{CHDX}	10		10		ns	(Note 4)
Data hold time after WR	t _{WHDX}	t _{CLCH} − 30		t _{CLCH} − 30		ns	(Note 4)
Control active delay 1	t _{CVCTV}	10	110	10	70	ns	(Note 4)
Control active delay 2	t _{CHCTV}	10	110	10	60	ns	(Note 4)
Control active delay	t _{CVCTX}	10	110	10	70	ns	(Note 4)
Address float to READ active	t _{AZRL}	0		0		ns	(Note 4)
RD active delay	t _{CLRL}	10	165	10	80	ns	(Note 4)
RD inactive delay	t _{CLRH}	10	150	10	80	ns	(Note 4)
RD inactive to next address active	t _{RHAV}	t _{CLCL} − 45		t _{CLCL} − 40		ns	(Note 4)
HLDA valid delay	t _{CLHAV}	10	160	10	100	ns	(Note 4)
RD width	t _{RLRH}	2t _{CLCL} − 75		2t _{CLCL} − 50		ns	(Note 4)
WR width	t _{WLWH}	2t _{CLCL} − 60		2t _{CLCL} − 40		ns	(Note 4)
Address valid to ALE low	t _{AVALL}	t _{CLCH} − 60		t _{CLCH} − 40		ns	(Note 4)
Output rise time	t _{OLOH}		20		20	ns	From 0.8 V to 2.0 V
Output fall time	t _{OHOL}		12		12	ns	From 2.0 V to 0.8 V

Note:

- (1) Signal at μPD8284 shown for reference only.
- (2) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
- (3) Applies only to T2 state. (8 ns into T3)
- (4) C_L = 20-100 pF for all μPD8086 outputs (in addition to μPD8086 self-load).

AC Characteristics (cont)

Maximum Mode System with μPB8288 Bus Controller

μPD8086: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$

Parameter	Symbol	Limits				Unit	Test Conditions
		μPD8086		μPD8086-2			
		Min	Max	Min	Max		
CLK cycle period	t _{CLCL}	200	500	125	500	ns	
CLK low time	t _{CLCH}	(2/3 t _{CLCL}) – 15		(2/3 t _{CLCL}) – 15		ns	
CLK high time	t _{CHCL}	(1/3 t _{CLCL}) + 2		(1/3 t _{CLCL}) + 2		ns	
CLK rise time	t _{CH1CH2}		10		10	ns	From 1.0 V to 3.5 V
CLK fall time	t _{CL2CL1}		10		10	ns	From 3.5 V to 1.0 V
Data in setup time	t _{DVCL}	30		20		ns	
Data in hold time	t _{CLDX}	10		10		ns	
READY setup time into μPD8284	t _{R1VCL}	35		35		ns	(Notes 1 & 2)
READY hold time into μPD8284	t _{CLR1X}	0		0		ns	(Notes 1 & 2)
READY setup time into μPD8086	t _{RYHCH}	(2/3 t _{CLCL}) – 15		(2/3 t _{CLCL}) – 15		ns	
READY hold time into μPD8086	t _{CHRYX}	30		20		ns	
READY inactive to CLK	t _{RYLCL}	– 8		– 8		ns	(Note 5)
INTR, NMI, TEST setup time	t _{INVCH}	30		15		ns	(Note 2)
RQ / GT setup time	t _{GVCH}	30		15		ns	
RQ hold time into μPD8086	t _{CHGX}	40		30		ns	
Input rise time	t _{ILIH}		20		20	ns	From 0.8 V to 2.0 V
Input fall time	t _{IHIL}		12		12	ns	From 2.0 V to 0.8 V

AC Characteristics (cont)

Timing Responses

μPD8086: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$

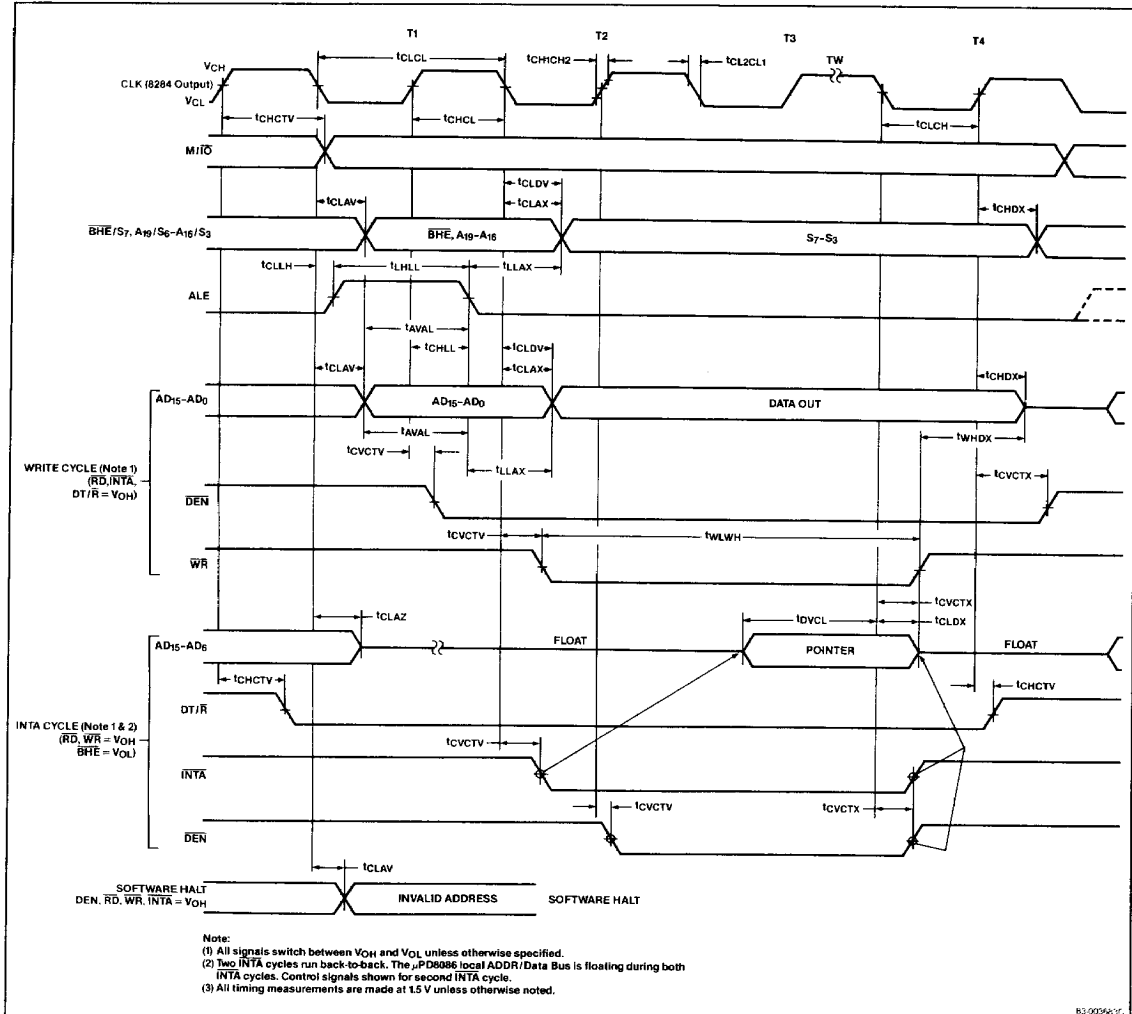
Parameter	Symbol	Limits				Unit	Test Conditions
		μPD8086		μPD8086-2			
		Min	Max	Min	Max		
Command active delay	t _{CLML}	10	35	10	35	ns	(Notes 1 & 4)
Command inactive delay	t _{CLMH}	10	35	10	35	ns	(Notes 1 & 4)
READY active to status passive	t _{RYHSH}		110		65	ns	(Notes 3 & 4)
Status active delay	t _{CHSV}	10	110	10	60	ns	(Note 4)
Status inactive delay	t _{CLSH}	10	130	10	70	ns	(Note 4)
Address valid delay	t _{CLAV}	10	110	10	60	ns	(Note 4)
Address hold time	t _{CLAX}	10		10		ns	(Note 4)
Address float delay	t _{CLAZ}	t _{CLAX}	80	t _{CLAX}	50	ns	(Note 4)
Status valid to ALE high	t _{SVLH}		15		15	ns	(Notes 1 & 4)
Status valid to MCE high	t _{SVMCH}		15		15	ns	(Notes 1 & 4)
CLK low to ALE valid	t _{CLLH}		15		15	ns	(Notes 1 & 4)
CLK low to MCE high	t _{CLMCH}		15		15	ns	(Notes 1 & 4)
ALE inactive delay	t _{CHLL}		15		15	ns	(Notes 1 & 4)
MCE inactive delay	t _{CLMCL}		15		15	ns	(Notes 1 & 4)
Data valid delay	t _{CLDV}	10	110	10	60	ns	(Note 4)
Data hold time	t _{CHDX}	10		10		ns	(Note 4)
Control active delay	t _{CVNV}	5	45	5	45	ns	(Notes 1 & 4)
Control inactive delay	t _{CVNX}	10	45	10	45	ns	(Notes 1 & 4)
Address float to READ active	t _{AZRL}	0		0		ns	(Note 4)
RD active delay	t _{CLRL}	10	165	10	100	ns	(Note 4)
RD inactive delay	t _{CLRH}	10	150	10	80	ns	(Note 4)
RD inactive to next address active	t _{RHAV}	t _{CLCL} – 45		t _{CLCL} – 40		ns	(Note 4)
Direction control active delay	t _{CHDTL}		50		50	ns	(Notes 1 & 4)
Direction control inactive delay	t _{CHDTH}		30		30	ns	(Notes 1 & 4)
GT active delay	t _{CLGL}	0	85	0	50	ns	(Note 4)
GT inactive delay	t _{CLGH}	0	85	0	50	ns	(Note 4)
RD width	t _{RLRH}	2t _{CLCL} – 50		2t _{CLCL} – 50		ns	(Note 4)
Output rise time	t _{OLDH}		20		20	ns	From 0.8 V to 2.0 V
Output fall time	t _{OHOL}		12		12	ns	From 2.0 V to 0.8 V

Note:

- (1) Signal at μPB8284 or μPB8288 shown for reference only.
- (2) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
- (3) Applies only to T3 and wait states.
- (4) $C_L = 20\text{--}100\text{ pF}$ for all μPD8086 outputs (in addition to μPD8086 self-load).
- (5) Applies only to T2 state. (8 ns into T3).

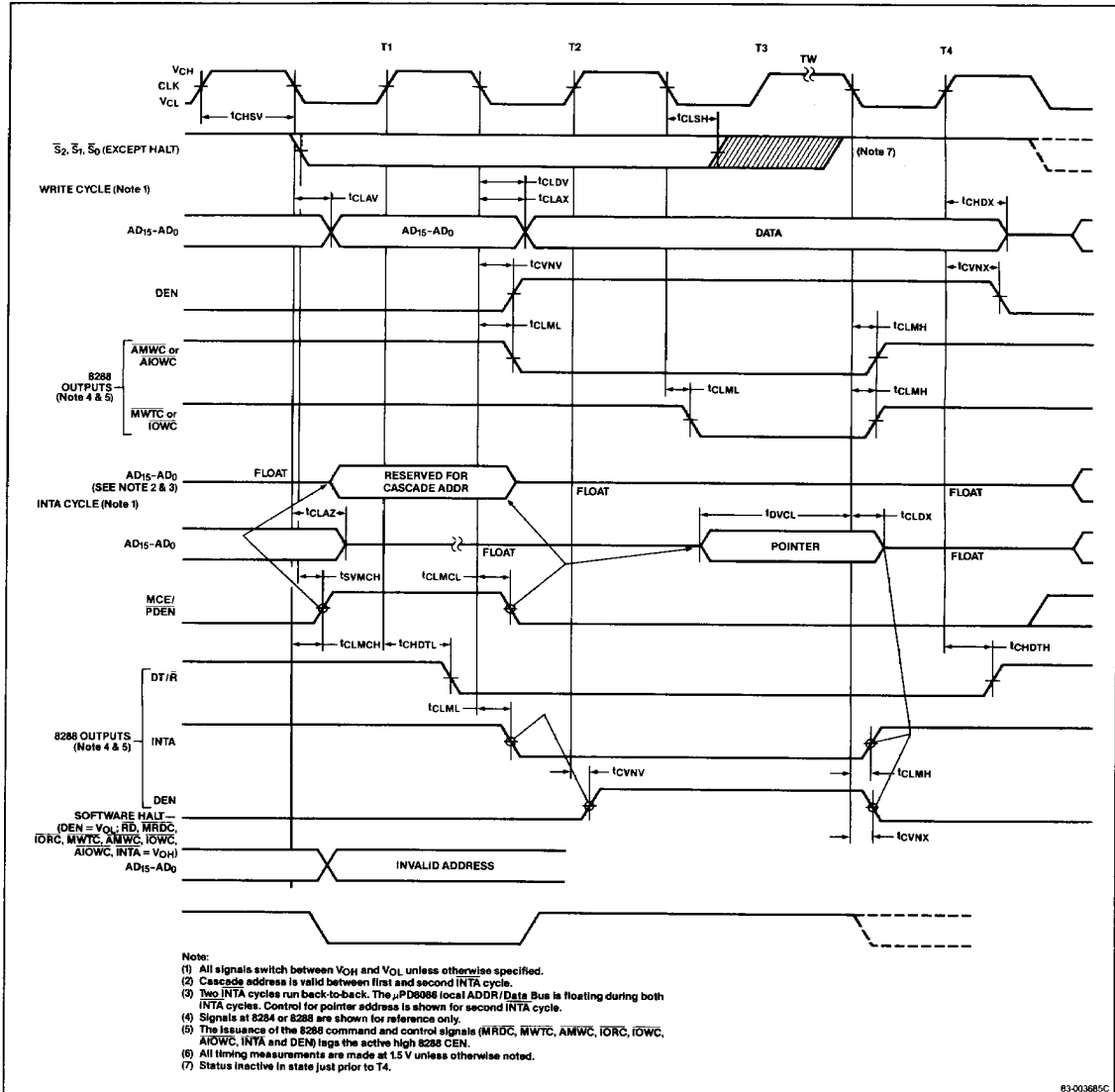
AC Timing Waveforms (cont)

Minimum Complexity Systems (Note 3)



AC Timing Waveforms (cont)

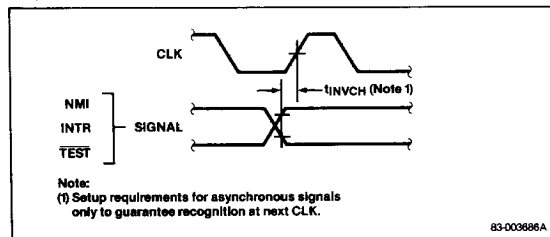
Maximum Mode System Using μPB8288 Controller (Note 6)



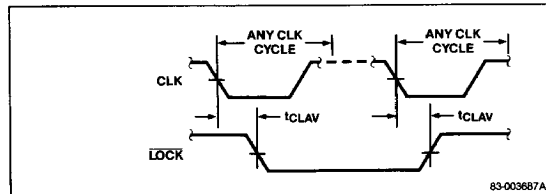
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Timing Waveforms

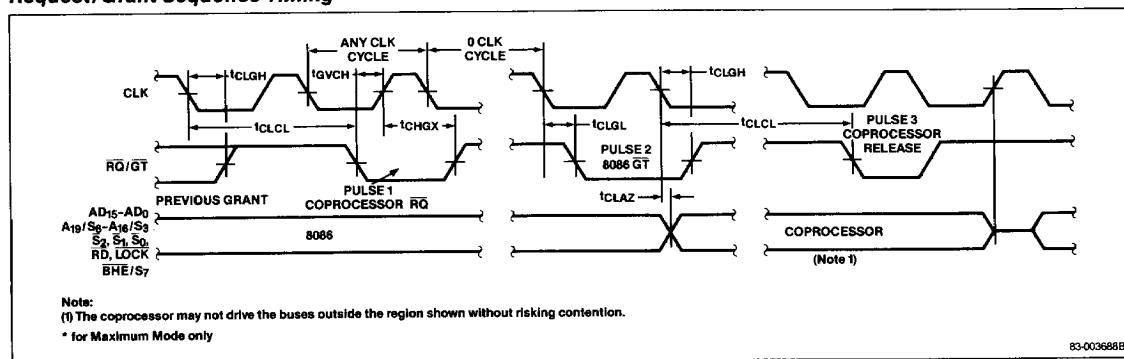
Asynchronous Signal Recognition



Bus Lock Signal Timing



Request/Grant Sequence Timing*



Hold/Hold Acknowledge Timing*

