EG&G RETICON

RA0640A
Solid State Imaging Array

General Description

EG&G Reticon's RA0640A Array is a two-dimensional self-scanned solid state imaging array. 300,720 discrete photodiodes are arranged in a 640 x 480 matrix. In contrast to comparable CCD devices, the discrete photodiode sensors require no surface electrode so there is no interference pattern or light loss and the full inherent sensitivity is obtainable. This also makes it much easier to deposit materials such as Cesium Iodide directly onto the surface of the silicon detector to generate the electron-hole pairs from an x-ray source which are captured and stored in the associated pixels.

Key Features

- 20 lines per millimeter resolution
- Dynamic range greater than 1,500:1
- On-chip Double Correlated Sampling Readout
- 50 µm center-to-center element spacing in both the X and the Y directions
- Data rates up to 10 MHz
- High antiblooming/antismearing capability

Functional Description

The die pinout configuration and PCB package pinout for the RA0640A are shown in Figure 1A and 1B. The device consists of several functional elements as shown in Figure 2 to control its operation. These elements have been indicated in Figure 2 by the dotted lines. They are:

1. Imaging Region

The first region consists of a 640 x 480 diode array matrix, schematically indicated by the columns and rows of individual photodiode sites. The diodes in each row are connected simultaneously through multiplex switches to one of two buffered amplifier outputs. The even columns to one row of buffers and the odd columns to another. When a row of diodes is selected, the signal charge is removed from the diodes and transferred through a common column video line into the associated buffer amplifier for readout. Each row of amplifiers then connect the stored pixel's data to an output video line one at a time.

2. Row Shift Register (Y Shift Register)

The second element consists of a two-phase static shift register which controls the multiplex switches to transfer an entire row. The register turns on each row of diodes in sequence and transfers the corresponding signal charge into the appropriate buffer. The row shift register is driven by a two-phase clock denoted by ϕ_{Y1} and ϕ_{Y2} in Figure 2. The row of pixels is dumped into the buffered readout multiplexer on an active ϕ_{Y2}.

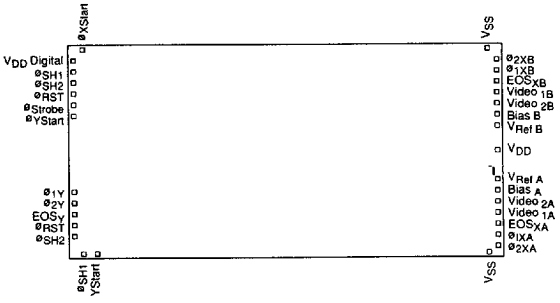
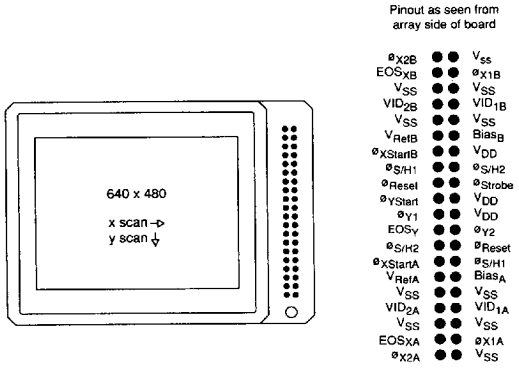


Figure 1A. Pinout Configuration, Die



Figue 1B. Pinout Configuration, PCB

3. Amplified and Buffered Readout Multiplexer

The third region in Figure 2 is the amplifier and buffered readout multiplexer. This region is also where the correlated double sampling capability is located. These are located at both the top and bottom of the imaging region. The even columns of diodes dump their accumulated charge into one buffer and the odd columns of diodes dump into the other. The charge from each pixel is converted to an output voltage by using internal feedback integration capacitors. Switched sampling circuits follow the capacitors. They are designed to provide, along with the buffer's gain, DC offset and noise correction. The stored voltage-output samples in turn are read out sequentially, becoming the active differential output when addressed by the static readout shift register multiplexer.

To use the on-chip double correlated sampling (DCS) noise reduction option, activate one sample and hold switch after the line reset is released, but before a row of pixel data is switched into the buffered readout. Activate the other sample and hold

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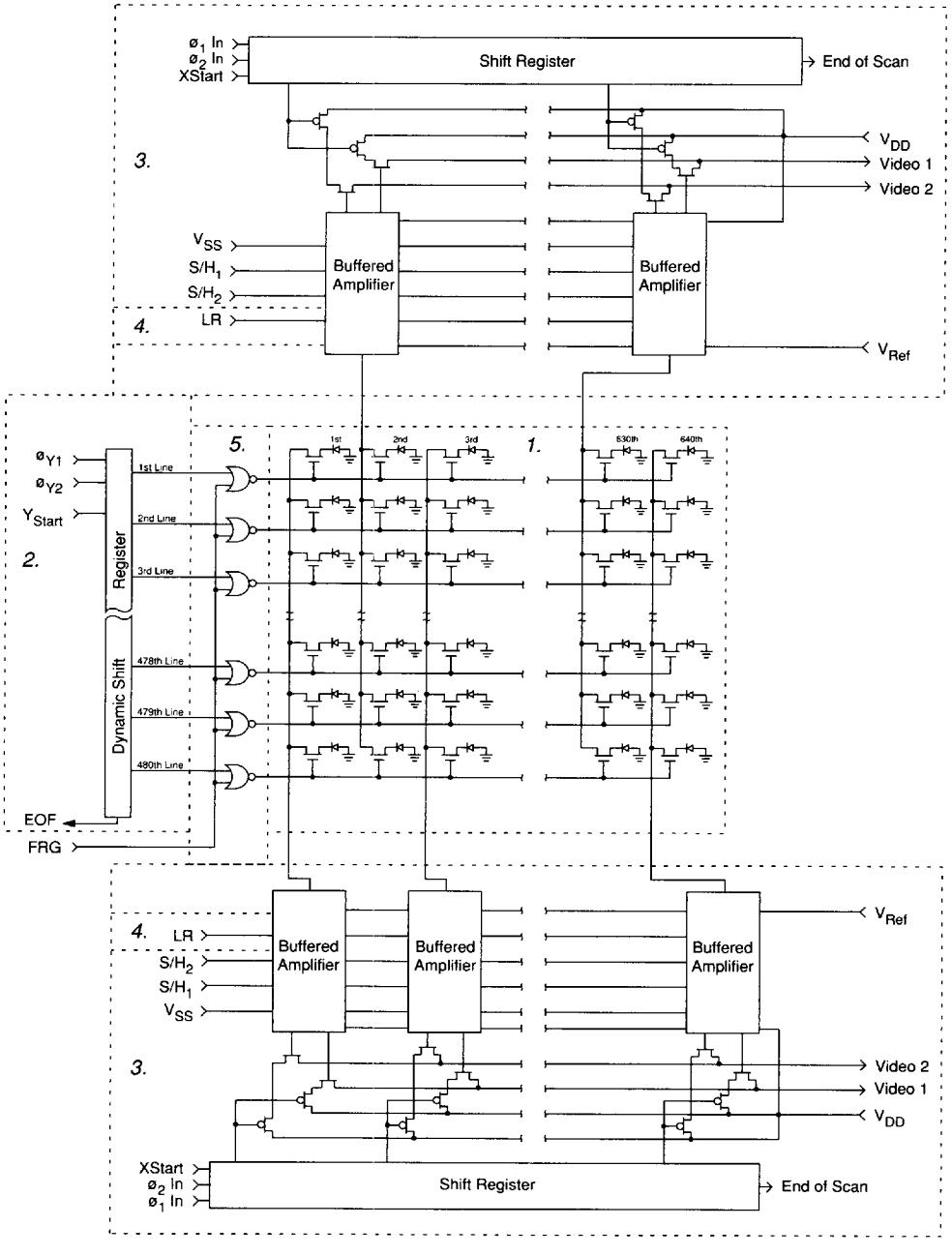

Figure 2. Schematic Diagram

switch after the row of pixel data has been switched into the buffered readout as shown in the timing diagrams of Figure 3. One sampled pair of data pulses contains any DC offset and switching noise which may have occurred on the video line. The other contains any DC offset switching noise and the integrated and converted image. The pair of pulses can be differentially combined to subtract off the noise and offset which may have occurred.

4. Line Reset (LR)

The LR maintains the potential of the column video line between line transfers by bleeding off the excess charges collected under excess exposure. It will require adjustment when the frame reset function is used.

5. Frame Reset Gate (FRG)

The fifth element consists of the frame reset gate, FRG. This switch provides access to the multiplex switches of all diodes in the matrix and allows the entire frame to be dumped to the buffered readout registers simultaneously. Used simultaneously with the Line Reset, this enables all charge accumulated in the array to be drained off. Since the diodes in each line are automatically reset as soon as the line is accessed, the frame reset control is not normally used and is held low. However, when a particular exposure is desired, this control may be used to clear the diodes to start a fresh integration cycle by setting the FRG terminal to V_{DD}. When this mode is used, a shutter or strobed input is needed since the diodes are sequentially accessed and will thus differ in exposure time if the beam input is continued during the readout sequence. The FRG and LR need to be active for at least 10 µsecs to fully recharge both the pixels and the video lines. Depending upon the timing, or the exposure, more line scans may be needed.

Device Operation

Figure 3 shows the timing diagram for the device. Two sets of complimentary clocks are needed; ϕ_{Y1} and ϕ_{Y2} for the simultaneous row multiplexer, and ϕ_{X1} and ϕ_{X2} for the readout multiplexers. For optimum operation, these clock pairs should not overlap. If the application requires clock overlap, they should not overlap by more than 50%. Since both the row shift register and register in the buffered readout multiplexer are static, the clock rise (tr) and fall (tr) times are not as critical as with a dynamic shift register.

The frame start pulse, ϕ_{YStart}, loads the row shift register with a voltage pulse to initiate the scanning process. It loads the register on each ϕ_{Y1} high to low (positive to negative) transition as long as the start pulse is held high. Therefore, to ensure that only one bit is loaded, the start pulse should be high during only one ϕ_{Y1} falling edge. Figure 3 illustrates the timing relationship with respect to ϕ_{Y1}. The clock amplitude of ϕ_{YStart} should be similar to the row shift clocks (ϕ_{Y1} and ϕ_{Y2}). The setup time (t_{set}) should be at least 30 ns and the hold time at least 20 ns.

Note: The shift register will load multiple bits if the start pulse is high for more than one ϕ_{Y1} falling edge.

The row of pixel data is dumped into the buffered readout multiplexer on each ϕ_{Y2} high pulse, once the frame start pulse has been successfully loaded.

There are two sample and hold gates ($\phi_{S/H1}$ and $\phi_{S/H2}$) associated with each readout multiplexer and can be used to facilitate double correlated sampling (DCS). Each pair of gates are linked to one bonding pad then split to each of the video outputs of that multiplexer. The circuit design for each sample and hold pair of gates are duplicates (see Figure 2). By sampling one gate immediately preceding a row transfer then sampling the other as the row transfer is occurring, one sample and hold circuit has the circuit noise and a DC offset, the other has the noise, DC offset, and the integrated signal. Using a simple differential circuit as shown in Figure 4 would provide the user with a signal which contains only the integrated signal.

The End Of Scan (EOS) pulse is generated at the output of the row shift register to mark the termination of the scan, the last position accessed with the ϕ_{Y2} clock going positive. On the next ϕ_{Y1} rising edge, the output pulse is applied to the gate of the EOS transistor.

The line start pulse, ϕ_{XStart}, initiated after the completion of the sample and hold circuits, loads each of the readout multiplexer shift registers with a voltage pulse to initiate the readout process. It loads the register on each ϕ_{X1} high to low (positive to negative) transition as long as the start pulse is held high. Therefore, to ensure that only one bit is loaded, the start pulse should be high during only one ϕ_{X1} falling edge. Figure 3 illustrates the timing relationship with respect to ϕ_{X1}. The clock amplitude of X_{Start} should be similar to the row shift clocks (ϕ_{X1} and ϕ_{X2}). The setup time (t_{set}) should be at least 30 ns and the hold time at least 20 ns. A line start pulse is needed each time a row of data from the imaging region is dumped into the buffered readout register to initiate the readout scan.

Note: The shift register will load multiple bits if the start pulse is high for more than one ϕ_{X1} falling edge.

An End Of Scan (EOS) pulse is generated at the output of each of the readout shift registers to mark the termination of each scan, the last position accessed with the ϕ_{X2} clocks going positive. On the next ϕ_{X1} rising edge, the output pulse is applied to the gate of the EOS transistor.

Two of the basic modes of imaging which can be achieved using this device are continuous and single shot. With the continuous mode of operation, after each row of pixels is dumped to the readout buffers, that row of diodes immediately start to integrate charge for the next frame readout. The total integration time of each row of diodes is the time between two consecutive readouts of the same row of diodes. When using the single shot mode of operation, frame reset is held on until immediately before a single pulse of energy, accomplished by either strobing or shuttering the source, is absorbed by the array. The array is then readout and frame reset is then turned on until the next energy pulse.

Array Cooling

Both the dark current and the noise performance of the array can be improved by cooling. The dark current will be reduced 50% for every 7°C reduction in array temperature. Cooling can be achieved via a thermo-electric, Joule Thomson cooler, or liquid nitrogen dewar.

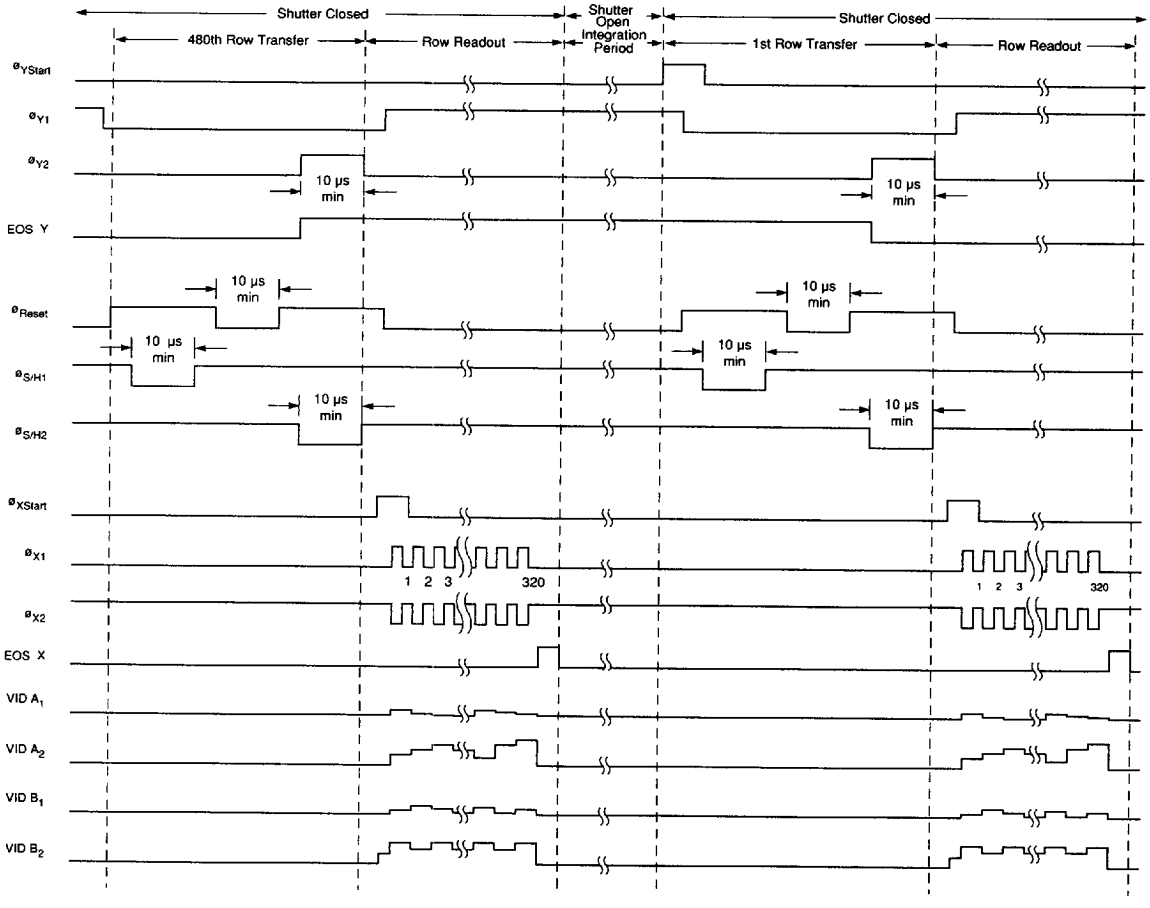

Figure 3. Timing Diagram with Double Correlated Sampling for Shuttered Operation

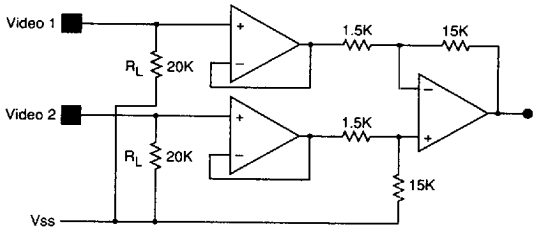

Figure 4. Differential to Single Video Output

Specifications

Table 1 gives typical capacitance values, Table 2 gives recommended operating conditions, and Table 3 shows typical device specifications for the RA0640A.

Table 1. Typical Capacitiance Values

Sym	Function	Capacitance	Units
ϕ_{XStart}	Horizontal start clock	3.5	pF
V_{DD}	Positive voltage supply		
ϕ_{SH1}	Sample-and-hold clock	33	pF
ϕ_{SH2}	Sample-and-hold clock	33	pF
ϕ_{RS}	Pre-amp reset clock	39	pF
FRG	Frame reset/exposure control clock		
ϕ_{YStart}	Vertical start clock	3.5	pF
ϕ_{1Y}	Vertical shift register clock	96	pF
ϕ_{2Y}	Vertical shift register clock	128	pF
EOS_Y	Vertical end-of-scan pulse	4.5	pF
V_{SS}	Substrate supply		
ϕ_{2XA}	Horizontal shift register clock	48	pF
ϕ_{1XA}	Horizontal shift register clock	48	pF
EOS_{XA}	Horizontal end-of-scan pulse	4.5	pF
VID_{1A}	Video output	100	pF
VID_{2A}	Video output	100	pF
$Bias_A$	Curren tsource amplifier bias	125	pF
V_{RefA}	Amplifier reference voltage	138	pF
V_{DD}	Positive voltage supply		
V_{RefB}	Amplifier reference voltage	138	pF
$Bias_B$	Current source amplifier bias	125	pF
VID_{2B}	Video output	100	pF
VID_{1B}	Video output	100	pF
EOS_{XB}	Horizontal end-of-scan pulse	4.5	pF
ϕ_{1XB}	Horizontal shift register clock	48	pF
ϕ_{2XB}	Horizontal shift register clock	48	pF

Table 2. Operating Conditions

Parameter		Sym	Low	Typ	High	Units
DC supply		V_{DD}	4.5	5	5.5	V DC
Substrate		V_{SS}		0		V DC
Substrate bias		V_{SUB}		V_{SS}		V DC
Reference bias		V_{Ref}	V_{SS} + 2	$(V_{DD}-V_{SS})/2$	V_{DD} - 2	V DC
Voltage bias[1]		V_{Bias}		V_{DD}-1.5		V DC
Readout clocks	High	ϕ_H	V_{DD} - 0.5	V_{DD}	V_{DD}	V
	Low		V_{SS}	V_{SS}	V_{SS} + 0.5	V
Row transfer clocks	High	ϕ_V	V_{DD} - 0.5	V_{DD}	V_{DD}	V
	Low		V_{SS}	V_{SS}	V_{SS} + 0.5	V
Reset gate clock	High	ϕ_{RG}	V_{DD}- 0.5	V_{DD}	V_{DD}	V
	Low		V_{SS}	V_{SS}	V_{SS} + 0.5	V

Note:
1 With external 100KΩ resistor to V_{SS}.

Table 3. Device Specifications

Conditions: 25°C, Data Rate 2 MHz, Integration time 170 ms. Voltage levels set to typical values shown in Table 1

Parameter	Sym	Min	Typ	Max	Units
Format			640 x 480		
Pixel size			50 x 50		µm
Imaging area			32 x 24		mm
Dynamic range	DR		1500:1		rms
Saturation voltage	V_{sat}		300	500	mV
Dark current	DL		0.1		nA/cm²
Saturation exposure [1]	Esat		.1		µJ/cm²
Responsivity	R		3		V/µJ/cm²
Photo response nonuniformity	PRNU		10	15	±%
Noise equivalent exposure	NEE		.07		nJ/cm²
DC power dissipation	D_{dc}		50		mW
Operating frequency	f_{clock}		1	5	MHz
Read out noise			200		µV (rms)

Note:
1 Light source is 2870°K tungsten lamp with a HA-11 visible spectrum filter.

Table 4. Absolute Maximum Ratings

Voltages: measured WRT substrate

	Min	Max
Storage temperature	-55°C	+85°C
Operating temperature	-55°K	50°C
Voltages: measured WRT substrate	0V	15V

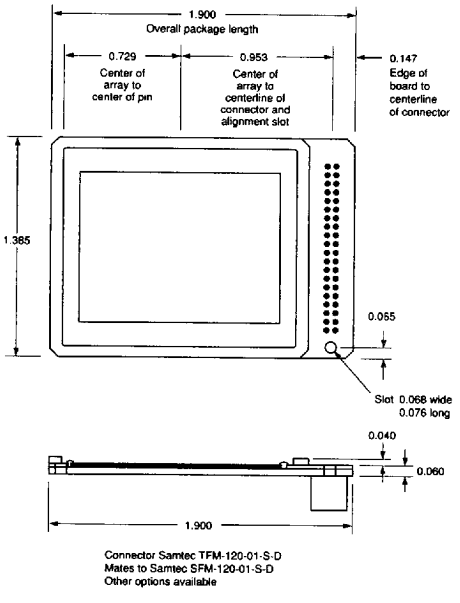

Figure 5. Package Dimensions

Ordering Information

Part Number
RA0640ANN-011