HY524800 Series
512K x 8-bit CMOS DRAM

DESCRIPTION

The HY524800 is the new generation and fast dynamic RAM organized 524,288 x 8-bits. The HY524800 utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY524800 to be packaged in a 350 mil 28 pin plastic SOJ.

The package size provides high system bit densities and is compatible with widely available automated-test equipments. System oriented-feature includes single power supply of 5V± 10% tolerence and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- **Low power dissipation**
  Max. CMOS standby 5.5mW
  Max. TTL standby 11.0mW
  Max. operating

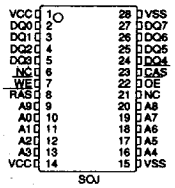
Speed	Power
70	742.5mW
80	632.5mW

- **Single power supply of 5V± 10%**
- **TTL compatible inputs and outputs**
- **Fast access time**

Speed	tRAC	tCAC	tPC
70	70ns	20ns	45ns
80	80ns	20ns	50ns

- **Fast page mode operation**
- **350 mil 28 pin SOJ**
- **Read-Modify-Write capability**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only refresh**
- **1024 refresh cycles / 16ms**

PIN CONNECTION

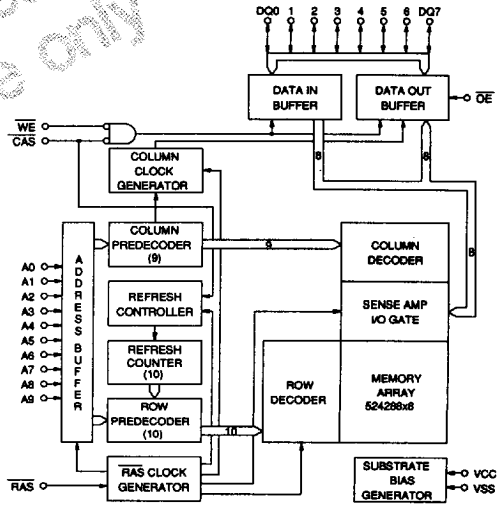


PIN DESCRIPTION

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
A0-A9*	Address Input
DQ0-DQ7	Data Input/Output
Vcc	Power (+ 5V)
Vss	Ground

*A9 is applied to Row address input only.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	–1.0 to 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	–1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature• Time	260• 10	°C• sec

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	V_{CC}+ 1.0	V
V_{IL}	Input Low Voltage	–1.0	-	0.8	V

NOTE : All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(T_A= 0°C to 70°C, V_{CC}= 5V± 10%, V_{SS}= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pins)	$V_{SS} \le V_{IN} \le$ 6.0V, All other pins not under test= V_{SS}		-10	10	µA	
I_{LO}	Output Leakage Current (High Impedance State)	$V_{SS} \le V_{OUT} \le$ 5.5V, $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-10	10	µA	
I_{CC1}	V_{CC} Supply Current, Operating	t_{RC}= t_{RC} (min.)	70 80	- -	135 115	mA	1,2,3
I_{CC2}	V_{CC} Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH},		-	2	mA	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-only refresh	t_{RC}= t_{RC} (min.)	70 80	- -	135 115	mA	1,3
I_{CC4}	V_{CC} Supply Current, Fast Page mode	t_{PC}= t_{PC} (min.)	70 80	- -	65 55	mA	1,2,3
I_{CC5}	V_{CC} Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS} \le V_{CC}$–0.2V		-	1	mA	
I_{CC6}	V_{CC} Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_{RC}= t_{RC} (min.)	70 80	- -	135 115	mA	1,3
V_{OL}	Output Low Voltage	I_{OL}= 4.2mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH}= –5mA		2.4	-	V	

NOTE :

1. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while $\overline{RAS}$= V_{IL} and $\overline{CAS}$= V_{IH}.

AC CHARACTERISTICS

(TA= 0°C to 70°C, Vcc= 5V± 10%, Vss= 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HY524800J				UNIT	NOTE
			-70		-80			
			MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	130	128K	150	128K	ns	1,2
2	tRWC	Read-Modify-Write Cycle Time	180	128K	205	128K	ns	1,2,10
3	tPC	Fast Page Mode Cycle Time	45	-	50	-	ns	2
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	90	-	100	-	ns	2,12
5	tRAC	Access Time from $\overline{RAS}$	-	70	-	80	ns	3,4,5
6	tCAC	Access Time from $\overline{CAS}$	-	25	-	20	ns	3,4,5
7	tAA	Access Time from Column Address	-	35	-	40	ns	4,5
8	tCPA	Access Time from $\overline{CAS}$ Precharge		-	40	-	45	ns5
9	tCLZ	$\overline{CAS}$ to Output Low Impedance	0	-	0	-	ns	
10	tOFF	Output Buffer Turn-off Delay	0	15	0	15	ns	7
11	tT	Transition Time (Rise and Fall)	3	50	3	50	ns	
12	tRP	$\overline{RAS}$ Precharge Time	50	-	60	-	ns	
13	tRAS	$\overline{RAS}$ Pulse Width	70	16K	80	16K	ns	1,2
14	tRASP	$\overline{RAS}$ Pulse Width (Fast Page Mode)	120	16K	135	16K	ns	1,2,10
15	tRSH	$\overline{RAS}$ Hold Time	20	-	20	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	70	-	80	-	ns	
17	tCAS	$\overline{CAS}$ Pulse Width	20	10K	20	10K	ns	
18	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	50	20	60	ns	3
19	tRAD	$\overline{RAS}$ to Column Address Delay Time	15	-	15	-	ns	6
20	tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	ns	
21	tCP	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	9
22	tASR	Row Address Set-up Time	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	ns	
26	tAR	Column Address Hold Time from $\overline{RAS}$	50	-	55	-	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	ns	
30	tRRH	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	ns	
31	tWCH	Write Command Hold Time	15	-	15	-	ns	
32	tWCR	Write Command Hold Time from $\overline{RAS}$	55	-	60	-	ns	
33	tWP	Write Command Pulse Width	15	-	15	-	ns	
34	tRWL	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	ns	
35	tCWL	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	ns	8
37	tDH	Data-In Hold Time	15	-	15	-	ns	8
38	tDHR	Data-In Hold Time Referenced to $\overline{RAS}$	55	-	60	-	ns	
39	tREF	Refresh Period (1024 cycles)	-	16	-	16	ms	
40	tWCS	Write Command Set-up Time	0	-	0	-	ns	

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY524800J				UNIT	NOTE
			-70		-80			
			MIN.	MAX.	MIN.	MAX.		
41	tCWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	-	50	-	ns	10
42	tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time	95		110	-	ns	10
43	tAWD	Column Address to $\overline{WE}$ Delay Time	60	-	70	-	ns	10
44	tCSR	$\overline{CAS}$ Set-up Time (CBR Cycle)	10	-	10	-	ns	9
45	tCHR	$\overline{CAS}$ Hold Time (CBR Cycle)	15	-	20	-	ns	
46	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	ns	
47	tOEH	$\overline{OE}$ Command Hold Time	15	-	15	-	ns	
48	tROH	$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	10	-	10	-	ns	
49	tOEA	$\overline{OE}$ Access Time	-	20	-	20	ns	4,5
50	tOED	$\overline{OE}$ to Data Delay	15	-	15	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from $\overline{OE}$	-	15	-	15	ns	7
52	tWRP	$\overline{WE}$ to $\overline{RAS}$ Precharge Time (CBR Cycle)	5	-	5	-	ns	9
53	tWRH	$\overline{WE}$ to $\overline{RAS}$ Hold Time (CBR Cycle)	10	-	10	-	ns	9

NOTE :

1. 1024 refreshes are required every 16ms. A burst of eight consecutive refreshes are allowed to keep t_{RAS}= 16μs average. A maximum of 128μs between refreshes is allowed, however 16ms retention must be met.
2. All AC timings assume t_T(max.)= 5ns. If the actual t_T is greater than t_T(max.), then the cycle times need to be greater than that specified by the amount each transition exceeds t_T(max.). HY524800 will support a t_T up to 50ns. The transition time is defined between the V_{IH} and V_{IL}. All timings are referenced to a V_{IL} or V_{IH}.
3. t_{RCD}(max.) is specified as a reference point only. If t_{RCD}> t_{RCD}(max), then this parameter increased by the amount t_{RCD} exceeds t_{RCD}(max.)
4. t_{RAC}, t_{CAC}, t_{AA} and t_{OEA} must be satisfied to guarantee access. Please check that all parameters are met for your application.
5. Access assumes a load equivalent to 100pF.
6. t_{RAD} is specified as a reference point only. If t_{RAD}> t_{RAC}-t_{AA}, then the access is increased by the difference.
7. This parameter defines the time at which the output achieves the open circuit and is not referenced to the output voltage levels.
8. Data in set-up and holds are measured from the later of falling signal $\overline{CAS}$ or $\overline{WE}$.
9. t_{CP}, t_{CSR}, t_{WRP}, t_{WRH} all need to be valid for CBR users.
10. A 5ns delta is used between data reaching high impedance and having valid data in for these numbers.

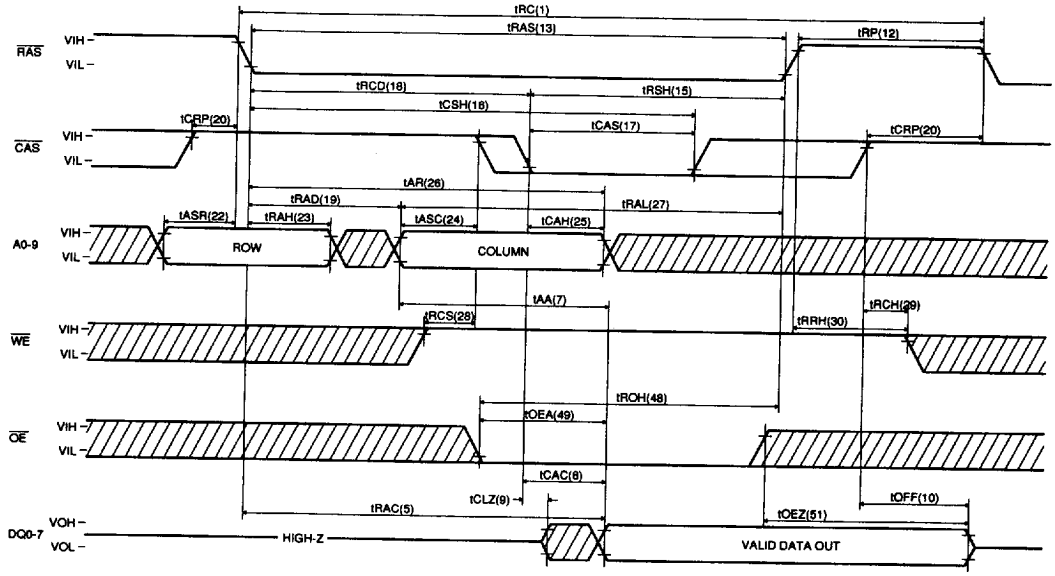
CAPACITANCE

(T_A= 25°C, V_{CC}= 5V± 10%, V_{SS}= 0V, f= 1MHz, unless otherwise noted.)

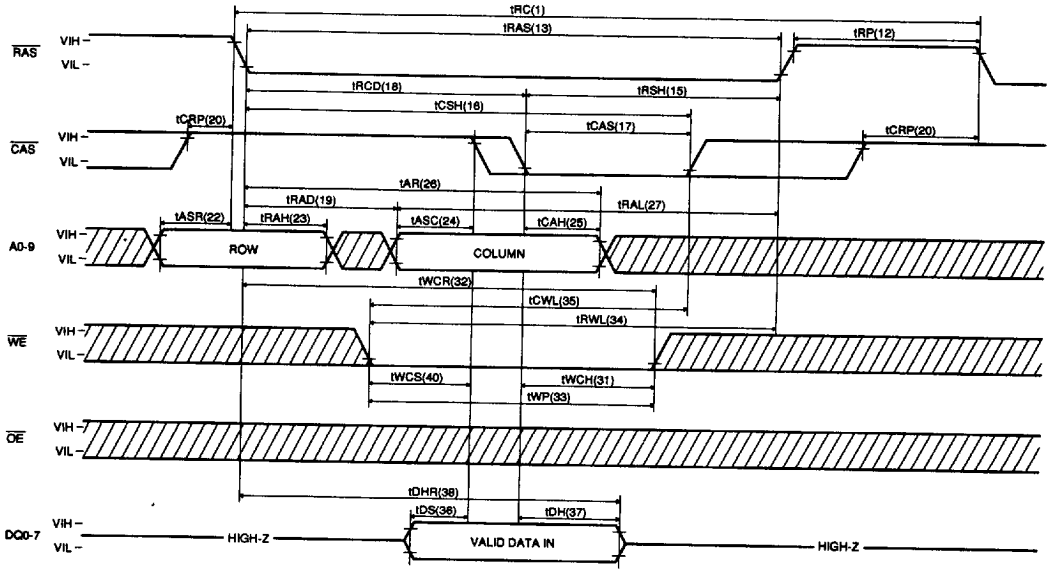
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A9, D)	-	5	pF
C_{IN2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	-	5	pF
C_{OUT}	Output Capacitance (Q)	-	8	pF

TIMING DIAGRAM

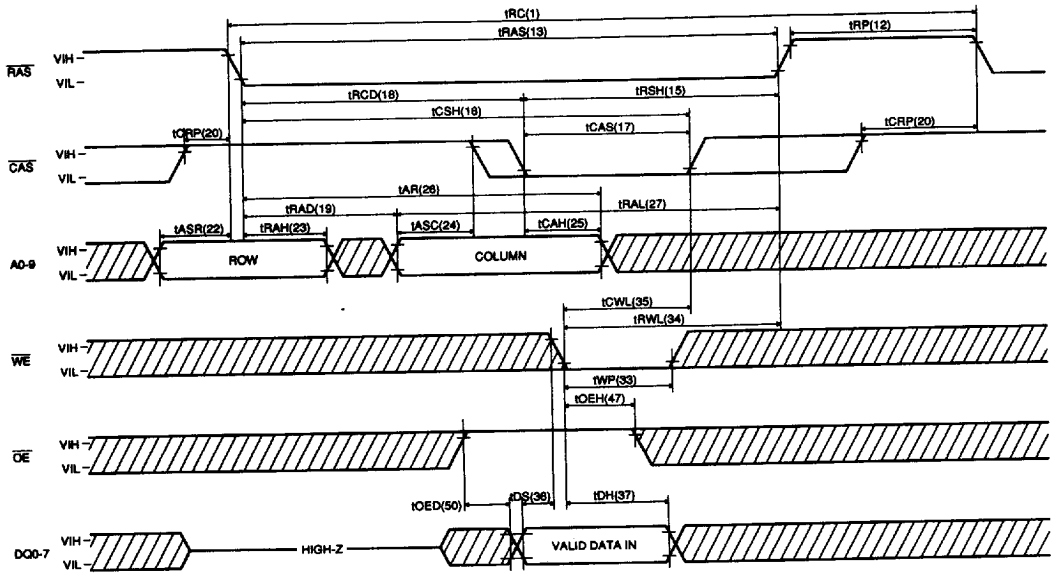
READ CYCLE



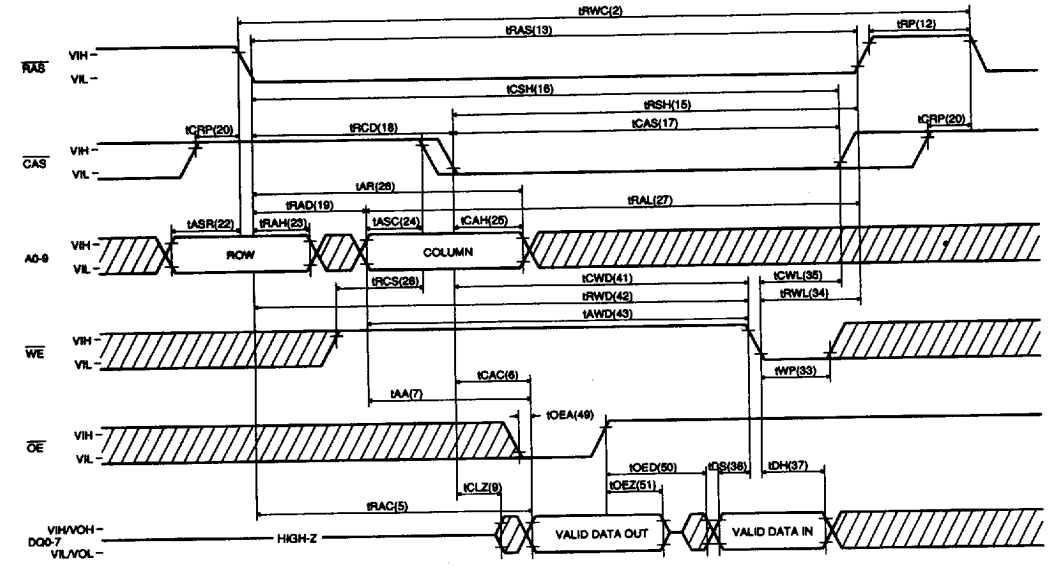
EARLY WRITE CYCLE



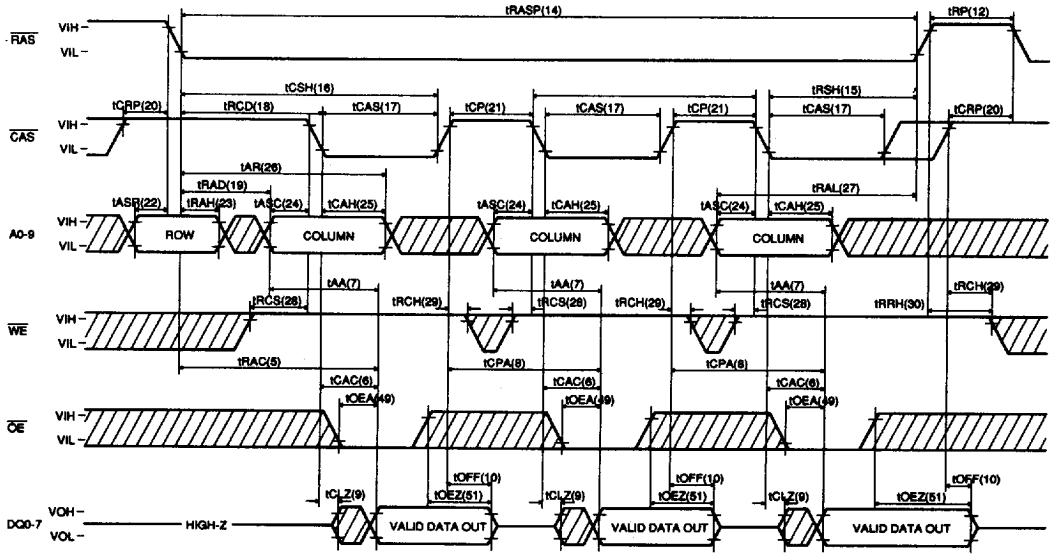
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



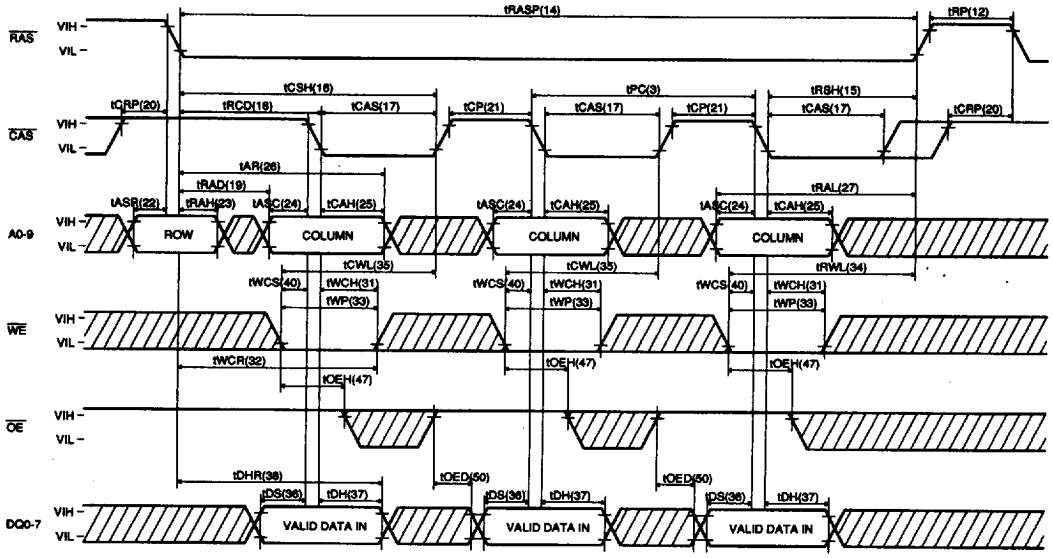
READ-MODIFY-WRITE CYCLE



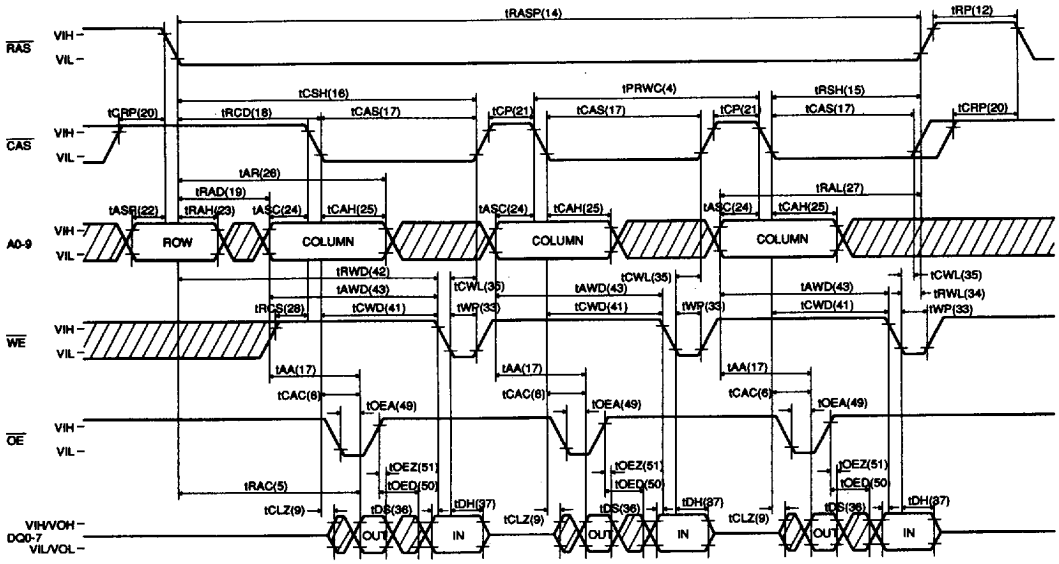
FAST PAGE MODE READ CYCLE



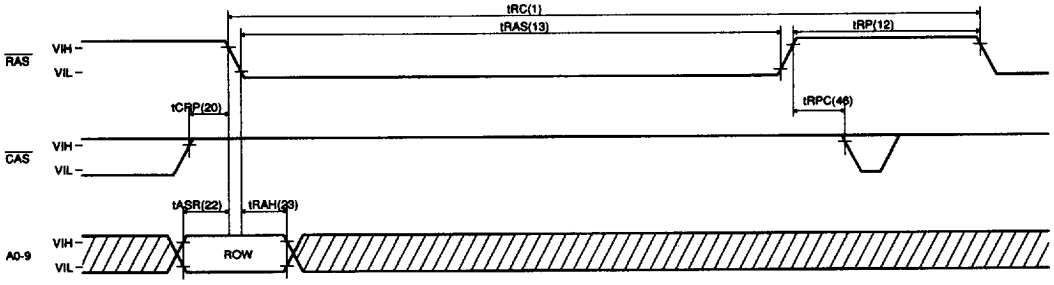
FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

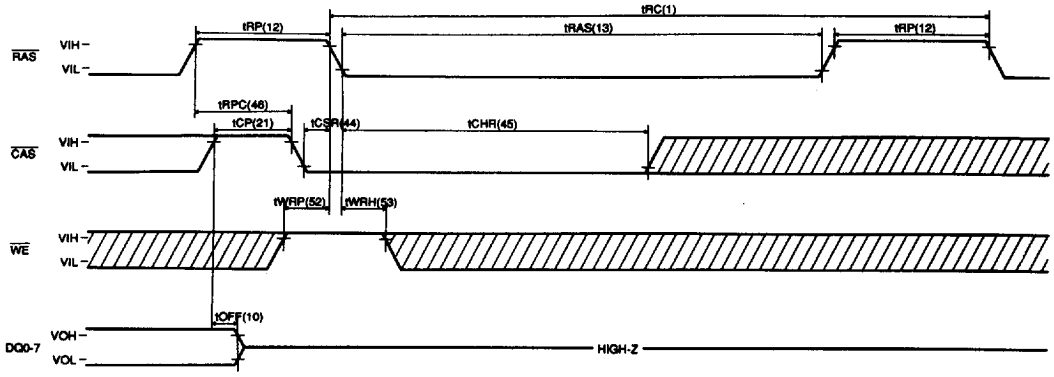


RAS-ONLY REFRESH CYCLE



NOTE : $\overline{OE}$ and $\overline{WE}$ = "H" or "L"

CAS-BEFORE-RAS REFRESH CYCLE



NOTE : A0-9 and $\overline{OE}$ = "H" or "L"

DEVICE OPERATION

POWER ON, INITIALIZATION, POWER OFF

After Vcc stabilizes, a pause of at least 500 microseconds is required before initialization begin. During this interval, $\overline{RAS}$ must be inactive(V_{IH}). A minimum of 8 cycles are required to initialized the device, these must be either $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, whose t_{RP} must be greater than 70ns. After the initialization cycles, the device is ready for normal use.

PAGE MODE OPERATION

The standard page mode for $\overline{CAS}$-before-$\overline{RAS}$ and $\overline{RAS}$-only refresh, early and late-write, read and Read-Modity-Write cycles are supported.

ADDRESS CONTROL

The row address is trapped with the falling edge of $\overline{RAS}$, which is common for all modes of operation. This selects the word line to be used during the $\overline{RAS}$ cycle. The W/L selected cannot be changed without $\overline{RAS}$ going inactive. The column address(A0-A8) is trapped with the falling edge of $\overline{CAS}$, for both the Read and Write operations. Each falling $\overline{CAS}$ allows a new Read or Write operation to occur on a selected new bit address on the same W/L. $\overline{CAS}$ cycles may continue with new random addresses trapped each time $\overline{CAS}$ falls, up to the limit of the $\overline{RAS}$ active time-t_{RAS}. The $\overline{CAS}$ pulse must rise past the V_{IH} value and remain at a high level for a specified time. Only one Write operation can occur while $\overline{CAS}$ is low. The device's access is impacted by active $\overline{RAS}$, active $\overline{CAS}$, active $\overline{OE}$, as well as valid address and inactive $\overline{CAS}$. All conditions must be met in order to have a valid access. Therefore the set-up time for column address may impact the device's access.

READ/WRITE CONTROL

The state of the $\overline{WE}$ pin at $\overline{CAS}$ falling time determines the type of cycle the device will start. If $\overline{WE}$ is low when $\overline{CAS}$ falls, an early write operation is initiated. Because the device knows that a write operation has been initiated, the off-chip drivers will remain in high impedance for the entire $\overline{CAS}$ cycle and only allows one write operation for each $\overline{CAS}$ cycle. If $\overline{WE}$ is high when $\overline{CAS}$ falls, a Read operation is performed, and the $\overline{OE}$ pin will control the OCD impedance. The $\overline{OE}$ pin is independent of $\overline{CAS}$, but does have an access requirement. $\overline{CAS}$ and $\overline{WE}$ must not change state until data out is read. If $\overline{WE}$ does fall while $\overline{CAS}$ is still low, a Read-Modify-Write or Late-Write cycle will be initiated. In this case, the $\overline{OE}$ pin will control the OCD impedance. When $\overline{WE}$ falls, it will trap Data-In information for the Write operation. The $\overline{OE}$ pin must be used for this cycle to guarantee correct "hand shaking" on the DQ pin for Data-Out and Data-In control. Until Data-Out is read and Data-In is set up, Write must not go low. In this case, the Data In will be written on the same Column address which was trapped when $\overline{CAS}$ fall. $\overline{CAS}$ must remain low for a specified time after $\overline{WE}$ is low. and can not start another cycle until after a t_{RMW} cycle time has passed. The customer can mix the above cycle types as long as all other timings are obeyed.

DATA IN CONTROL

Input data are is trapped when the write cycle is initiated. For an early write operation, $\overline{CAS}$ will be the trapping signal. During a late write or Read-Modify-Write operation, $\overline{WE}$ will be the trapping signal.

IMPEDANCE CONTROL

The following signals are used to control the impedance of the OCDs ; $\overline{OE}$ pin, $\overline{WE}$ pin, $\overline{RAS}$ pin, and $\overline{CAS}$ pin. All pins must be in there proper state in order to drive Data Out. With the $\overline{OE}$ pin high, the OCDs are turned off and will maintain hi-impedance. Thus Data Out can be turned "off" by returning the $\overline{OE}$ pin to hi-level.
$\overline{OE}$ pin going to low will allow the output driver to be turned "on", but only if the device is doing a Read operation ($\overline{WE}$ pin high) and both the $\overline{CAS}$ and $\overline{RAS}$ pins are still low. If $\overline{CAS}$ never falls($\overline{RAS}$-Only Refresh), the device will also maintain hi-impedance. Data-Out can be turned "off" by returning the $\overline{CAS}$ pin to hi-level. If $\overline{WE}$ is low when $\overline{CAS}$ falls, the device will maintain hi-impedance. Data-Out will not be turned "off" by returning the $\overline{RAS}$ pin to a hi-level, but when $\overline{RAS}$ falls to start another cycle, the device will return to a hi-impedance even if $\overline{CAS}$ had remained low. Thus Hidden-Refresh is not supported.

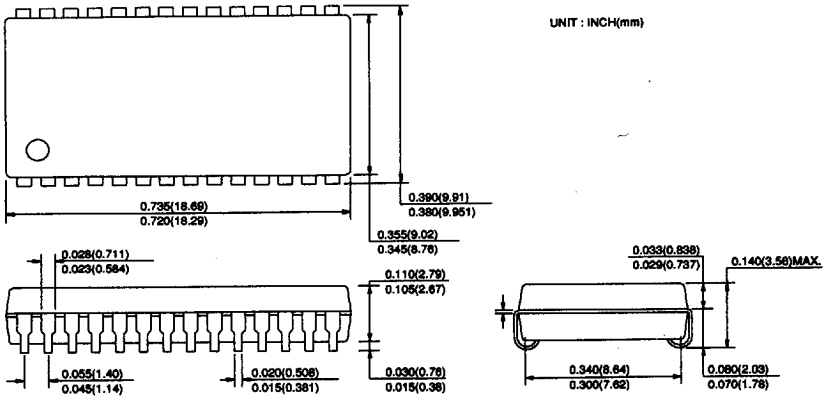
REFRESH CYCLE

Because 512K x 8 bits are a dynamic memory cells (data is represented by charge stored on a capacitor), each cell must be refreshed periodically to replace leakage. Refreshing the entire chip requires sequence through all 1024 row addresses. This must be done within each 16ms refresh interval. Two refresh methods are provided.
A $\overline{RAS}$-Only Refresh used a $\overline{RAS}$ select with $\overline{CAS}$ high. The selected row address (A0-A9) must be provided to the device. A $\overline{CAS}$-Before-$\overline{RAS}$ Refresh capability is also provided. If $\overline{CAS}$ is low, $\overline{RAS}$ is pulled low to initiate the Refresh, an on-chip Row Address Counter(RAC) will provide the next row address for the Refresh.
No external addresses are used.

NOTE :
1.Refresh occurs whenever $\overline{RAS}$ is selected ; eg, read or write.
2. If both $\overline{CAS}$ & $\overline{WE}$ are low when $\overline{RAS}$ becomes active(low), the device will be forced into a test mode.
Since some test modes may cause physical damage to the device, the above sequence is not allowed.
Test modes are cleared by $\overline{RAS}$-only and $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.

PACKAGE INFORMATION

350 mil 28 pin Small Outline J-form Package (J)



ORDERING INFORMATION

PART NO	SPEED	POWER	PACKAGE
HY524800J	70/80		SOJ