AT40495
Addendum to AT40493

The AT40495 system and cache controller functions exactly like the AT40493 (see AT40493 data sheet) with the following exceptions:

- The AT40495 supports one or two banks of cache SRAM and does not require the use of buffers in the data path. Thus the even and odd bank output enables (BEOE# and BOOE#, respectively) are not asserted during CPU or DMA write cycles.
- The TLB# (pin 110) signal on the AT40493 is redefined as BEA2# (cache even bank address bit 2).
- The AT40495 supports 2-1-1-1 cache burst mode for 16 MHz, 20 MHz and 25 MHz operation and 3-2-2-2- cache burst mode for 33 MHz and 50 MHz operation.

Ordering Information

CPU Clock (MHz)	Power Supply	Ordering Code	Package	Operation Range
25	5V ± 5%	AT40495-25 AT40392-25	160Q 160Q	Commercial (0°C to 70°C)
33	5V ± 5%	AT40495-33 AT40392-33	160Q 160Q	Commercial (0°C to 70°C)
50	5V ± 5%	AT40495-50 AT40392-50	160Q 160Q	Commercial (0°C to 70°C)

Package Type	
160Q	160 Lead, Plastic Gull Wing Quad Flat Package (PQFP)