



12.5 MIPS DSP Microprocessor

ADSP-2100/ADSP-2100A

1.1 Scope.

ANALOG DEVICES INC

65E D

This specification covers the detail requirements for a monolithic CMOS 16-bit fixed-point DSP microprocessor.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	ADSP-2100S(X)/883B
-2	ADSP-2100AS(X)/883B
-3	ADSP-2100AT(X)/883B
-4	ADSP-2100AU(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X) Package Description

G	G-100A	100-Lead Pin Grid Array
Z	F-100A	100-Contact Ceramic Quad Flat Pack

1.3 Absolute Maximum Ratings.

Supply Voltage		-0.3 V to 7 V
Input Voltage		-0.3 V to $V_{DD} + 0.3$ V
Output Voltage		-0.3 V to $V_{DD} + 0.3$ V
Operating Temperature Range (Ambient)		-55°C to +125°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering 10 sec)		+300°C
Maximum Power Dissipation		0.750 W

1.5 Thermal Characteristics.

Maximum Thermal Resistance θ_{JC} : see MIL-M-38510, Appendix C.

ADSP-2100/ADSP-2100A—SPECIFICATIONS

Table 1.

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Digital Input High Voltage ²	V _{IHI}	-1, 2, 3, 4	2.0	2.2	2.2			V _{DD} = max	V min
Digital Input High Voltage at CLKIN	V _{IH2}	-2, 3, 4	2.2	2.4	2.4			V _{DD} = max	V min
Digital Input Low Voltage ²	V _{IL}	-1, 2, 3, 4	0.8	0.8	0.8			V _{DD} = min	V max
Digital Output High Voltage ³	V _{OH}	-1, 2, 3, 4	2.4	2.4	2.4			V _{DD} = max I _{OH} = -1 mA	V min
Digital Output Low Voltage ³	V _{OL}	-1, 2, 3, 4	0.4	0.6	0.6			V _{DD} = min I _{OL} = +4 mA	V max
Digital Input High Current ⁴	I _{IH}	-1, 2, 3, 4	10	10	10			V _{DD} = max V _{IN} = max	μA max
Digital Input Low Current ⁴	I _{IL}	-1, 2, 3, 4	10	10	10			V _{DD} = max V _{IN} = 0.0 V	μA max
Three-State Leakage ⁵ Current High	I _{OZH}	-1, 2, 3, 4	10	10	10			V _{DD} = max V _{IN} = max ⁸	μA max
Three-State Leakage ⁶ Current Low	I _{OZL1}	-1, 2, 3, 4	10	10	10			V _{DD} = max V _{IN} = 0.0 V ⁸	μA max
Three-State Pullup Current ⁷	I _{OZL2}	-1 -2, 3, 4	150 180	150 180	150 180			V _{DD} = max V _{IN} = 0.0 V ⁸	μA max
Supply Current, Dynamic	I _{DD1}	-1 -2 -3 -4	90 150	100 130 180 200	100 130 180 200			V _{DD} = max Max Clock Rate ⁹	mA max
Supply Current, Power-Down ¹⁰	I _{DD2}	-1 -2, 3, 4	10 10	15 10	15 10			V _{DD} = max V _{IN} = 0.0 V ^{7, 8}	mA max
CLKIN Period	t ¹²	-1 -2 -3 -4	40.5 24.4 20 20			40.5 30.5 24.4 20	40.5 30.5 24.4 20	A	ns min
CLKIN Width Low	2	-1 -2 -3 -4	11 7 4 4			11 8 7 4	11 8 7 4	A	ns min
CLKIN Width High	3	-1 -2 -3 -4	18 9 8 8			18 12 9 8	18 12 9 8	A	ns min
CLKIN Low (3-4) to CLKOUT Low	4	-1 -2 -3 -4	13 34 24 22 22			11 34 29 24 22	11 34 29 24 22	B	ns min ns max
CLKIN LOW (7-8) to CLKOUT High	5	-1 -2 -3 -4	6 24 20 18 18			5 24 20 20 18	5 24 20 20 18	B	ns min ns max

Table 1. (Continued)

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
CLKOUT Width Low	6	-1 -2 -3 -4	60 36 28 28			60 45 36 28	60 45 36 28	A	ns min
RESET Low to CLKIN High	7	-1, 2, 3, 4	2			2	2	B	ns min
CLKIN High to RESET High	8	-1 -2 -3 -4	36 6 20 6 16 4 16 4			36 6 26 6 20 4 16 4	36 6 26 6 20 4 16 4	B	ns max ns min ns max ns min ns max ns min ns max ns min
RESET Width Low	9	-1 -2 -3 -4	162 98 80 80			170 128 98 80	170 128 98 80	A	ns min
HALT Valid to CLKIN Low (3-4)	10	-1 -2, 3, 4	0 2			0 2	0 2	B	ns min
CLKIN Low (3-4) to HALT Invalid	11	-1 -2 -3 -4	12 10 8 8			12 10 10 8	12 10 10 8	B	ns min
CLKIN Low (7-8) to TRAP Valid	12	-1 -2 -3 -4	25 18 16 16			25 20 18 16	25 20 18 16	B	ns max
CLKIN Low (7-8) to IRQ Valid	13	-1 -2, 3, 4	2 1			1 1	1 1	B	ns max
CLKIN Low (7-8) to IRQ Invalid	14	-1 -2 -3, 4	21 14 14			21 17 14	21 17 14	B	ns min
BR Valid to CLKIN Low (3-4)	15	-1 -2 -3, 4	1 4 4			1 1 4	1 1 4	B	ns min
CLKIN Low (3-4) to BR Invalid	16	-1 -2 -3, 4	10 4 4			10 7 4	10 7 4	B	ns min
CLKIN Low (3-4) to $\overline{BG}$ Low	17	-1 -2 -3 -4	38 26 24 24			38 30 26 24	38 30 26 24	B	ns max

Table 1. (Continued)

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
CLKIN Low (7-8) to $\overline{BG}$ High	18	-1 -2 -3 -4	31 24 20 20			31 25 24 20	31 25 24 20	B	ns max
$\overline{BG}$ Low to xMxx Disable	19 ¹³	-1 -2 -3, 4	22 16 16			22 17 16	22 17 16	D	ns max
xMxx Enable to $\overline{BG}$ High	20 ¹³	-1 -2 -3 -4	12 10 8 8			12 10 10 8	12 10 10 8	F	ns max
$\overline{BR}$ Low to $\overline{BG}$ Low During Reset	21	-1 -2 -3 -4	28 18 16 16			28 23 18 16	28 23 18 16	A	ns max
$\overline{BR}$ High to $\overline{BG}$ High During Reset	22	-1 -2 -3 -4	21 16 14 14			21 18 16 14	21 18 16 14	A	ns max
PMRD Width Low	31	-1 -2 -3 -4	60 36 28 28			60 45 36 28	60 45 36 28	A	ns min
PMA Valid to PMRD Low	32	-1 -2 -3 -4	18 6 4 4			18 14 6 4	18 14 6 4	A	ns min
PMRD High to PMA Invalid	33	-1 -2 -3 -4	20 8 6 6			20 10 8 6	20 10 8 6	A	ns min
PMDA Valid to PMRD Low	34	-1 -2 -3 -4	41 20 18 18			41 24 20 15	41 24 20 15	A	ns min
PMRD High to PMDA Invalid	35	-1 -2 -3, 4	23 10 10			22 12 10	22 12 10	A	ns min
PMS Valid to PMRD Low	36	-1 -2 -3 -4	55 32 26 26			55 40 32 26	55 40 32 26	A	ns min

Table 1. (Continued)

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
PMRD High to PMS Invalid	37	-1	16			16	16	A	ns min
		-2	8			8	8		
		-3	6			8	8		
		-4	6			6	6		
PMWR Width Low	40	-1	60			60	60	A	ns min
		-2	36			45	45		
		-3	28			36	36		
		-4	28			28	28		
PMA Valid to PMWR Low	41	-1	16			16	16	A	ns min
		-2	8			12	12		
		-3	4			8	8		
		-4	4			4	4		
PMWR High to PMA Invalid	42	-1	19			19	19	A	ns min
		-2	8			10	10		
		-3	6			8	8		
		-4	6			6	6		
PMDA Valid to PMWR Low	43	-1	39			39	39	A	ns min
		-2	20			28	28		
		-3	16			20	20		
		-4	15			16	16		
PMWR High to PMDA Invalid	44	-1	20			21	21	A	ns min
		-2	10			12	12		
		-3	8			10	10		
		-4	8			8	8		
PMS Valid to PMWR Low	45	-1	54			54	54	A	ns min
		-2	32			40	40		
		-3	26			32	32		
		-4	26			26	26		
PMWR High to PMS Invalid	46	-1	15			14	14	A	ns min
		-2	6			8	8		
		-3	4			6	6		
		-4	4			4	4		
PMWR Low to PMD Out Enable	51	-1	15			15	15	F	ns min
		-2	8			8	8		
		-3	6			8	8		
		-4	6			6	6		
PMWR High to PMD Out Disable	52	-1	43			43	43	D	ns max
		-2	32			38	38		
		-3	29			32	32		
		-4	29			29	29		
PMWR Low to PMD Out Valid	53	-1	40			40	40	A	ns max
		-2	29			32	32		
		-3	26			29	29		
		-4	26			26	26		

Table 1. (Continued)

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
PMWR High to PMD Out Invalid	54	-1	23			21	21	A	ns min
		-2	10			12	12		
		-3	8			10	10		
		-4	8			8	8		
PMD Out Valid to to PMWR High	55	-1	33			33	33	A	ns min
		-2	16			25	25		
		-3	13			16	16		
		-4	13			13	13		
PMRD Low to PMD Input Valid	58	-1	45			45	45	A	ns max
		-2	28			33	33		
		-3	20			28	28		
		-4	20			18	18		
PMA Valid to PMD Input Valid	59	-1	57			57	57	A	ns max
		-2	46			50	50		
		-3	32			46	46		
		-4	32			32	32		
PMS Valid to PMD Input Valid	60	-1	90			90	90	A	ns max
		-2	50			65	65		
		-3	45			50	50		
		-4	45			35	35		
DMRD Width Low	67	-1	60			60	60	A	ns min
		-2	36			45	45		
		-3	28			36	36		
		-4	28			28	28		
DMA Valid to DMRD Low	68	-1	21			21	21	A	ns min
		-2	6			14	14		
		-3	4			6	6		
		-4	4			4	4		
DMRD High to DMA Invalid	69	-1	19			19	19	A	ns min
		-2	8			10	10		
		-3	6			8	8		
		-4	6			6	6		
DMS Valid to DMRD Low	70	-1	35			35	35	A	ns min
		-2	18			27	27		
		-3	14			18	18		
		-4	14			14	14		
DMRD High to DMS Invalid	71	-1	22			21	21	A	ns min
		-2	8			10	10		
		-3	6			8	8		
		-4	6			6	6		

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Table 1. (Continued)

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
DMRD Low to DMACK Valid	74	-1	31 0			31 0	31 0	A	ns max ns min
		-2	16 0			21 0	21 0		ns max ns min
		-3	10 0			16 0	16 0		ns max ns min
		-4	10 0			10 0	10 0		ns max ns min
DMA Valid to DMACK Valid	75	-1	57 0			57 0	57 0	A	ns max ns min
		-2	30 0			42 0	42 0		ns max ns min
		-3	20 0			30 0	30 0		ns max ns min
		-4	20 0			20 0	20 0		ns max ns min
DMWR Width Low	78	-1	60			60	60	A	ns min
		-2	36			45	45		
		-3	28			36	36		
		-4	28			28	28		
DMA Valid to DMWR Low	79	-1	24			24	24	A	ns min
		-2	8			17	17		
		-3	4			8	8		
		-4	4			4	4		
DMWR High to DMA Invalid	80	-1	20			19	19	A	ns min
		-2	8			10	10		
		-3	6			8	8		
		-4	6			6	6		
DMS Valid to DMWR Low	81	-1	37			37	37	A	ns min
		-2	20			28	28		
		-3	16			20	20		
		-4	16			16	16		
DMWR High to DMS Invalid	82	-1	22			22	22	A	ns min
		-2	6			8	8		
		-3	4			6	6		
		-4	4			4	4		
DMWR Low to DMD Out Enable	87	-1	14			14	14	F	ns min
		-2	8			8	8		
		-3	6			8	8		
		-4	6			6	6		
DMWR High to DMD Out Disable	88	-1	40			40	40	D	ns max
		-2	32			38	38		
		-3	29			32	32		
		-4	29			29	29		

Table 1. (Continued)

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
DMWR Low to DMD Out Valid	89	-1	38			38	38	A	ns max
		-2	29			32	32		
		-3	26			29	29		
		-4	26			26	26		
DMWR High to DMD Out Invalid	90	-1	21			19	19	A	ns min
		-2	10			12	12		
		-3	8			10	10		
		-4	8			8	8		
DMD Out Valid to DMWR High	91	-1	33			33	33	A	ns min
		-2	18			25	25		
		-3	13			16	16		
		-4	13			13	13		
DMRD Low to DMD Input Valid	94	-1	57			55	55	A	ns max
		-2	30			37	37		
		-3	20			28	28		
		-4	20			18	18		
DMA Valid to DMD Input Valid	95	-1	82			79	79	A	ns max
		-2	48			59	59		
		-3	32			46	46		
		-4	32			32	32		
DMS Valid to DMD Input Valid	96	-1	96			96	96	A	ns max
		-2	52			67	67		
		-3	45			50	50		
		-4	45			35	35		
PMRD High to PMD Input Valid	97	-1, 2, 3, 4	0			0	0	A	ns min
DMRD High to DMD Input Invalid	98	-1, 2, 3, 4	0			0	0	A	ns min
DMWR Low to DMACK Valid	99	-1	31 0			31 0	31 0	A	ns max ns min
		-2	16 0			20 0	20 0		ns max ns min
		-3	10 0			16 0	16 0		ns max ns min
		-4	10 0			10 0	10 0		ns max ns min
CLKOUT High to DMACK Invalid	103	-1	60 0			60 0	60 0	A	ns max ns min
		-2	36 0			45 0	45 0		ns max ns min
		-3	28 0			36 0	36 0		ns max ns min
		-4	28 0			28 0	28 0		ns max ns min

Table 1. (Continued)

NOTES

¹T_A = 25°C; V_{DD} = +4.5 V to +5.5 V max (unless otherwise noted).²Applies to pins: PMD₀₋₂₃, DMD₀₋₁₅, $\overline{\text{BR}}$, $\overline{\text{IRQ}}_{0-3}$, DMACK, $\overline{\text{RESET}}$, $\overline{\text{HALT}}$, (48 input pins for ADSP-2100A). Includes CLKIN for ADSP-2100 (49 input pins).³Applies to pins: PMA₀₋₁₃, $\overline{\text{PMS}}$, PMD₀₋₂₃, $\overline{\text{PMRD}}$, $\overline{\text{PMWR}}$, PMDA, $\overline{\text{BG}}$, DMA₀₋₁₃, $\overline{\text{DMS}}$, DMD₀₋₁₅, $\overline{\text{DMRD}}$, $\overline{\text{DMWR}}$, TRAP, CLKOUT (78 output pins).⁴Applies to pins: $\overline{\text{BR}}$, $\overline{\text{IRQ}}_{0-3}$, DMACK, $\overline{\text{RESET}}$, $\overline{\text{HALT}}$, CLKIN (9 input only pins).⁵Applies to pins: PMA₀₋₁₃, $\overline{\text{PMS}}$, PMD₀₋₂₃, $\overline{\text{PMRD}}$, $\overline{\text{PMWR}}$, PMDA, DMA₀₋₁₃, $\overline{\text{DMS}}$, DMD₀₋₁₅, $\overline{\text{DMRD}}$, $\overline{\text{DMWR}}$ (75 tristateable pins).⁶Applies to pins: PMS₀₋₁₃, PMDA, DMA₀₋₁₃ (29 tristateable pins w/o pullup).⁷Applies to pins: PMD₀₋₂₃, $\overline{\text{PMS}}$, $\overline{\text{PMRD}}$, $\overline{\text{PMWR}}$, DMD₀₋₁₅, $\overline{\text{DMS}}$, $\overline{\text{DMRD}}$, $\overline{\text{DMWR}}$ (46 tristateable pins w/pullup).⁸Additional Test Conditions: V_{IN} = 0 V on $\overline{\text{BR}}$ and $\overline{\text{RESET}}$, CLKIN active forces tristate condition.⁹Additional Test Conditions: Outputs loaded TTL loads w/100 pF capacitance, V_{IH} = 2.4 V, V_{IL} = 0.4 V, clock rate = max.¹⁰"Power-down" refers to an idle state. While the processor does not have any special standby or low power mode, these conditions represent the lowest power consumption state.¹¹Input levels are GND and +3.0 V; V_{DD} = +4.5 V, and timing transitions per Figures 1 through 10b, measured at 1.5 V.¹²Rise and fall times ≤ 4 ns for ADSP-2100A, 5 ns for ADSP-2100.¹³"xMxx" refers to PMA₀₋₁₃, $\overline{\text{PMS}}$, $\overline{\text{PMRD}}$, $\overline{\text{PMWR}}$, PMDA, DMA₀₋₁₃, $\overline{\text{DMS}}$, $\overline{\text{DMRD}}$ and $\overline{\text{DMWR}}$.

TEST CODES

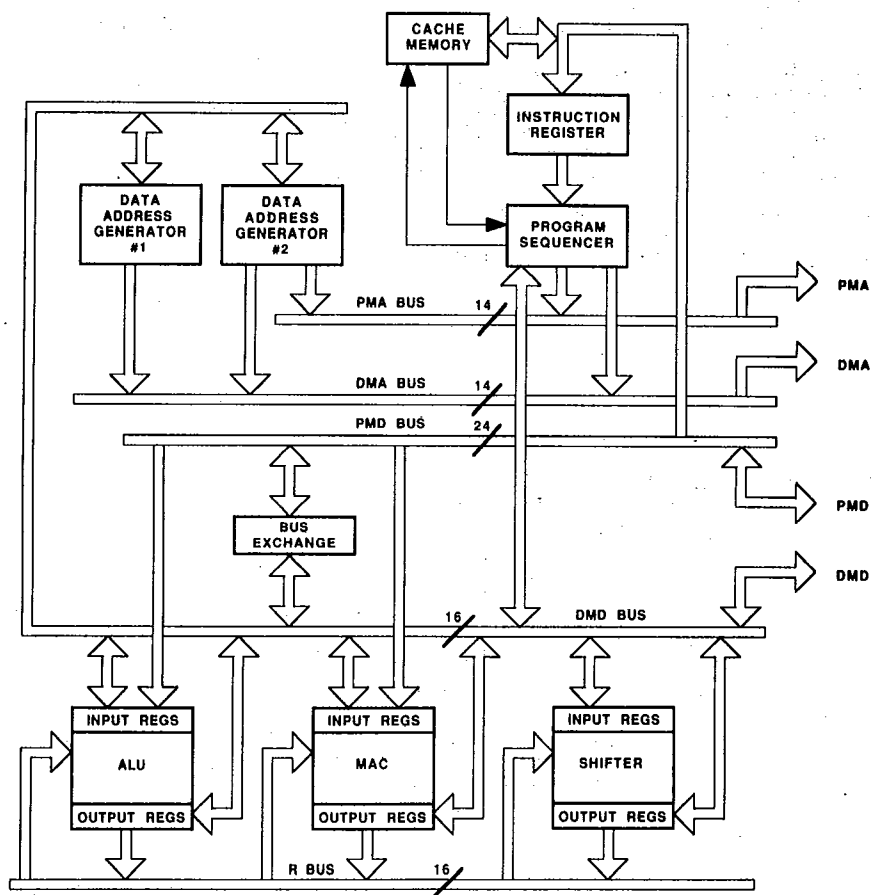
Code	Test Type	Level Reference
A	Inputs, Outputs	Low = 0.8V, High = 2.0V
B	CLKIN to/from	1.5V
	Inputs, Outputs	Low = 0.8V, High = 2.0V
D	Output to	Low = 0.8V, High = 2.0V
	Output Disable	Low = V _{OH} + 0.5V, High = V _{OH} - 0.5V
F	Output to/from	Low = 0.8V, High = 2.0V
	Output Enable	Low = VT - 0.1V, High = VT + 0.1V

VT = 1.5 V, the voltage to which tristated outputs are forced.

3.2.1 Functional Block Diagram and Terminal Assignments.

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Pin Assignments

G-100A

Function	Location	Function	Location	Function	Location	Function	Location
V _{DD}	A7	PMA1	B13	PMD12	K13	DMA9	G1
V _{DD}	G13	PMA2	C12	PMD13	K12	DMA10	G3
V _{DD}	H1	PMA3	A13	PMD14	L13	DMA11	G2
V _{DD}	N8	PMA4	B12	PMD15	L12	DMA12	F1
GND	A1	PMA5	A12	PMD16	M13	DMA13	F2
GND	A6	PMA6	B11	PMD17	M12	DMD0	A5
GND	A11	PMA7	B10	PMD18	N13	DMD1	B5
GND	E13	PMA8	A10	PMD19	M11	DMD2	A4
GND	H13	PMA9	B9	PMD20	N12	DMD3	B4
GND	J1	PMA10	A9	PMD21	N11	DMD4	A3
GND	M2	PMA11	C8	PMD22	M10	DMD5	A2
GND	N6	PMA12	B8	PMD23	N10	DMD6	B3
GND	N7	PMA13	A8	PMS	N5	DMD7	B2
CLKIN	L7	PMD0	D12	PMWR	L6	DMD8	B1
CLKOUT	L8	PMD1	D13	PMRD	M9	DMD9	C2
BR	M8	PMD2	E12	PMDA	M4	DMD10	C1
BG	N9	PMD3	F11	DMA0	N1	DMD11	D2
IRQ0	C6	PMD4	F12	DMA1	L2	DMD12	D1
IRQ1	B6	PMD5	F13	DMA2	M1	DMD13	E2
IRQ2	C7	PMD6	G11	DMA3	L1	DMD14	E1
IRQ3	B7	PMD7	G12	DMA4	K2	DMD15	F3
RESET	N2	PMD8	H12	DMA5	K1	DMS	M5
TRAP	N4	PMD9	H11	DMA6	J2	DMWR	M6
HALT	N3	PMD10	J13	DMA7	H3	DMRD	M7
INDEX PIN	NC	PMD11	J12	DMA8	H2	DMACK	M3
PMA0	C13						

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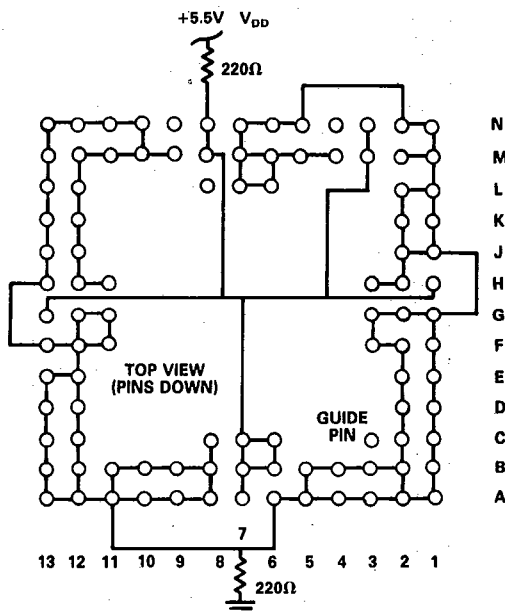
PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	PMD6	21	PMA10	41	DMD9	61	DMA2	81	BG
2	V _{DD}	22	PMA11	42	DMD10	62	DMA1	82	PMRD
3	PMD5	23	PMA12	43	DMD11	63	DMA0	83	PMD23
4	PMD4	24	PMA13	44	DMD12	64	GND	84	PMD22
5	PMD3	25	IRQ3	45	DMD13	65	RESET	85	PMD21
6	GND	26	IRQ2	46	DMD14	66	DMACK	86	PMD20
7	PMD2	27	V _{DD}	47	DMD15	67	HALT	87	PMD19
8	PMD1	28	GND	48	DMA13	68	PMDA	88	PMD18
9	PMD0	29	IRQ1	49	DMA12	69	TRAP	89	PMD17
10	PMA0	30	IRQ0	50	DMA11	70	DMS	90	PMD16
11	PMA1	31	DMD0	51	DMA10	71	PMS	91	PMD15
12	PMA2	32	DMD1	52	DMA9	72	PMWR	92	PMD14
13	PMA3	33	DMD2	53	V _{DD}	73	DMWR	93	PMD13
14	PMA4	34	DMD3	54	DMA8	74	GND	94	PMD12
15	PMA5	35	DMD4	55	DMA7	75	DMRD	95	PMD11
16	PMA6	36	DMD5	56	GND	76	CLKIN	96	PMD10
17	GND	37	DMD6	57	DMA6	77	GND	97	PMD9
18	PMA7	38	GND	58	DMA5	78	V _{DD}	98	PMD8
19	PMA8	39	DMD7	59	DMA4	79	BR	99	GND
20	PMA9	40	DMD8	60	DMA3	80	CLKOUT	100	PMD7

3.2.4. Microcircuit Technology Group.

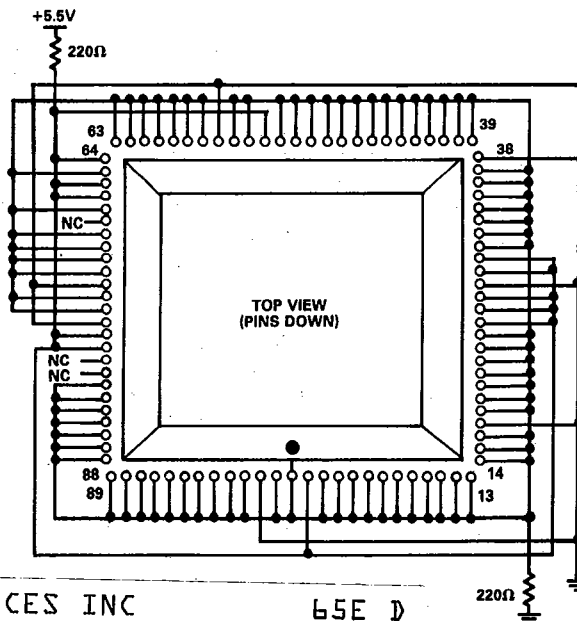
This microcircuit is covered by technology group (105).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



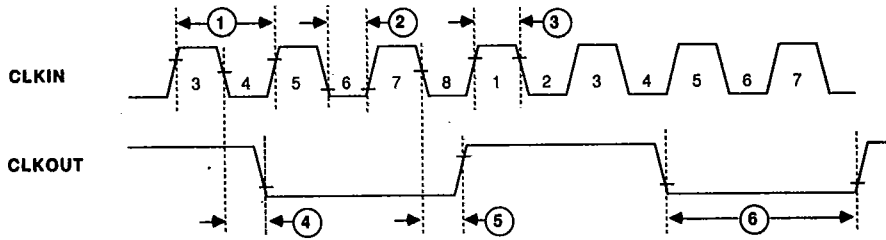
ADSP-2100G/ADSP-2100AG Life Test and Burn-In Circuit



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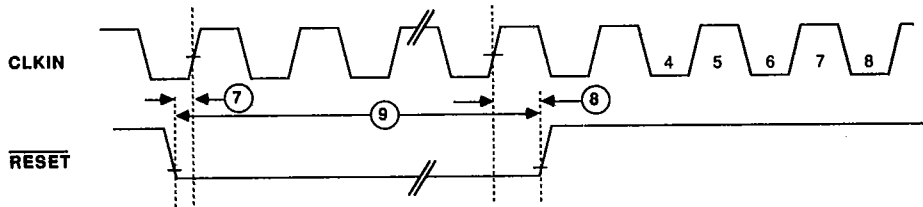
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ADSP-2100Z/ADSP-2100AZ Life Test and Burn-In Circuit

**NOTE**

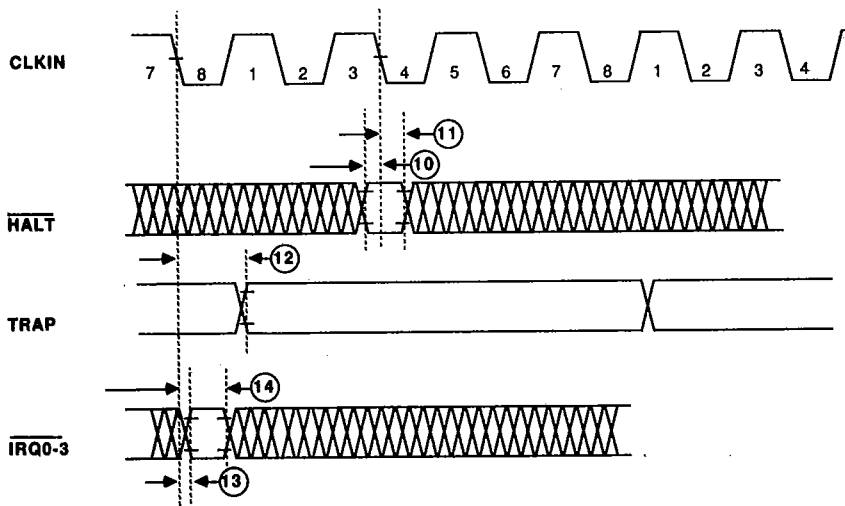
The Processor Cycle is Divided into 8 Internal States Determined by the Rising and Falling Edges of CLKIN. CLKOUT is Synchronized to the Processor States as Shown Above.

Figure 1. Clock Signals

**NOTE**

The Reset signal determines the phase of the processor cycle. The processor starts from state 4 after the release of the Reset signal.

Figure 2. RESET Signal

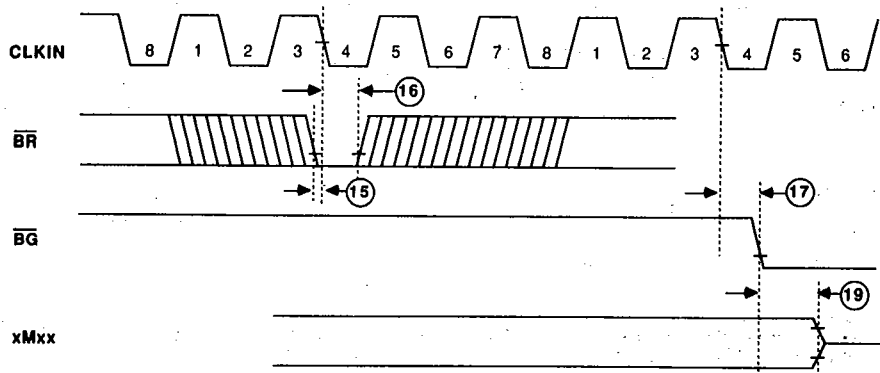
**NOTE**

The Control Signals are Shown in Relationship to the Processor States in Which They are Recognized or Asserted as Defined by CLKIN. There is No Implied Relationship between HALT, TRAP, and IRQ₀₋₃.

Figure 3. Control Signals

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NOTE: RESET NOT PERMITTED DURING $\overline{BR}$.

Figure 4. Bus Request Asserted

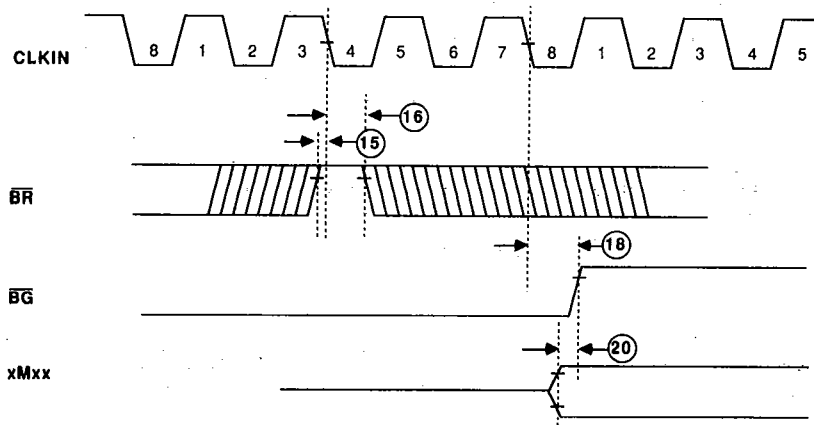
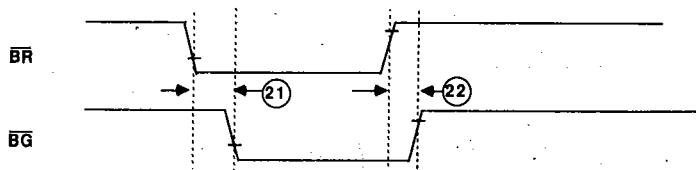


Figure 5. Bus Request Negated



NOTE
During Reset, the Processor Bus Ignores the CLKIN Signal and Therefore the Bus Request/Grant Signals Operate Asynchronously.

Figure 6. Bus Request/Grant with $\overline{RESET}$ Low

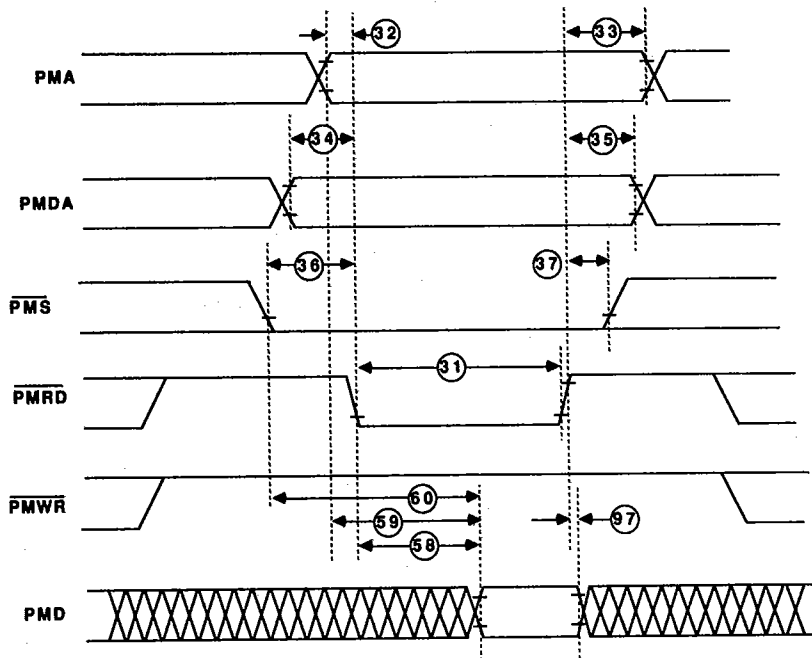


Figure 7. Program Memory Read

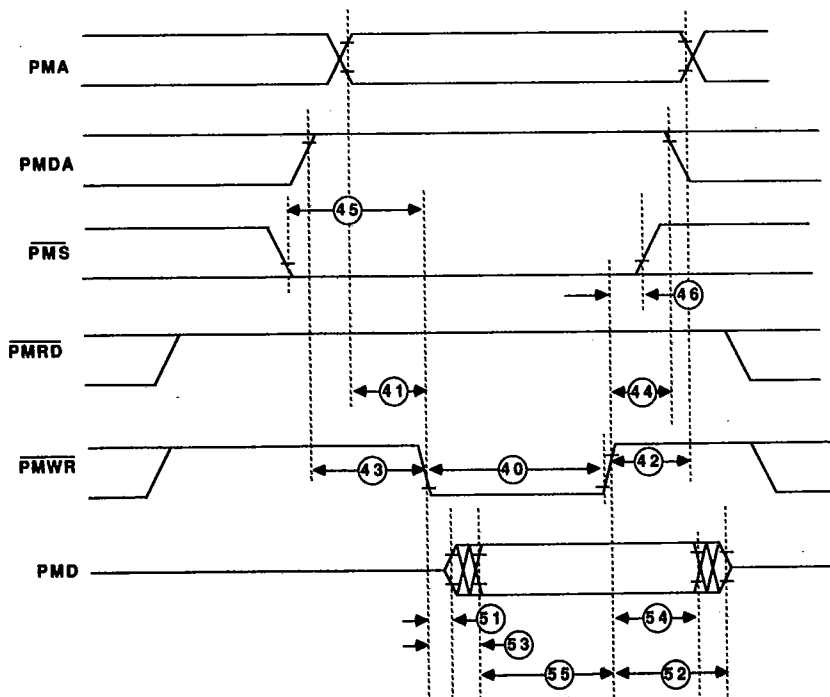


Figure 8. Program Memory Write

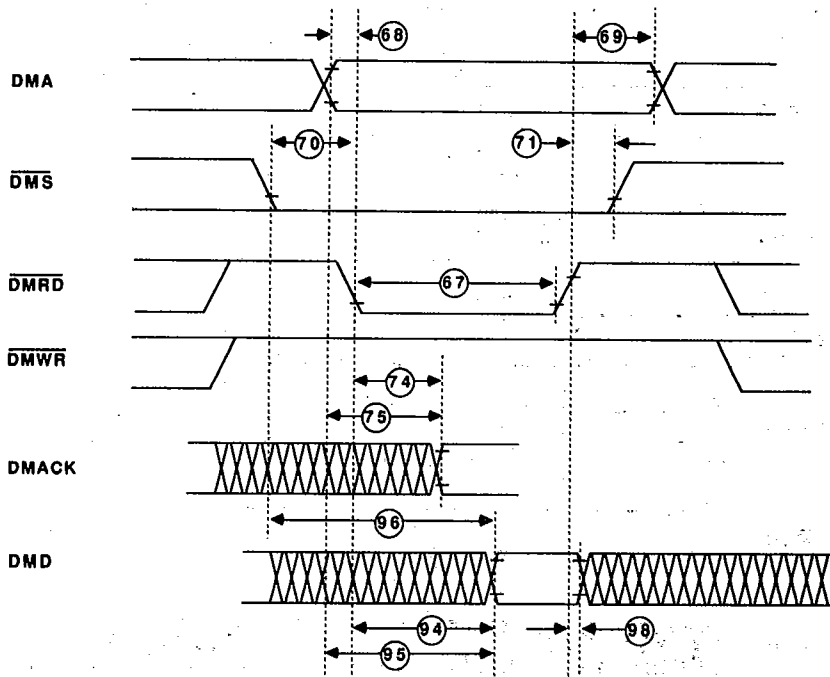


Figure 9a. Data Memory Read

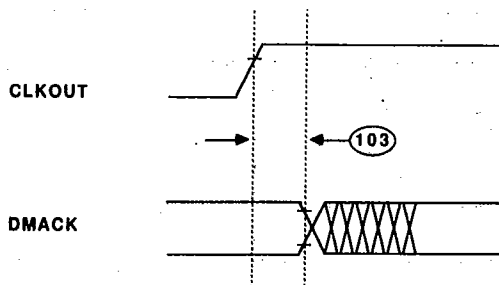


Figure 9b. Data Memory Wait States Extended with DMACK

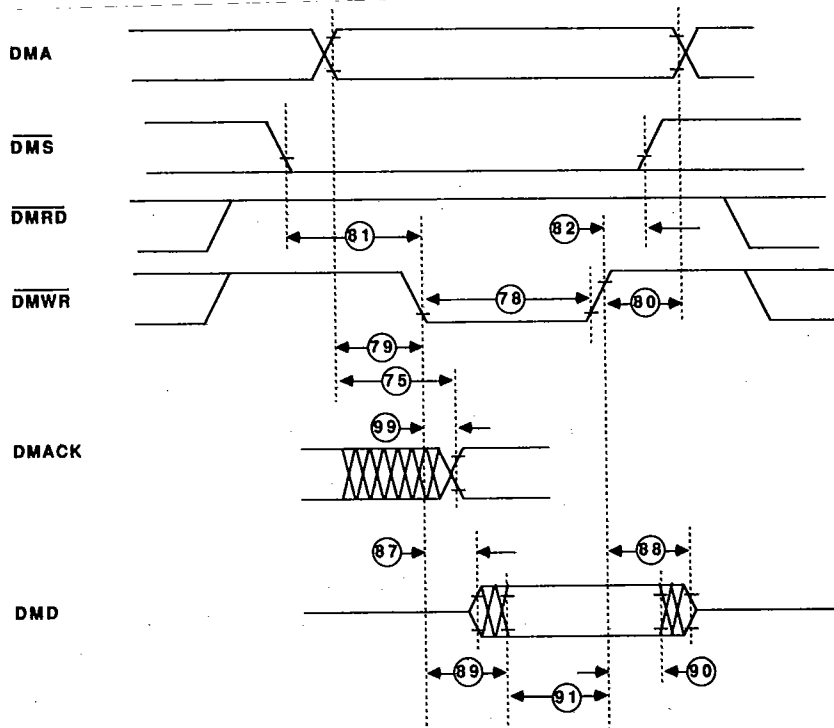


Figure 10a. Data Memory Write

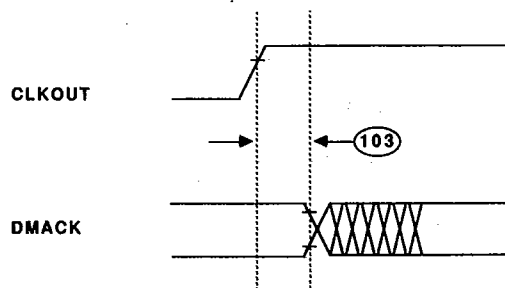


Figure 10b. Data Memory Wait States Extended with DMACK

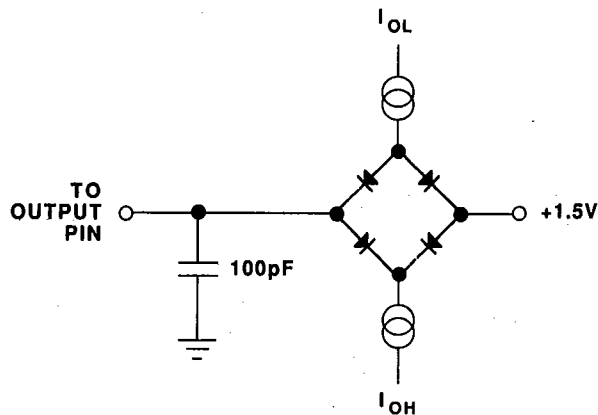


Figure 11. Normal Load for AC Measurements

Table 2. Condition Codes

Code	Status Condition	True If:
EQ	ALU Equal Zero	AZ = 1
NE	ALU Not Equal Zero	AZ = 0
LT	ALU Less Than Zero	AN .XOR. AV = 1
GE	ALU Greater Than or Equal Zero	AN .XOR. AV = 0
LE	ALU Less Than or Equal Zero	(AN .XOR. AV) .OR. AZ = 1
GT	ALU Greater Than Zero	(AN .XOR. AV) .OR. AZ = 0
AC	ALU Carry	AC = 1
NOT AC	Not ALU Carry	AC = 0
AV	ALU Overflow	AV = 1
NOT AV	Not ALU Overflow	AV = 0
MV	MAC Overflow	MV = 1
NOT MV	Not MAC Overflow	MV = 0
NEG	ALU X Input Sign Negative	AS = 1
POS	ALU X Input Sign Positive	AS = 0
NOT CE	Not Counter Expired	CE $\neq$ 0
TRUE	True	Always True

Table 3. Register Classification

AX0, AX1	Data Registers (dreg)	Accessible Registers (reg)
AY0, AY1		
AR		
MX0, MX1		
MY0, MY1		
MR0, MR1, MR2		
SI		
SE		
SR0, SR1		
SB		
PX		
I0, I1, I2, I3, I4, I5, I6, I7		
M0, M1, M2, M3, M4, M5, M6, M7		
L0, L1, L2, L3, L4, L5, L6, L7		
CNTR		
ASTAT		
MSTAT		
SSTAT		
IMASK		
ICNTL		

Table 4. Computational Input/Output Registers

ALU		
Source for X input port (xop)	Source for Y input port (yop)	Destination for output port R
AX0, AX1 AR MR0, MR1, MR2 SR0, SR1	AY0, AY1 AF	AR AF
MAC		
Source for X input port (xop)	Source for Y input port (yop)	Destination for output port R
MX0, MX1 AR MR0, MR1, MR2 SR0, SR1	MY0, MY1 MF	MR (MR2, MR1, MR0) MF
Shifter		
Source for Shifter input (xop)		Destination for Shifter output
SI AR MR0, MR1, MR2 SR0, SR1		SR (SR1, SR0)

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These conventions are used in Table 5.

1. All keywords are shown in capital letters.
2. Brackets enclose optional parts of the syntax.
3. Vertical lines indicate that one parameter must be chosen from those enclosed.
4. Table 2 defines the conditions for *condition*.
5. Table 3 defines the set of registers for *dreg* and *reg*.
6. Table 4 defines the set of registers for *xop* and *yop*.
7. <data> represents an immediate value.
8. <address> may be an immediate value or label.
9. <comp>, in a multifunction instruction, represents all legal ALU, MAC or Shifter operations with these restrictions:
 - All operations are performed unconditionally
 - Shift Immediate operations are not allowed
 - ALU division (DIVS, DIVQ) is not allowed.

Table 5. Instruction Set Summary

DATA MOVE INSTRUCTIONS

Register Move

reg = reg;

Load Register Immediate

reg = <data>;

Data Memory Read (direct address)

reg = DM (<address>;

Data Memory Read (indirect address)

dreg = DM (

I0	M0
I1	M1
I2	M2
I3	M3
I4	M4
I5	M5
I6	M6
I7	M7

);

Program Memory Read (indirect address)

dreg = PM (

I4	M4
I5	M5
I6	M6
I7	M7

);

Data Memory Write (direct address)

DM (<address>) = reg;

Data Memory Write (indirect address)

DM (

I0	M0
I1	M1
I2	M2
I3	M3
I4	M4
I5	M5
I6	M6
I7	M7

) = dreg; <data>

Program Memory Write (Indirect address)

PM (

I4	M4
I5	M5
I6	M6
I7	M7

) = dreg;

COMPUTATIONAL INSTRUCTIONS: ALU

Add/Add with Carry

[IF condition]

AR
AF

 = xop

+yop
+C
+ yop + C

 ;

Subtract X-Y/Subtract X-Y with Borrow

[IF condition]

AR
AF

 = xop

-yop
-yop + C - 1

 ;

Subtract Y-X/Subtract with Borrow

[IF condition]

AR
AF

 = yop

-xop
-xop + C - 1

 ;

AND, OR, Exclusive OR

[IF condition]

AR
AF

 = xop

AND
OR
XOR

 yop ;

Pass/Clear

[IF condition]

AR
AF

 = PASS

xop
yop

 ;

Negative

[IF condition]

AR
AF

 = -

xop
yop

 ;

NOT

[IF condition]

AR
AF

 = NOT

xop
yop

 ;

Absolute Value

[IF condition]

AR
AF

 = ABS

xop
yop

 ;

Increment

[IF condition]

AR
AF

 = yop + 1 ;

Decrement

[IF condition]

AR
AF

 = yop - 1 ;

Divide

DIVS yop, xop ;
DIVQ xop ;

Table 5. Instruction Set Summary (Continued)

COMPUTATIONAL INSTRUCTIONS: SHIFTER**Arithmetic Shift**

[IF condition] SR = [SR OR] ASHIFT xop $\left(\begin{array}{c} \text{(HI)} \\ \text{(LO)} \end{array} \right)$;

Logical Shift

[IF condition] SR = [SR OR] LSHIFT xop $\left(\begin{array}{c} \text{(HI)} \\ \text{(LO)} \end{array} \right)$;

Normalize

[IF condition] SR = [SR OR] NORM xop $\left(\begin{array}{c} \text{(HI)} \\ \text{(LO)} \end{array} \right)$;

Derive Exponent

[IF condition] SE = EXP xop $\left(\begin{array}{c} \text{(HI)} \\ \text{(LO)} \\ \text{(HIX)} \end{array} \right)$;

Block Exponent Adjust

[IF condition] SB = EXPADJ xop ;

Arithmetic Shift Immediate

SR = [SR OR] ASHIFT xop BY <data> $\left(\begin{array}{c} \text{(HI)} \\ \text{(LO)} \end{array} \right)$;

Logical Shift Immediate

SR = [SR OR] LSHIFT xop BY <data> $\left(\begin{array}{c} \text{(HI)} \\ \text{(LO)} \end{array} \right)$;

COMPUTATIONAL INSTRUCTIONS: MAC**Multiply**

[IF condition] $\left(\begin{array}{c} \text{MR} \\ \text{MF} \end{array} \right) = \text{xop} * \text{yop} \left(\begin{array}{c} \text{SS} \\ \text{SU} \\ \text{US} \\ \text{UU} \\ \text{RND} \end{array} \right) ;$

Multiply Accumulate

[IF condition] $\left(\begin{array}{c} \text{MR} \\ \text{MF} \end{array} \right) = \text{MR} + \text{xop} * \text{yop} \left(\begin{array}{c} \text{SS} \\ \text{SU} \\ \text{US} \\ \text{UU} \\ \text{RND} \end{array} \right) ;$

Multiply Subtract

[IF condition] $\left(\begin{array}{c} \text{MR} \\ \text{MF} \end{array} \right) = \text{MR} - \text{xop} * \text{yop} \left(\begin{array}{c} \text{SS} \\ \text{SU} \\ \text{US} \\ \text{UU} \\ \text{RND} \end{array} \right) ;$

Clear

[IF condition] $\left(\begin{array}{c} \text{MR} \\ \text{MF} \end{array} \right) = 0 ;$

Transfer MR

[IF condition] $\left(\begin{array}{c} \text{MR} \\ \text{MF} \end{array} \right) = \text{MR} [\text{RND}] ;$

Conditional MR Saturation

IF MV SAT MR ;

PROGRAM FLOW CONTROL INSTRUCTION**Jump**

[IF condition] Jump $\left(\begin{array}{c} \text{I4} \\ \text{I5} \\ \text{I6} \\ \text{I7} \\ \text{<address>} \end{array} \right) ;$

Call

[IF condition] CALL $\left(\begin{array}{c} \text{I4} \\ \text{I5} \\ \text{I6} \\ \text{I7} \\ \text{<address>} \end{array} \right) ;$

Return from Subroutine

[IF condition] RTS ;

Return from Interrupt

[IF condition] RTI ;

Do Until

DO <address> [UNTIL condition] ;

Trap

[IF condition] TRAP ;

MULTIFUNCTION INSTRUCTIONS**Computation with Memory Read**

<comp> , dreg = DM $\left(\begin{array}{c} \text{I0} \\ \text{I1} \\ \text{I2} \\ \text{I3} \\ \text{I4} \\ \text{I5} \\ \text{I6} \\ \text{I7} \end{array} \right)$, $\left(\begin{array}{c} \text{M0} \\ \text{M1} \\ \text{M2} \\ \text{M3} \\ \text{M4} \\ \text{M5} \\ \text{M6} \\ \text{M7} \end{array} \right) ;$

PM $\left(\begin{array}{c} \text{I4} \\ \text{I5} \\ \text{I6} \\ \text{I7} \end{array} \right)$, $\left(\begin{array}{c} \text{M4} \\ \text{M5} \\ \text{M6} \\ \text{M7} \end{array} \right) ;$

Computation with Data Register Move

<comp> , dreg = dreg ;

Computation with Memory Write

DM $\left(\begin{array}{c} \text{I0} \\ \text{I1} \\ \text{I2} \\ \text{I3} \\ \text{I4} \\ \text{I5} \\ \text{I6} \\ \text{I7} \end{array} \right)$, $\left(\begin{array}{c} \text{M0} \\ \text{M1} \\ \text{M2} \\ \text{M3} \\ \text{M4} \\ \text{M5} \\ \text{M6} \\ \text{M7} \end{array} \right) = \text{dreg}, \text{<comp>} ;$

PM $\left(\begin{array}{c} \text{I4} \\ \text{I5} \\ \text{I6} \\ \text{I7} \end{array} \right)$, $\left(\begin{array}{c} \text{M4} \\ \text{M5} \\ \text{M6} \\ \text{M7} \end{array} \right) ;$

Table 5. Instruction Set Summary (Continued)

Data & Program Memory Read

AX0	= DM (	I0	,	M0	)	,	AY0	= PM (	I4	,	M4	)	;
AX1		I1		M1			AY1		I5		M5		
MX0		I2		M2			MY0		I6		M6		
MX1		I3		M3			MY1		I7		M7		

ALU/MAC Operation with Data & Program Memory Read*

$\left\{ \begin{array}{l} \langle \text{ALU} \rangle \\ \langle \text{MAC} \rangle \end{array} \right\}$	,	$\left\{ \begin{array}{l} \text{AX0} \\ \text{AX1} \\ \text{MX0} \\ \text{MX1} \end{array} \right\}$	= DM (	$\left\{ \begin{array}{l} \text{I0} \\ \text{I1} \\ \text{I2} \\ \text{I3} \end{array} \right\}$	,	$\left\{ \begin{array}{l} \text{M0} \\ \text{M1} \\ \text{M2} \\ \text{M3} \end{array} \right\}$	)	,	$\left\{ \begin{array}{l} \text{AY0} \\ \text{AY1} \\ \text{MY0} \\ \text{MY1} \end{array} \right\}$	= PM (	$\left\{ \begin{array}{l} \text{I4} \\ \text{I5} \\ \text{I6} \\ \text{I7} \end{array} \right\}$	,	$\left\{ \begin{array}{l} \text{M4} \\ \text{M5} \\ \text{M6} \\ \text{M7} \end{array} \right\}$	)	;
--	---	--	--------	--	---	--	---	---	--	--------	--	---	--	---	---

*ALU Division operations not allowed.

MISCELLANEOUS INSTRUCTIONS

Stack Control

[PUSH STS] [, POP CNTR] [, POP PC] [, POP LOOP] ;
[POP]

Mode Control

[ENA BIT_REV] [, [ENA AV_LATCH] [, [ENA AR_SAT] [, [ENA SEC_REG] ;
[DIS] [, [DIS] [, [DIS] [, [DIS]

Modify Address Register

MODIFY (	I0	,	M0	)	;
	I1		M1		
	I2		M2		
	I3		M3		
	I4		M4		
	I5		M5		
	I6		M6		
	I7		M7		

No Operation

NOP ;

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