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ADVANCED ANALOG

ADC674A

HYBRID 12-BIT A/D CONVERTER WITH μP INTERFACE

DESCRIPTION

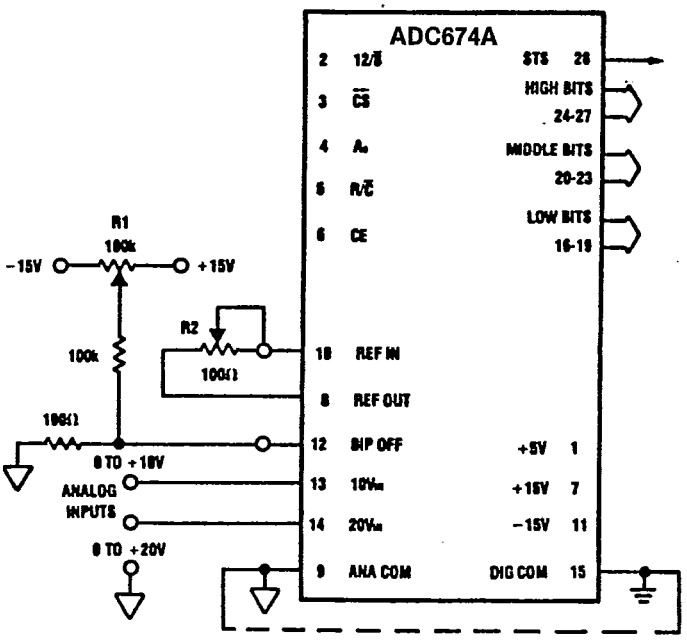
The ADC674A is a 12-bit analog-to-digital converter that contains a +10V reference, clock, three-state outputs plus a digital interface for μP control. It is a complete, successive approximation device and has four selectable input ranges. The voltage comparator features a high PSRR, plus a high speed current-mode latch. Low noise signal transmission is achieved by utilizing current rather than voltage between the analog and digital IC's. The clock oscillator is current controlled and features 12 μs (typ) conversion times.

Power requirements are +5V and ±12V to ±15V. Laser trimming assures that linearity, gain and offset accuracy meet or exceed specifications.

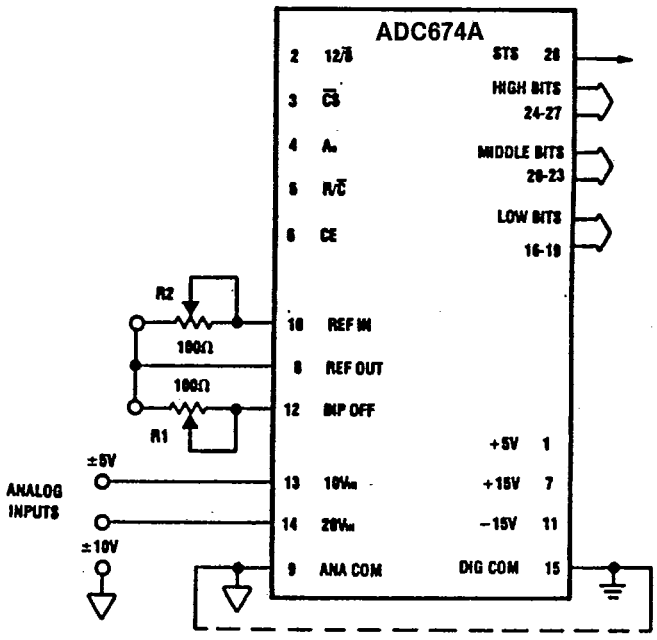
FEATURES

- LOW COST 12-BIT A/D CONVERTER
- SMALL 28-PIN HERMETIC DIP PACKAGE
- CONTAINS +10V REFERENCE, CLOCK, THREE-STATE OUTPUTS, μP INTERFACE
- LOW NOISE
- FULL 8- OR 16-BIT μP INTERFACE
- PIN COMPATIBLE WITH ADC574A
- 12 μs CONVERSION TIME

BLOCK DIAGRAM



UNIPOLAR CONNECTIONS



BIPOLAR CONNECTIONS

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC AND TRANSFER ACCURACY SPECIFICATIONS

MODEL	ADC674AJ	ADC674AK	ADC674AL	ADC674AS	ADC674AT	ADC674AU	UNITS
Temperature Range	0 TO +75			−55 TO +125			°C
Resolution (max)	12	12	12	12	12	12	Bits
Linearity Error							
25°C (max)	±1	±1/2	±1/2	±1	±1/2	±1/2	LSB
T_{min} to T_{max} (max)	±1	±1/2	±1/2	±1	±1	±1	LSB
Differential Linearity Error (Maximum resolution for which no missing codes is guaranteed)							
25°C	11	12	12	11	12	12	Bits
T_{min} to T_{max}	11	12	12	11	12	12	Bits
Unipolar Offset (max) (Adjustable to zero)	±2	±2	±2	±2	±2	±2	LSB
Bipolar Offset (max) (Adjustable to zero)	±10	±4	±4	±10	±4	±4	LSB
Full Scale Calibration Error							
25°C (max), with fixed 50 Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	0.3	0.3	0.3	0.3	% of F.S.
T_{min} to T_{max}							
(No adjustment at +25°C)	0.5	0.4	0.35	0.8	0.6	0.4	% of F.S.
(With adjustment to zero at +25°C)	0.22	0.12	0.05	0.5	0.25	0.12	% of F.S.
Temperature Coefficients							
Guaranteed max change, T_{min} to T_{max} (Using internal reference)							
Unipolar Offset	±2	±1	±1	±2	±1	±1	LSB
	(10)	(5)	(5)	(5)	(2.5)	(2.5)	(ppm/°C)
Bipolar Offset	±2	±1	±1	±4	±2	±1	LSB
	(10)	(5)	(5)	(10)	(5)	(2.5)	(ppm/°C)
Full Scale Calibration	±9	±5	±2	±20	±10	±5	LSB
	(45)	(25)	(10)	(50)	(25)	(12.5)	(ppm/°C)
Power Supply Rejection							
Max change in Full Scale Calibration							
+13.5V<V_{CC}<+16.5V or +11.4V<V_{CC}<+12.6V	±2	±1	±1	±2	±1	±1	LSB
+4.5V<V_{LOGIC}<+5.5V	±1/2	±1/2	±1/2	±1/2	±1/2	±1/2	LSB
−16.5V<V_{EE}<−13.5V or −12.6V<V_{EE}<−11.4V	±2	±1	±1	±2	±1	±1	LSB
Analog Inputs							
Input Ranges							
Bipolar	−5 to +5			−5 to +5			Volts
	−10 to +10			−10 to +10			Volts
Unipolar	0 to +10			0 to +10			Volts
	0 to +20			0 to +20			Volts
Input Impedance							
10 Volt Span	5K, ± 25%			5K Ω, ± 25%			Ohms
20 Volt Span	10K, ± 25%			10K Ω, ± 25%			Ohms
Power Supplies							
Operating Voltage Range							
V_{LOGIC}	+4.5 to +5.5			+4.5 to +5.5			Volts
V_{CC}	+11.4 to +16.5			+11.4 to +16.5			Volts
V_{EE}	−11.4 to −16.5			−11.4 to −16.5			Volts
Operating Current							
I_{LOGIC}	7 TYP, 15 MAX			7 TYP, 15 MAX			mA
I_{CC}	11 TYP, 15 MAX			11 TYP, 15 MAX			mA
I_{EE}	21 TYP, 28 MAX			21 TYP, 28 MAX			mA
Power Dissipation	515 TYP, 720 MAX			515 TYP, 720 MAX			mW
Internal Reference Voltage	+10.00 ± 0.1 MAX			+10.00 ± 0.1 (MAX)			Volts
Output current,[1] available for external loads (External load should not change during conversion).	2.0 MAX			2.0 MAX			mA

Consult factory for devices with mil screening.

1. When supplying an external load and operating on ± 12V supplies, a buffer must be provided for the reference output.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

Truth table for ADC674A control inputs

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and A_0. Refer to timing diagram.

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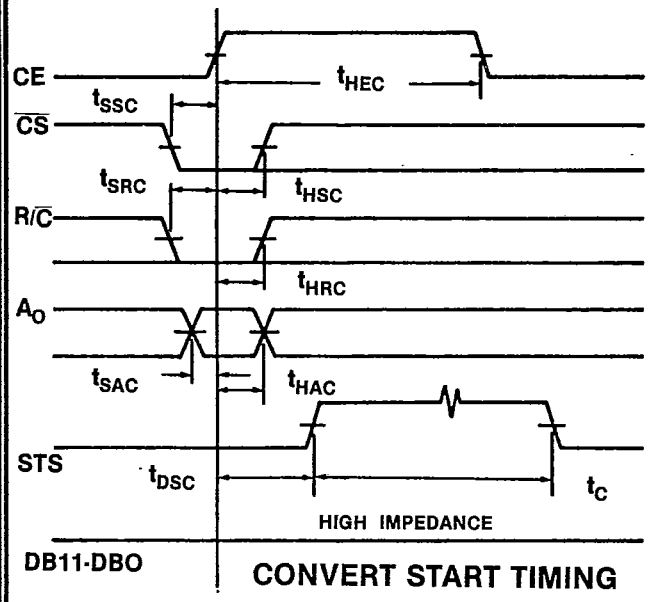
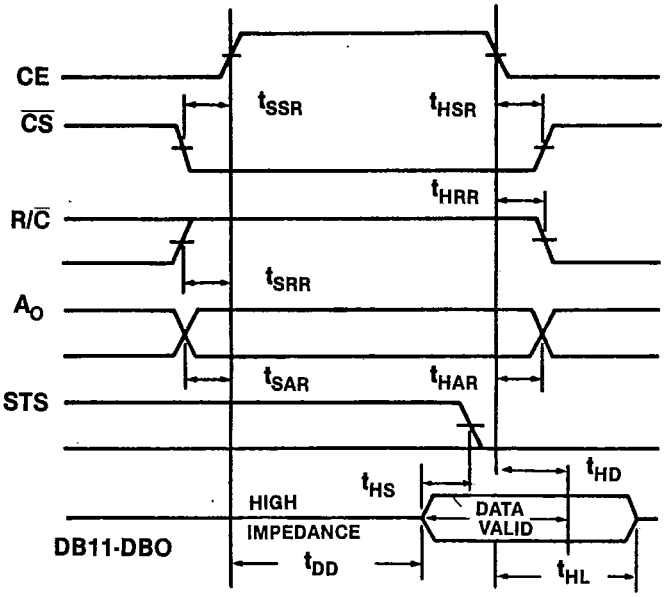
TIMING DIAGRAM



CONVERT START TIMING



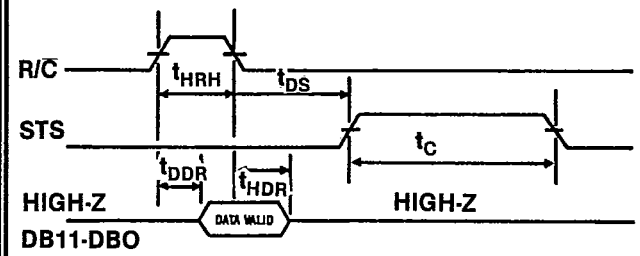
READ CYCLE TIMING

ADC674A TIMING SPECIFICATIONS (+25°C)

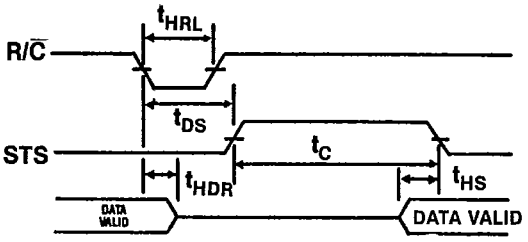
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Convert Mode					
t_{DSC}	STS Delay from CE		100	200	ns
t_{HEC}	CE Pulse width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup	50	20		ns
t_{HSC}	$\overline{CS}$ Low during CE High	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0		ns
t_{HRC}	R/$\overline{C}$ Low during CE High	50	20		ns
t_{SAC}	A_0 to CE Setup	0	0		ns
t_{HAC}	A_0 Valid during CE high	50	20		ns
t_C	Conversion Time, 12-bit cycle	9	12	15	μS
	8-bit cycle	6	8	10	μS
Read Mode					
t_{DD}	Access Time from CE		75	150	ns
t_{HD}	Data Valid after CE Low	25	35		ns
t_{HL}	Output Float Delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0	0		ns
t_{SAR}	A_0 to CE Setup	50	25		ns
t_{HSR}	$\overline{CS}$ Valid after CE Low	0	0		ns
t_{HRR}	R/$\overline{C}$ High after CE Low	0	0		ns
t_{HAR}	A_0 Valid after CE High	50	25		ns
t_{HS}	STS Delay after Data Valid	100	300	600	ns

Note: Time is measured from 50% level of digital transitions.

INDEPENDENT OPERATION



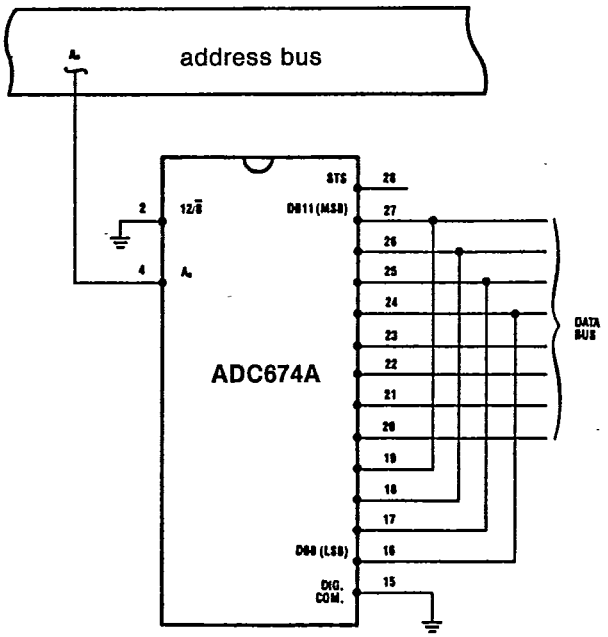
HIGH PULSE FOR R/$\overline{C}$-OUTPUTS ENABLED WHILE R/C HIGH, OTHERWISE HIGH-Z

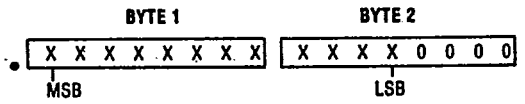


LOW PULSE FOR R/$\overline{C}$-OUTPUTS ENABLED AFTER CONVERSION

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	100	300	600	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

The independent control interface requires one control line connected to R/$\overline{C}$. CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_0 are wired low. Output data will have 12-bit words each. The R/$\overline{C}$ signal may have any duty cycle within and including the parameters shown in the diagram.



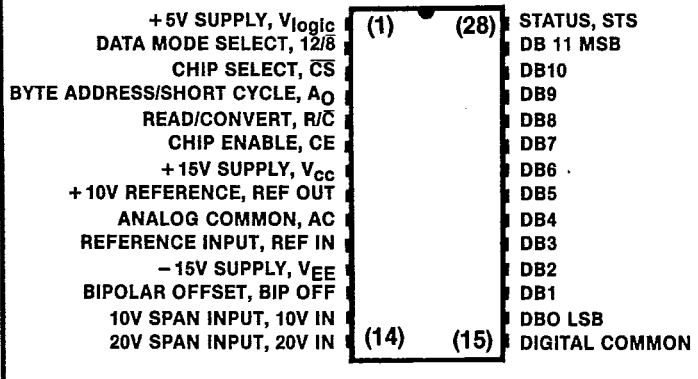


8-BIT DATA BUS INTERFACE

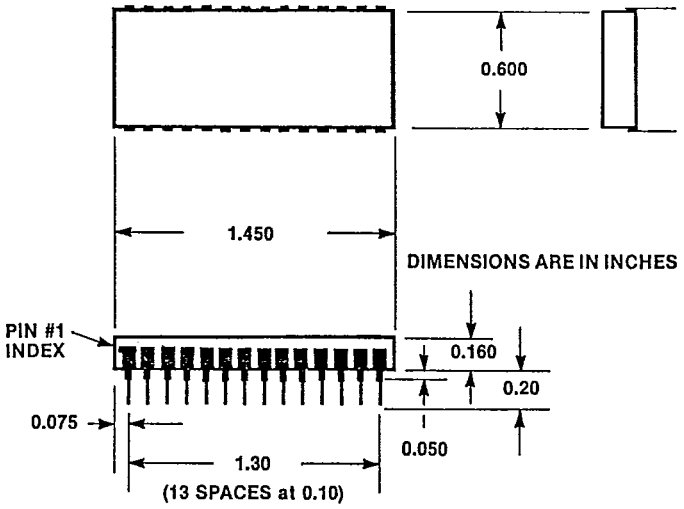
PART NUMBER

MODEL	TEMP. RANGE	LINEARITY ERROR MAX (T_{MIN} to T_{MAX})	RESOLUTION (NO MISSING CODES, T_{MIN} to T_{MAX})	FULL SCALE TC (PPM/°C MAX)
ADC674AJ	0 to 75°C	±1 LSB	11 Bits	45.0
ADC674AK	0 to 75°C	±½LSB	12 Bits	25.0
ADC674AL	0 to 75°C	±½LSB	12 Bits	10.0
ADC674AS	-55 to +125°C	±1 LSB	11 Bits	50.0
ADC674AS/B	-55 to +125°C	±1 LSB	11 Bits	50.0
ADC674AT	-55 to +125°C	±1 LSB	12 Bits	25.0
ADC674AT/B	-55 to +125°C	±1 LSB	12 Bits	25.0
ADC674AU	-55 to +125°C	±1 LSB	12 Bits	12.5
ADC674AU/B	-55 to +125°C	±1 LSB	12 Bits	12.5

PIN DESIGNATION



MECHANICAL OUTLINE



The information in this data sheet has been carefully checked and is believed to be accurate, however, no responsibility is assumed for possible errors. The specifications are subject to change without notice.

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ADVANCED ANALOG
2270 MARTIN AVENUE, SANTA CLARA, CALIFORNIA 95050-2781
TELEPHONE (408) 988-4930 TWX 910-338-2213