SGS-THOMSON MICROELECTRONICS

STV0117

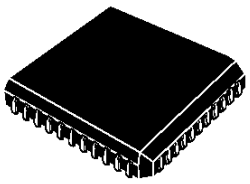
PAL/NTSC DIGITAL ENCODER

- NTSC-M, PAL-M, PAL-B, D, G, H, I, PAL-N EASILY PROGRAMMABLE VIDEO OUTPUTS
- U/V AND Q/I MATRIXING FOR RESPECTIVELY PAL AND NTSC ENCODING
- DIGITAL FRAME SYNC INPUT/OUTPUT (ODDEVEN)
- DIGITAL FRAME SYNC EXTRACTION FROM MULTIPLEXED 8-BIT INPUT PORT
- DIGITAL FIELD SYNC OUTPUT (FSYNC)
- DIGITAL COMPOSITE SYNC OUTPUT (VCS/HSYNC = VCS)
- DIGITAL HORIZONTAL SYNC INPUT/OUTPUT (VCS/HSYNC = HSYNC)
- 3 SLAVE OR 2 MASTER OPERATION MODES
- DUAL MODE CCIR601/SQUARE_PIXEL ENCODING WITH EASILY PROGRAMMABLE COLOR SUBCARRIER FREQUENCIES
- INTERLACED OR NON-INTERLACED OPERATION MODE
- 625LINES/50Hz or 525LINES/60Hz 8-BIT MULTIPLEXED CB-Y-CR DIGITAL INPUT
- OSD INSERTION INTERFACE AND 3 x 8 x 6-BIT CLUT
- CLOSED CAPTIONING
- MACROVISION™ COPY PROTECTION PROCESS (**VERSION 6.0/6.1**) ALLOWED ON CVBS, YS & C
- LUMINANCE FILTERING WITH 2 TIMES OVERSAMPLING AND SINX/X CORRECTION
- PROGRAMMABLE DELAY ON LUMINANCE PATH TO DIGITALLY COMPENSATE C/L DELAYS
- CHROMINANCE FILTERING WITH 4 TIMES OVERSAMPLING
- SWITCHABLE DEDICATED FILTER FOR Q COMPONENT
- 22-BIT DIRECT DIGITAL FREQUENCY SYNTHESIZER FOR COLOR SUBCARRIER MODULATION
- SERIAL INPUT FOR COLOR SUBCARRIER FREQUENCY CONTROL (CFC)
- CVBS, YS AND C SIMULTANEOUS ANALOG OUTPUTS THROUGH 9-BIT DACS
- CONTROLLED RISE/FALL TIMES OF ANALOG SYNCHRONIZATION OUTPUT
- POWER-DOWN MODE AVAILABLE INDEPENDENTLY ON EACH DAC
- 9-BIT DIGITAL INPUT FOR DIGITIZED ANALOG VIDEO WITH DIRECT ACCESS TO CVBS DAC
- EASILY CONTROLLED VIA I^2C BUS
- 2 HARDWARE I^2C CHIP ADDRESSES
- ON-CHIP COLOR BAR PATTERN GENERATOR
- HIGH TESTABILITY WITH FULL SCAN METHODOLOGY (FAULT COVERAGE 98%)
- PIN COMPATIBILITY WITH STV0116 (PAL/NTSC DIGITAL ENCODER WITH R, G, B OUTPUTS)
- APPLICATIONS : SATELLITE & CABLE DECODERS, MULTIMEDIA TERMINALS

DESCRIPTION

The STV0117 is a digital video device implemented in pure CMOS technology for multimedia, digital TV and computer applications.

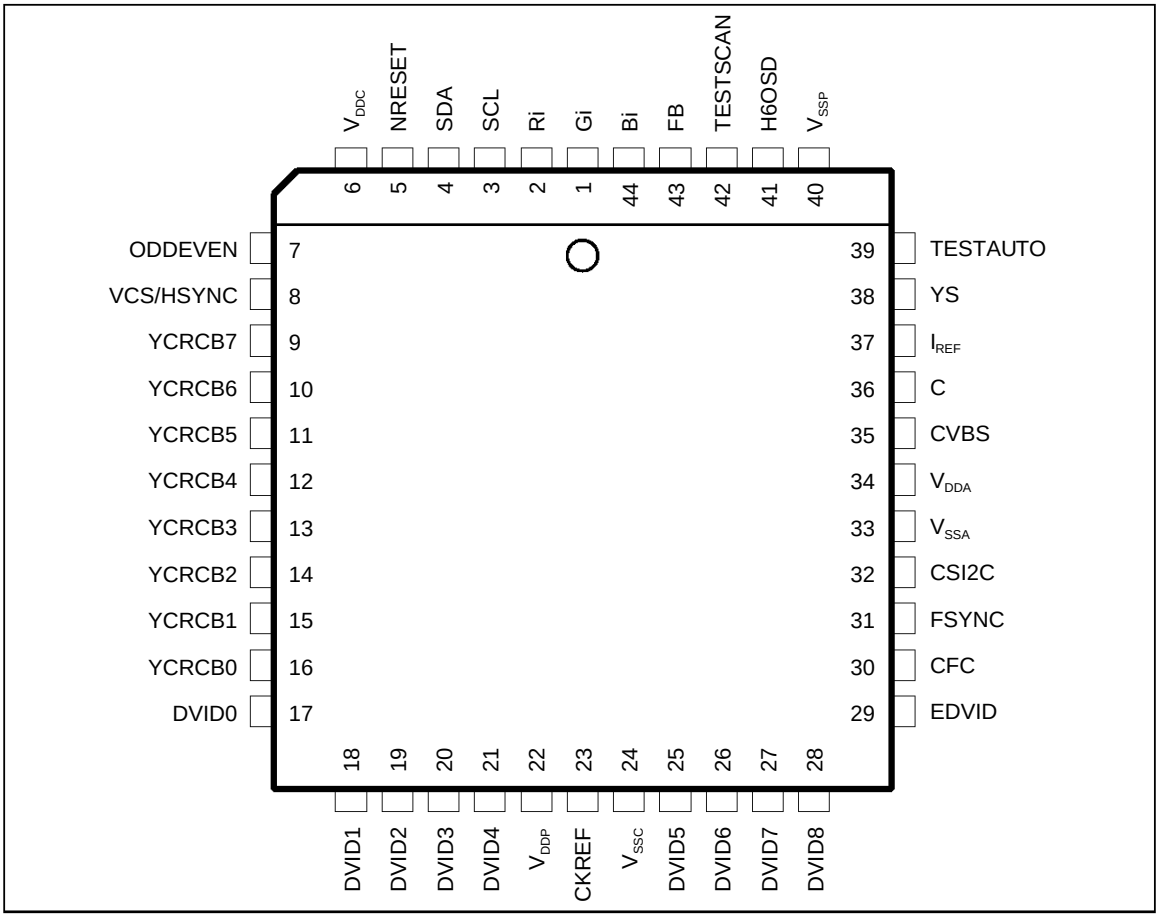
The STV0117 converts the digital output of a Video MPEG Decoder into a standard analog baseband NTSC/PAL signal with color subcarrier modulation. The STV0117 can handle interlaced mode (with 525 or 625 line standards), or non-interlaced mode (with 524 or 624 line standards), with square or rectangular pixels encoding. The STV0117 performs closed captions encoding and allows MACROVISION™ 6.0/6.1 copy protection process. Both composite and SVHS format video signals are simultaneously issued to three analog outputs, respectively CVBS, YS and C.



PLCC44
(Plastic Chip Carrier)
ORDER CODE : STV0117

Note : This device is protected by US patent numbers 4631603, 4577216 and 4819098 and other intellectual property rights. This device is protected by U.S. patent numbers 4,631,603, 4,577,216 and 4,819,098 and other intellectual property rights. The use of Macrovision's copy protection technology in the device must be authorized by Macrovision and is intended for home and other limited pay-per-view uses only, unless otherwise authorized in writing by Macrovision. Reverse engineering or disassembly is prohibited. Please contact your nearest SGS-THOMSON Microelectronics sales office for more information.

PIN CONNECTIONS



PIN DESCRIPTION

Pin	Symbol	Type	Function
1	Gi	Input	Second pixel index for 3 x 1-bit OSD input. **Minimum OSD_pixel width is one H6OSD period.**
2	Ri	Input	First pixel index (MSB) for 3 x 1-bit OSD input. **Minimum OSD_pixel width is one H6OSD period.**
3	SCL	Triggered Input	I^2C serial clock line (internal 5-bit majority logic).
4	SDA	I/O	I^2C serial data line triggered input (internal 5-bit majority logic). Open drain output, minimum LOW level duration 200ns.
5	NRESET	Input	Asynchronous reset, active LOW. It has priority over software reset (see I^2C REGISTER4). NRESET imposes default states (see I^2C REGISTERS DESCRIPTION and reset procedure in FUNCTIONAL DESCRIPTION). **Minimum LOW level required duration is 5 CKREF periods.**
6	V_{DDC}	Supply	Digital positive supply voltage for core (+5V).
7	ODDEVEN	I/O	ODDEVEN video frame signal : - input in slave modes, except when SYNC is extracted from YCRCB data, - output in master modes and when SYNC is extracted from YCRCB data. Synchronous to rising edge of CKREF. Default polarity : - odd(top) field : HIGH level, - even(bottom) field : LOW level. Default mode is slave by ODDEVEN and HSYNC, both with rising active edge.
8	VCS/HSYNC	I/O	Composite or horizontal synchronization signal : - input in one slave mode : HSYNC input (defined by sym2 = 1), - output in other modes : VCS or HSYNC. Synchronous to rising edge of CKREF. Default polarity : leading edge of the pulse is rising Default mode is slave by ODDEVEN and HSYNC, both with rising active edge.
9 10 11 12 13 14 15 16	YCRCB7 YCRCB6 YCRCB5 YCRCB4 YCRCB3 YCRCB2 YCRCB1 YCRCB0	Input	Time multiplexed 4:2:2 luminance and chrominance data as defined in CCIR Rec601-2 and Rec656 (except for TTL input levels). Timing Rec656-partII for CCIR rectangular pixels ; for square pixels data see chapter DATA INPUT FORMAT in FUNCTIONAL DESCRIPTION. This bus interfaces with MPEG video decoder output port.
17 18 19 20 21	DVID0 DVID1 DVID2 DVID3 DVID4	I/O	Input (default mode) : 5 LSBs of digitized analog video for direct access to CVBS 9-bit DAC inputs. Enabled by software or/and by hardware. Tristate output for test purpose only.
22	V_{DDP}	Supply	Digital positive supply voltage for pad ring (+5V).
23	CKREF	Input	Clock reference signal : rising edge is the reference for setup and hold times of all inputs, and for propagation delay of all outputs (except for SDA output). Frequency is 27MHz in CCIR601 and in square pixel mode : 24.5454MHz or 29.50MHz.
24	V_{SSC}	Supply	Digital ground for core.
25 26 27 28	DVID5 DVID6 DVID7 DVID8	I/O	Input (default mode) : 4 MSBs of digitized analog video for direct access to CVBS 9-bit DAC inputs. Enabled by software or/and by hardware. Tristate output for test purpose only.
29	EDVID	Input	Hardware control signal for DVID inputs select when this control is allowed by software : - if EDVID is HIGH level, then DVID data is enabled and DVID data is an input for CVBS 9-bit DAC, - if EDVID is LOW level, then DVID data is disabled and DVID data is ignored for CVBS 9-bit DAC. When this control is disabled by software : DVID[8:0] inputs are controlled by software whatever the level on EDVID input.

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PIN DESCRIPTION (continued)

Pin	Symbol	Type	Function
30	CFC	Input	Color subcarrier frequency control line : 23-bit stream line, synchronous to CKREF. **In standby mode, CFC must be at HIGH level.** Reception starts with one LOW level bit and then a 22-bit word is received for increment of color subcarrier direct digital frequency synthesizer, and then line returns to standby mode i.e at HIGH level. This real time control is enabled by software and is a color lock interface. This line is ignored by default.
31	FSYNC	Output	Field synchronization signal, synchronous to CKREF. It is a horizontal sync signal generated every field beginning. Default polarity is positive (like HSYNC).
32	CSI2C	Input	Hardware I^2C chip address select : - when LOW, I^2C chip addresses are 40 and 41 hexadecimal, - when HIGH, I^2C chip addresses are 42 and 43 hexadecimal.
33	V_{SSA}	Supply	Analog ground for 3 DACs.
34	V_{DDA}	Supply	Analog positive supply voltage for 3 DACs (+5V).
35	CVBS	Output	Current analog video composite signal : CVBS must be connected to analog ground over a load resistor (R_L). Between the load resistor and the video equipment, an analog low pass filter may be necessary to suppress the alias signal. CVBS amplitude is typically $2.48V_{PP}$ on R_L and is proportional to I_{REF}.
36	C	Output	Current analog chrominance signal : S-VHS output for a VCR or a TV set. C must be connected to analog ground over a load resistor (R_L). Between the load resistor and the video equipment, an analog low pass filter may be necessary to suppress the alias signal. C amplitude is typically $1.6V_{PP}$ on R_L and is proportional to I_{REF}.
37	I_{REF}	Input	Reference current source for the 3 x 9-bit DACs CVBS,YS,C. I_{REF} must be connected to analog ground over a reference resistor (R_{REF}). I_{REF} range is from 2 up to 6mA.
38	YS	Output	Current analog luminance with composite synchronization signal : S-VHS output for a VCR or a TV set. YS must be connected to analog ground over a load resistor (R_L). Between the load resistor and the video equipment, an analog low pass filter may be necessary to suppress the alias signal. YS amplitude is typically $2.0V_{PP}$ on R_L and is proportional to I_{REF}.
39	TESTAUTO	Input	Hardware autotest mode control, active HIGH. TESTAUTO input forces the master mode with color bar pattern outputs.
40	V_{SSP}	Supply	Digital ground for pad ring.
41	H6OSD	Output	CKREF/4 clock signal for external OSD generator clock output stage. Synchronous to CKREF and controlled by software : inactive by default (LOW level).
42	TESTSCAN	Input	Full scan test mode control, active HIGH. **TESTSCAN must be grounded for normal operation.**
43	FB	Input	Fast blanking signal to control 3x1bit OSD inputs, active HIGH. Synchronous to H6OSD or CKREF. **FB must be LOW level in autotest mode.**
44	Bi	Input	Third pixel index (LSB) for 3 x 1-bit OSD input. **Minimum OSD_pixel width is one H6OSD period.**

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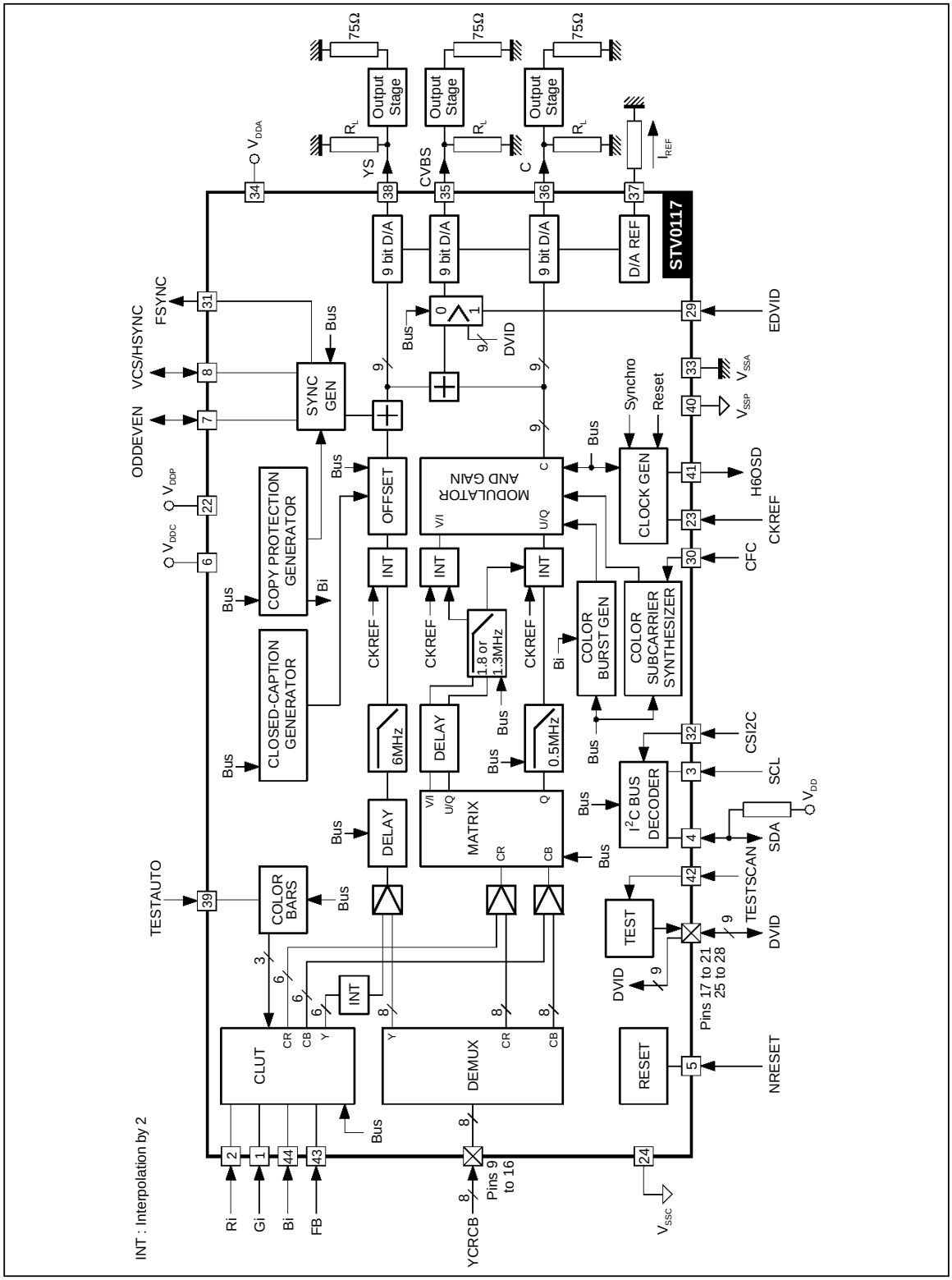
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The STV0117 can operate either in slave mode by locking onto a vertical parity synchronization signal received from MPEG video decoder, or in master mode by supplying the sync signal to this device.

By using an I^2C bus, it is allowed to control the following main functions :

- selection of the standard,
- synchronization mode and polarity,
- CCIR601 or square pixel data format,
- interlaced or non-interlaced mode,
- reset of the synchronization,
- luminance delay adjustment,
- chrominance filter selection,
- reset of the oscillator,
- subcarrier phase and frequency adjustment,
- color killer,
- closed captions encoding,
- MACROVISION™ 6.0/6.1 copy protection processing,
- OSD insertion,
- power-down mode for each DAC.

1 - Data Input Format

The digital input is a time multiplexed [[CB,Y,CR], Y], 8-bit stream. Input samples are taken into account on the rising edge of CKREF clock input signal (see Figure 1).

Dual mode CCIR601/square_pixel encoding is performed with semi-automatic programmation of subcarrier frequencies from master clock (CKREF) as shown in Table 1.

Table 1

Standard	Application	CKREF Frequency (MHz)	Pixel Rate (MHz)	Field Rate (Hz)	Vertical Resolution
PAL-B, D, G, H, I, PAL-N	CCIR601	27	13.5	50	625
NTSC-M, PAL-M	CCIR601	27	13.5	60	525
PAL-B, D, G, H, I, PAL-N	Square Pixel (graphics)	29.50	14.75	50	625
NTSC-M, PAL-M	Square Pixel (graphics)	24.5454	12.2727	60	525

The input pixel data for STV0117 has an integer relationship to the number of clock cycles per horizontal line as detailed in Table 2.

Table 2

Standard	Application	Pixel Clock (MHz)	Total Pixels per Line	Active Pixels per Line
PAL-B, D, G, H, I, PAL-N	CCIR601	13.5	864	720
NTSC-M, PAL-M	CCIR601	13.5	858	720
PAL-B, D, G, H, I, PAL-N	Square Pixel (graphics)	14.75	944	768
NTSC-M, PAL-M	Square Pixel (graphics)	12.2727	780	640

Square pixel and/or non-interlaced modes are updated on the beginning of the frame (see Figure 2).

In non-interlaced mode, it is a 624/2 = 312 line mode or a 524/2 = 262 line mode with waveforms like the first field of CCIR or SMPTE specifications (see Figures 3 to 10).

2 - Video Timing

The STV0117 outputs interlaced or non-interlaced video in PAL-B, D, G, H, I, PAL-N, PAL-M or NTSC-M standards.

The 8 field (for PAL) or 4 field (for NTSC) burst sequences are internally generated, with CKREF as reference.

Rise and fall times of synchronization tip, blanking and burst envelope are internally controlled according to the composite video specification.

Lines inside Vertical Interval are blanked and others included in Blanking Interval can be blanked via I^2C controls (not assumed by default).

Vertical Blanking Interval corresponds to the following lines :

- in 525/60 system : lines 1-19 and 2nd half of line 263 to line 282 (SMPTE line number convention),
- in 625/50 system : 2nd half of line 623 to line 22 and lines 311-335 (CCIR line number convention).

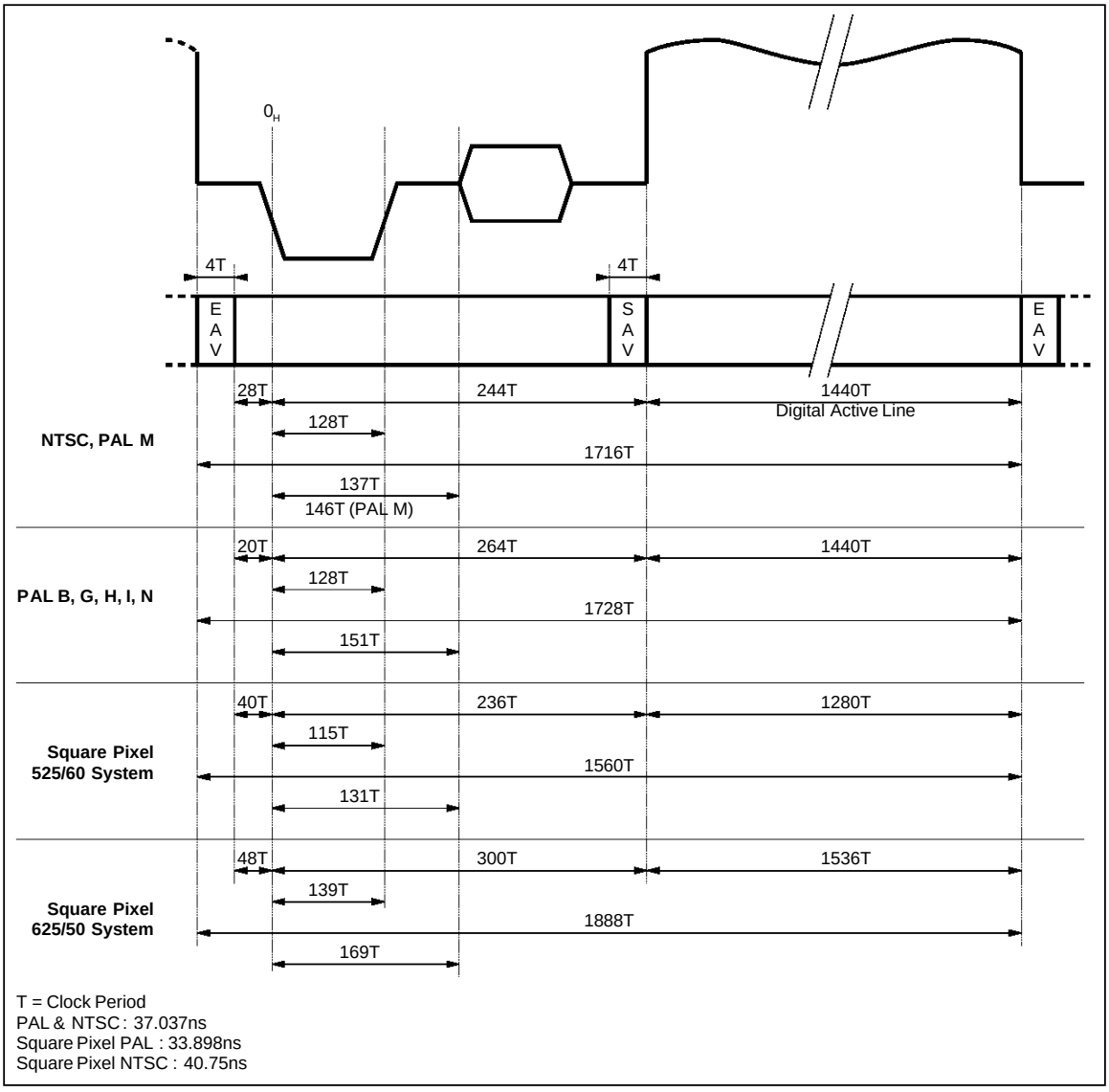
Video half lines are assumed only when preceding Vertical Interval. This is the case for the following lines :

- in 525/60 system : line 263 (SMPTE line number convention),
- in 625/50 system : line 623 (CCIR line number convention).

FUNCTIONAL DESCRIPTION (continued)

In a CCIR656 compliant digital TV line, the "active" portion of the line is the portion included between the SAV (Start of Active Video) and EAV (End of Active Video) words.
However, this digital active line starts somewhat earlier than the active line usually defined by analogue standards. The approach retained in the STV0117 is to encode the full digital line. Thus, the output waveform will reflect the full YCRCB stream included between SAV and EAV as Figure 1 reflects. Should it be absolutely necessary to obtain an analogue active line that starts later than the digital active line, a solution is to input a YCRCB stream that starts with samples at black level after the SAV word.
Autotest mode is operating when allowed by TESTAUTO Pin (HIGH level) or by I^2C programming. This mode is a master mode which encodes a color bar pattern in the appropriate selected standard (see Figure 11).

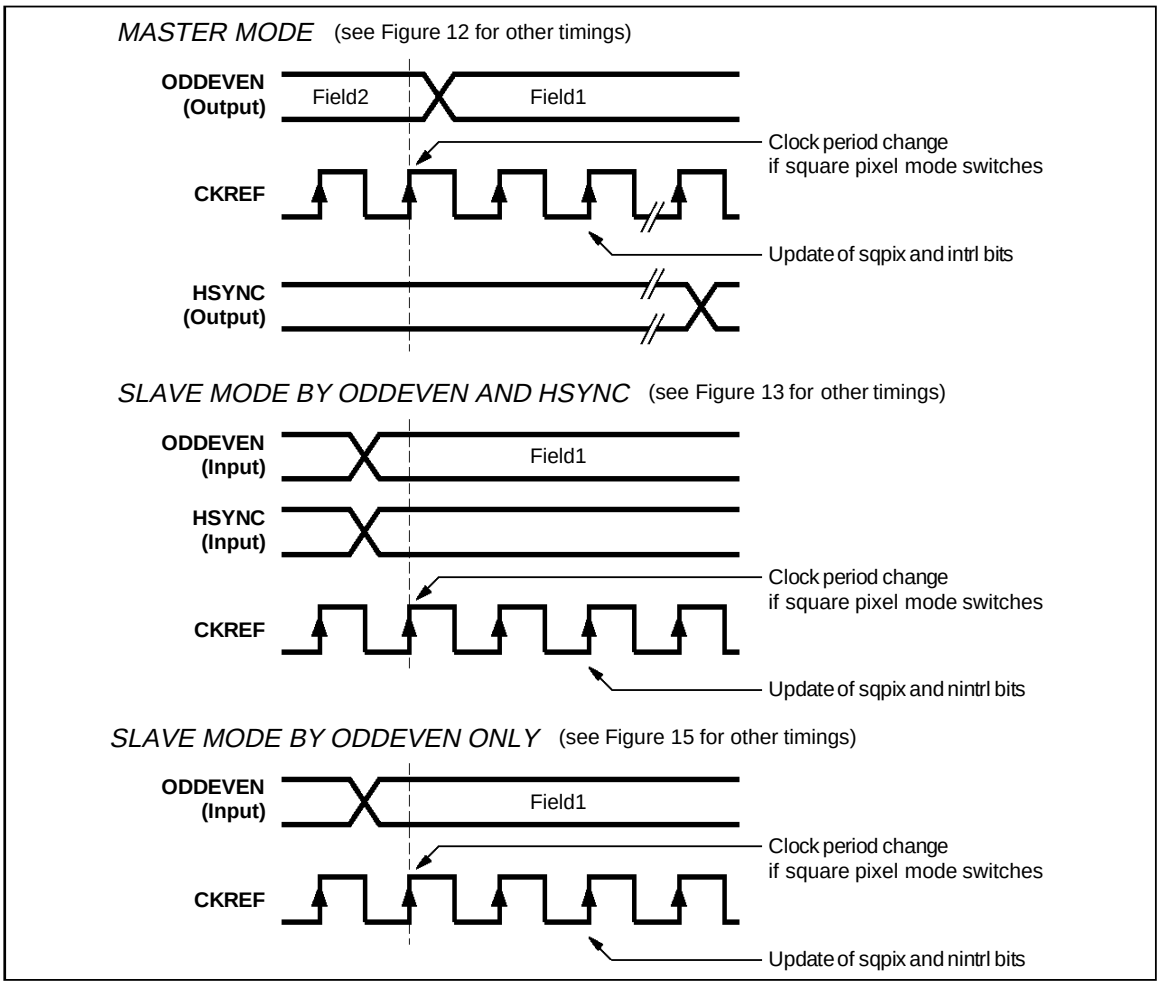
Figure 1 : Data Input Format



Note : The burst envelope shown here indicates the location from which the first subcarrier positive zero crossing is seeked (with respect to the 0_H reference). The burst always start with such a positive zero crossing.

FUNCTIONAL DESCRIPTION (continued)

Figure 2 : Square Pixel and/or Non-interlaced Mode Switch



Notes : 1. These diagrams are valid with contents of "delay" and "synchro-delay" registers equal to default value.
2. If on-the-fly format changing is required, clock switching must be synchronized onto the start of frame as shown in the above waveforms. Internally, "sqpix" and "nintrl" bits update is taken into account on beginning of new frame.

FUNCTIONAL DESCRIPTION (continued)

Figure 3 : Interlaced Mode (nintrl = 0 - I^2C) - Master Mode

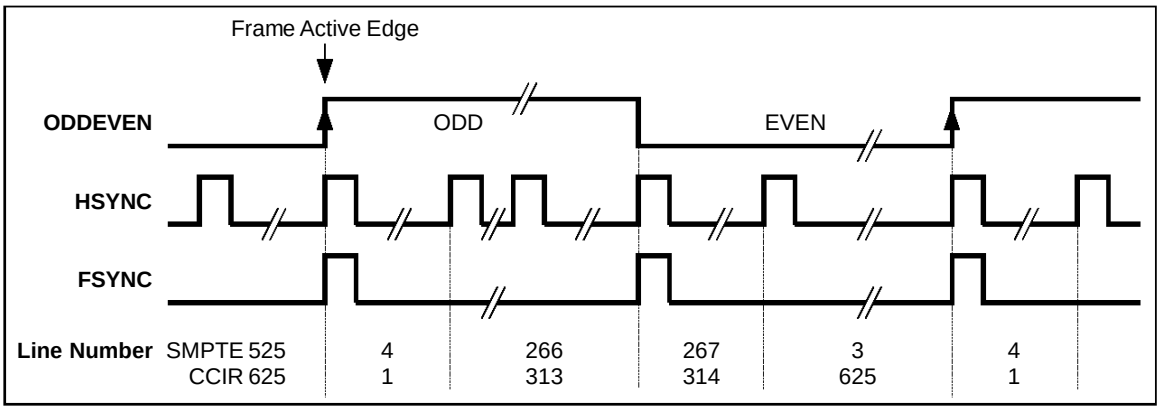
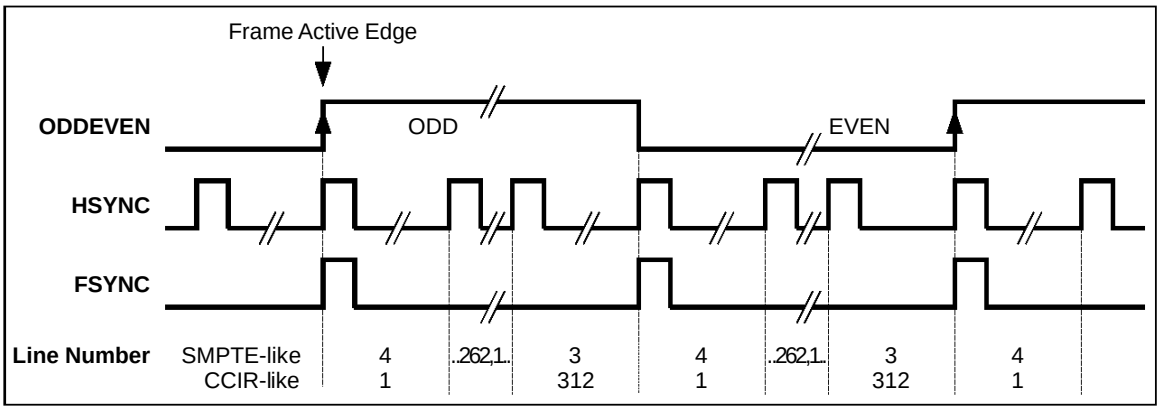


Figure 4 : Non-interlaced Mode (nintrl = 1 - I^2C) - Master Mode



Notes : 1. These diagrams are valid for sys0 = 1 and sys1 = 0 in Register 0 (i.e. synchro active edges defined as rising).
2. In slave mode, only one edge (the "active edge") of the incoming ODDEVEN is taken into account for synchronization. The "non-active edge" is not critical and its position may differ by up to half a line from the location shown in master mode.

FUNCTIONAL DESCRIPTION (continued)

Figure 5 : NTSC-M Typical VBI Waveforms (interlaced mode) (SMPTE-525 line numbering convention)

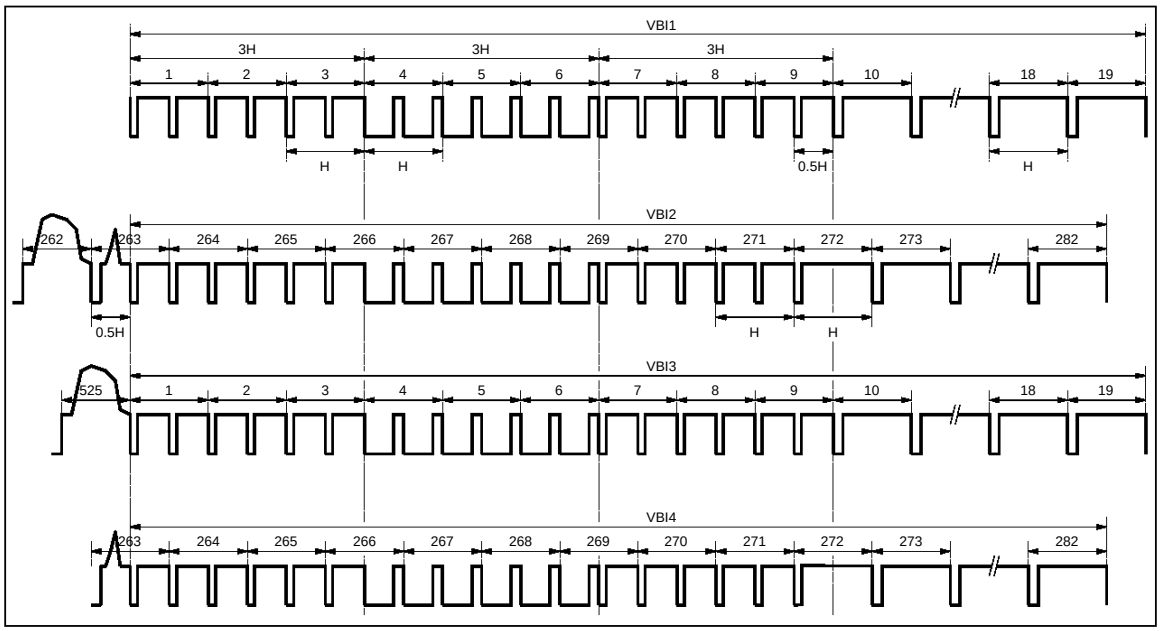
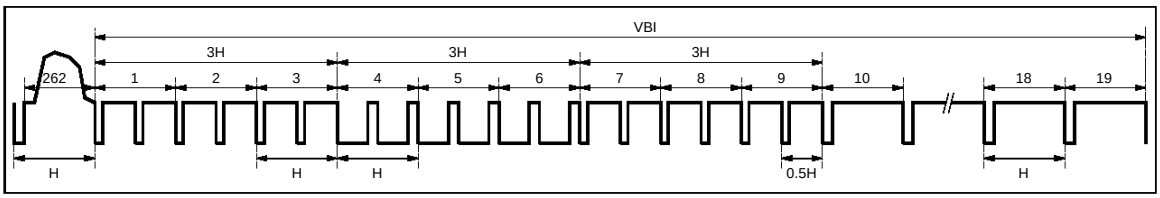
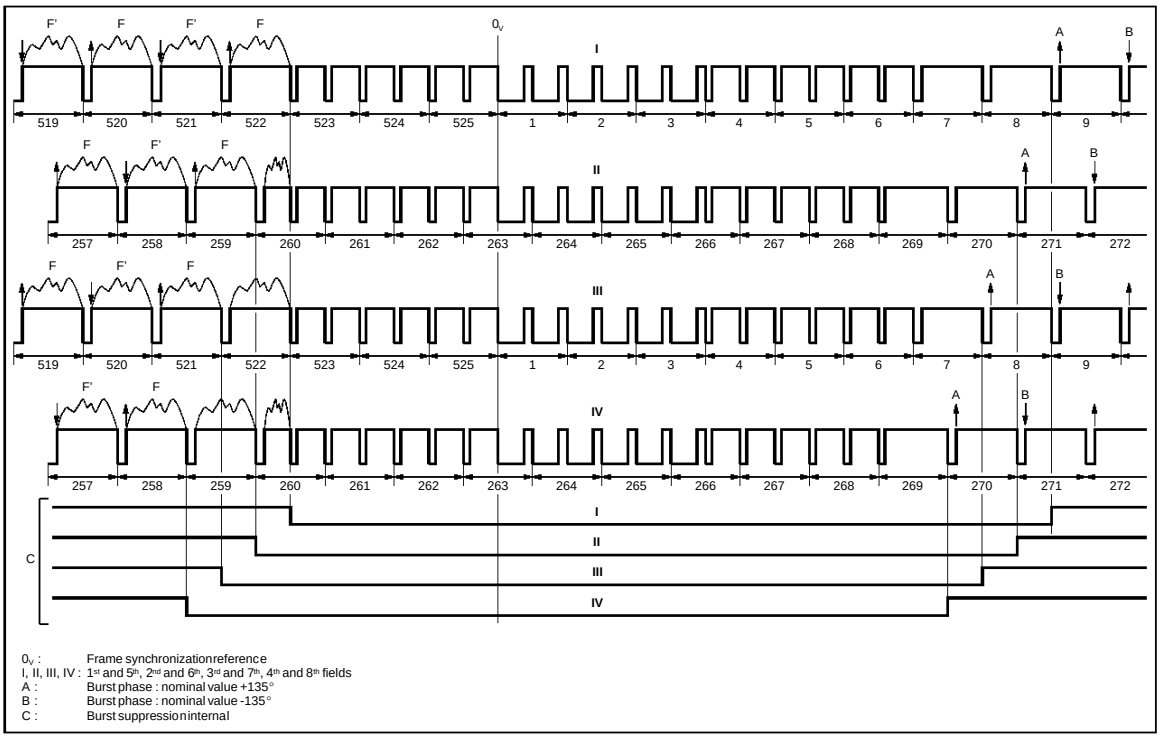


Figure 6 : NTSC-M Typical VBI Waveforms (non-interlaced mode) ("SMPTE-like" line numbering convention)



FUNCTIONAL DESCRIPTION (continued)

Figure 7 : PAL-M Typical VBI Waveforms (interlaced mode) (CCIR-525 line numbering convention)



0_V : Frame synchronizationreference
I, II, III, IV : 1st and 5th, 2nd and 6th, 3rd and 7th, 4th and 8th fields
A : Burst phase : nominal value +135°
B : Burst phase : nominal value -135°
C : Burst suppression internal

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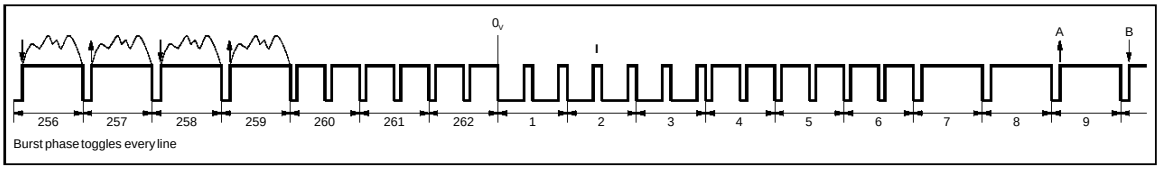
Figure 8 : PAL-M Typical VBI Waveforms (non-interlaced mode) ("CCIR-like" line numbering convention)



Burst phase toggles every line

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FUNCTIONAL DESCRIPTION (continued)

Figure 9 : PAL-BGHI Typical VBI Waveforms (interlaced mode) (CCIR-625 line numbering convention)

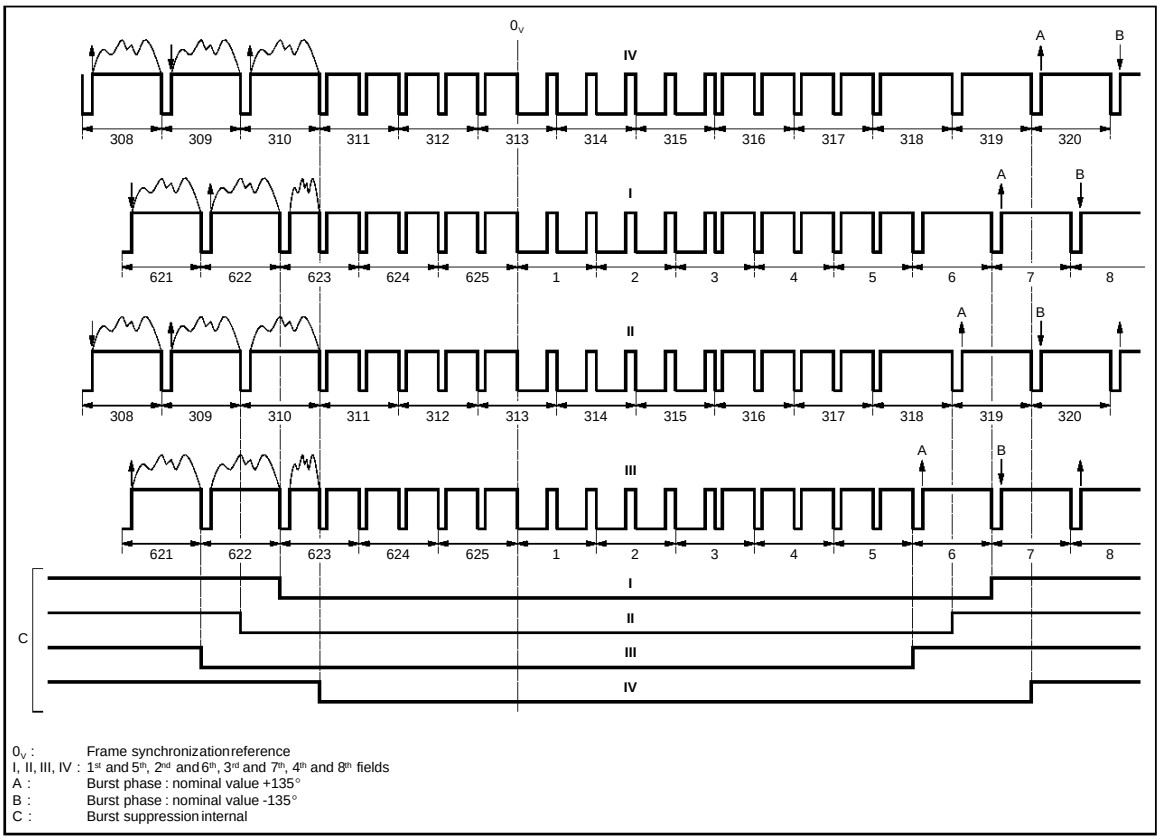

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Figure 10 : PAL-BGHI Typical VBI Waveforms (non-interlaced mode) ("CCIR-like" line numbering convention)

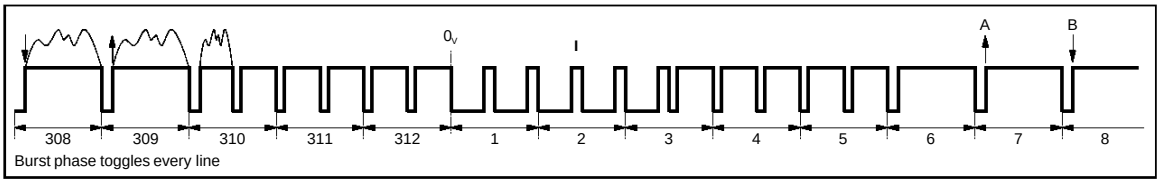

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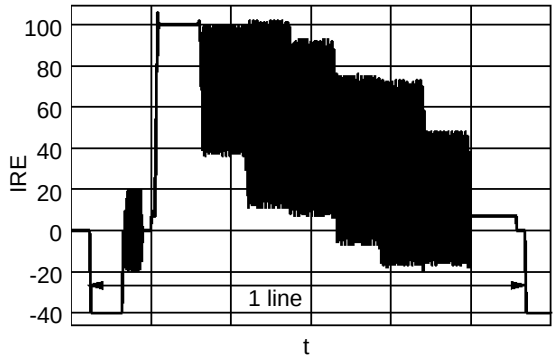
Figure 11 : Video Timing - Master Mode = Auto-test Mode - NTSC - CVBS Signal



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FUNCTIONAL DESCRIPTION (continued)

3 - Reset Procedure

A hardware reset is performed by grounding the Pin NRESET. This will set the STV0117 in slave mode driven by ODDEVEN and HSYNC input Pins, in NTSC-M standard, with CCIR601 rectangular pixel and interlaced mode encoding.
After power-on reset, MACROVISION™ copy protection process is disabled and no closed captions are encoded ; then, any I^2C bus programming and/or software reset will set the STV0117 in a customized operation mode in a partially or fully automatic way. A few I^2C registers are never reset, their contents is unknown until the first loading (see I^2C REGISTERS DESCRIPTION).

During reset hardware operation and after reset released, all digital I/O stages are set to input mode. This is the case for ODDEVEN, HSYNC signals and DVID[8:0] data.

It is also possible to perform a software reset by setting bit "softrst" in register 4. The IC's response in that case is similar to its response after a hardware reset, except that control and configuration registers are not altered (register 0 to 4).

Note that after writing a "1" into bit "softrst" (register 4), it is necessary to stop the I^2C sequence after register 4 and start a new I^2C transfer sequence to send the data for next registers.

4 - Master Mode

After a software reset, the synchronization generator starts counting the CKREF clock pulses and provides a complete repetitive composite synchronization pulse sequence. In that mode, the time base of the circuit runs continuously.
This is a 4 field sequence in NTSC-M and a 8 field sequence in PAL.
Whatever the standard, ODDEVEN signal and composite or horizontal synchronization signal (VCS/HSYNC Pin) are delivered to control an MPEG video decoder.
Non-interlaced and/or square pixel encoding is performed when selected by programmation.
The timings of sync signals depend on whether or not square pixel or non-interlaced modes have been selected and are also affected by the "delay-registers" and "synchro-delay-registers" (see Figure 12).

5 - Slave Modes

Three slave modes are selectable by the I^2C bus, bit "mod" (register 0) should be set to "0" to enable slave mode.

5.1 - Line-locked Sync

(sym2 = sym1 = "1" in register 0)

After a sofware reset, the synchronization counter waits for the rising edge of ODDEVEN and HSYNC signals sent by a video source.

In slave mode by ODDEVEN and HSYNC, the first active transition of ODDEVEN initializes the internal line counter and the simultaneous or first following active transition of HSYNC intializes a sample counter.

- If line length is shorter or equal to nominal value : sample counter is reinitialized and all internal active signals depending on sample counter are set inactive. The last pixels of the digital line are not output in that case ; however the encoded video is within the analog video requirements.
- If line length is longer than nominal value: sample counter is stopped when reaching nominal end of line and is waiting for next HSYNC active edge to reinitialize itself.

Note that the phase relationship between HSYNC and the incoming YCRCB data should be such that the first clock rising edge following the HSYNC active edge always samples "Cb" (see Figure 13).

Field count is incremented on each ODDEVEN transition. Line counter is reset on each active edge of ODDEVEN.

5.2 - Frame-locked Sync

(sym2 = sym1 = "0" in register 0)

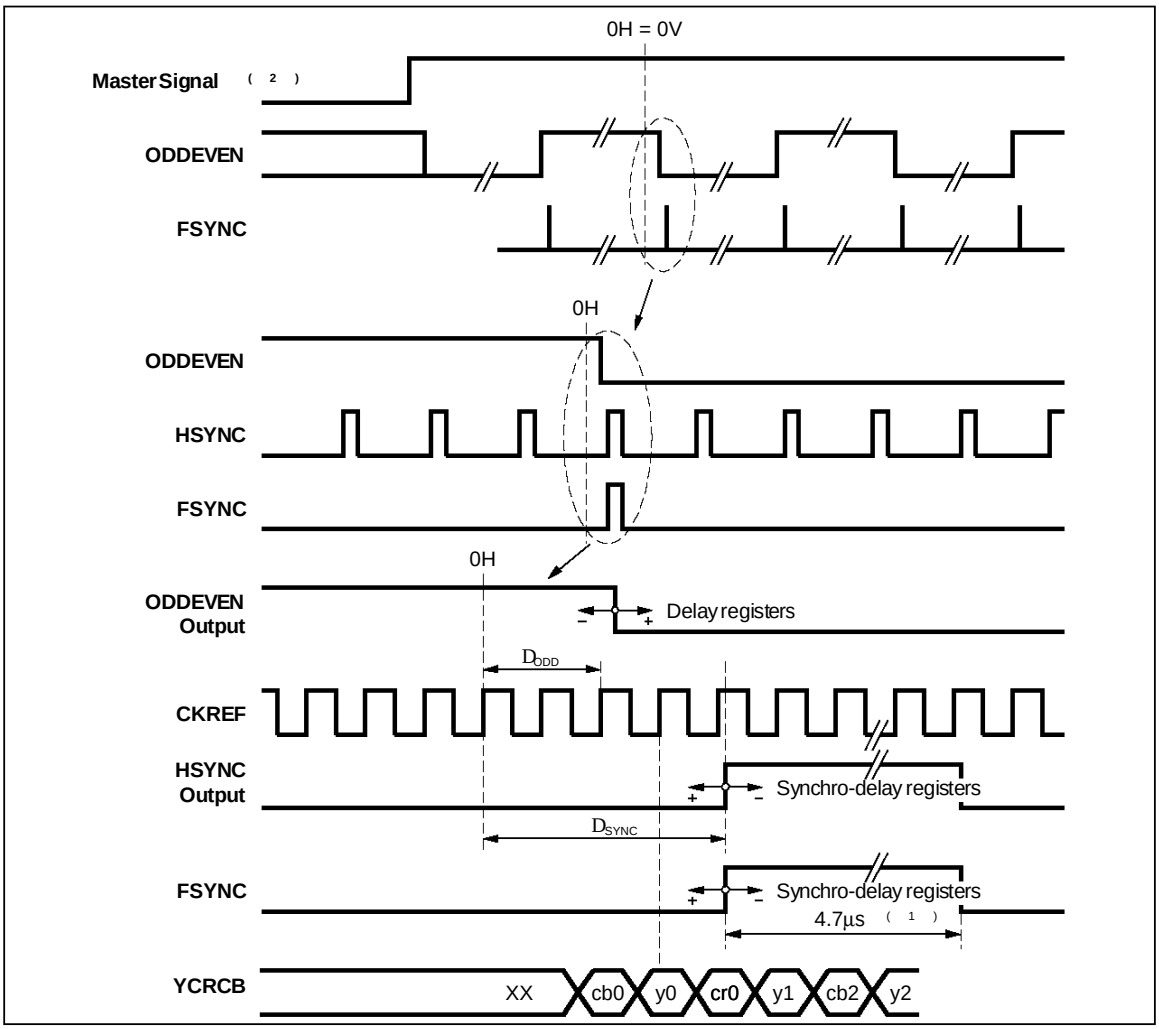
Alternatively, slave mode can be performed with ODDEVEN input only, or STV0117 can be set to extract the synchronization from YCRCB input data sequence (F : ODDEVEN signal from EAV sequence (see Figure 14)).

After a sofware reset, the synchronization counter waits for the first active edge of ODDEVEN or F first falling edge sent by a digital video source. Once the appropriate sync signals have been selected, a sequence identical to that in master mode can start and is repeated until 3 consecutive checks on ODDEVEN location fail. In the latter case, the IC stops outputting HSYNC and, if applicable, ODDEVEN, and blanks the video outputs until a new rising edge occurs on ODDEVEN onto which it locks again (see Figure 15).

Note that the phase relationship between ODDEVEN and the incoming YCRCB data should be such that the first clock rising edge following the ODDEVEN active edge always samples "Cb".

FUNCTIONAL DESCRIPTION (continued)

Figure 12 : Master (with sys0 = 0 and sys1 = 0 - I^2C Register 0)



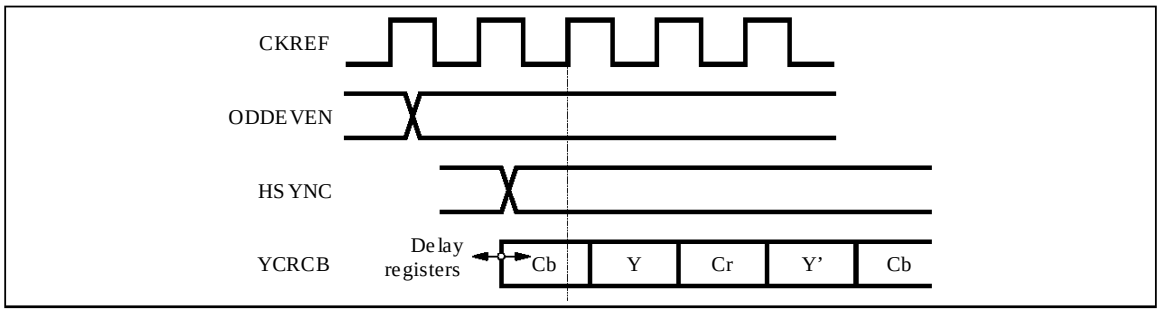
Notes : 1. These diagrams are valid when delay registers not loaded (default values) :
If delay register value < 0, then ODDEVEN edge is shifted left, else ODDEVEN edge is shifted right.
If synchro_delay register value < 0, then HSYNC and FSYNC edges are shifted right, else they are shifted left.

2. Master signal goes to 1 when soft/hard autotest mode or master mode is selected.

3. To keep the CB, Y, CR sequence correct, synchro-delay register must be changed **four steps by four steps.**

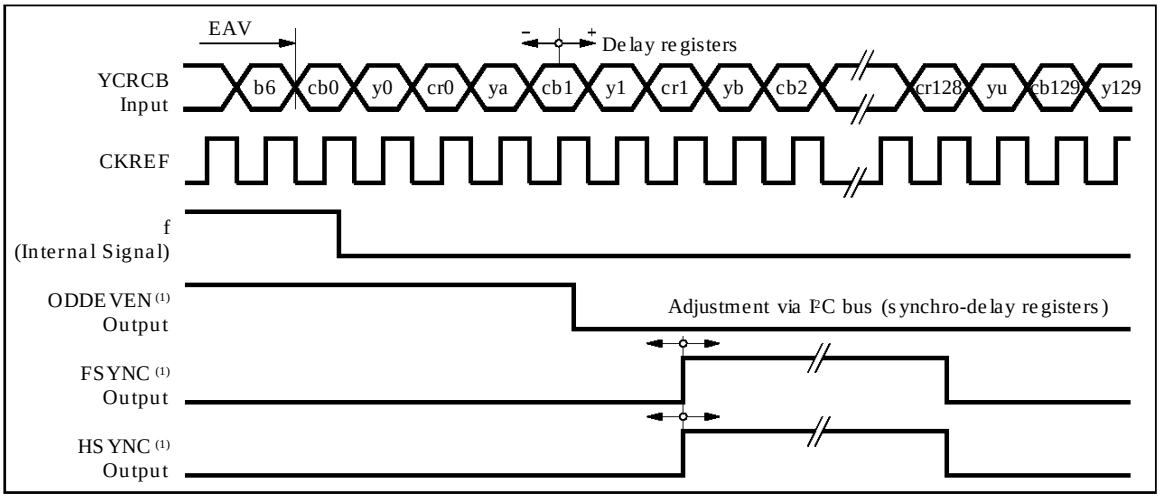
FUNCTIONAL DESCRIPTION (continued)

Figure 13 : HSYNC + ODDEVEN Based Slave Mode Sync Signals



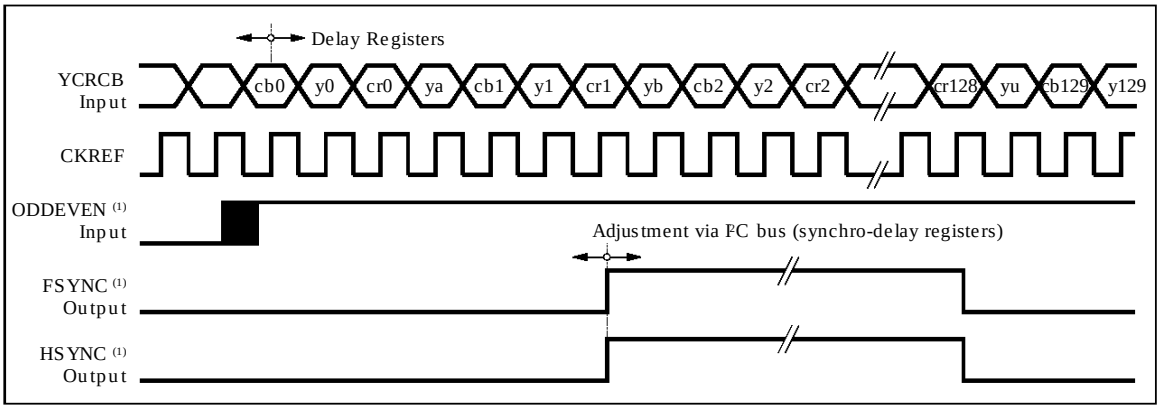
Notes : 1. Diagram valid for contents of "delay" and "synchro-delay" register = default.
2. In ODDEVEN + HSYNC synchronization mode, ODDEVEN and HSYNC may change level at the same time, alternatively ODDEVEN can change first and the next HSYNC flags the start of the first line of the frame.

Figure 14 : Slave Mode, Synchro by F (extracted from EAV) (1)



Note : 1. Diagram valid if both registers delay and synchro-delay are not loaded (default values).

Figure 15 : Slave Mode, Synchro by ODDEVEN



Note : 1. Diagram valid if both registers delay and synchro-delay are not loaded (default values).

FUNCTIONAL DESCRIPTION (continued)

6 - Chrominance Encoding

The demultiplexed CB, CR samples feed a chrominance Q/I matrix for NTSC-M (or a U/V matrix for PAL). The Q/I or U/V signals are then band limited according to CCIR Rec624 and interpolated at CKREF clock rate. This processing makes easier the filtering for D/A conversion and allows a more accurate encoding.

For modulation with the color subcarrier signal, the U/V or Q/I components are band limited to 1.3MHz for U/V and I, and to 0.5MHz for Q. In case of data issued from a graphics source, bandwidth can be extended to 1.8MHz for all components (see Figures 16, 17, 18 and 19 for curves of the different filters).

Figure 16 : Chroma Q Filter

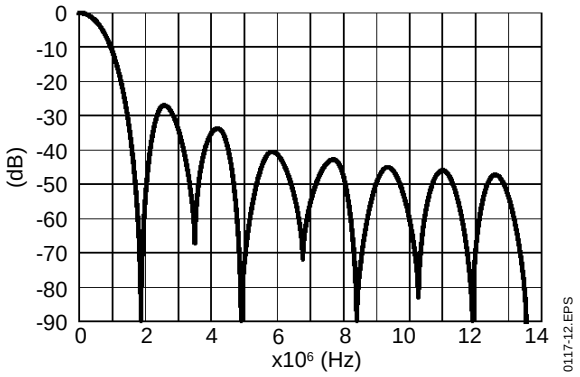


Figure 17 : Chroma Q Filter (zoom)

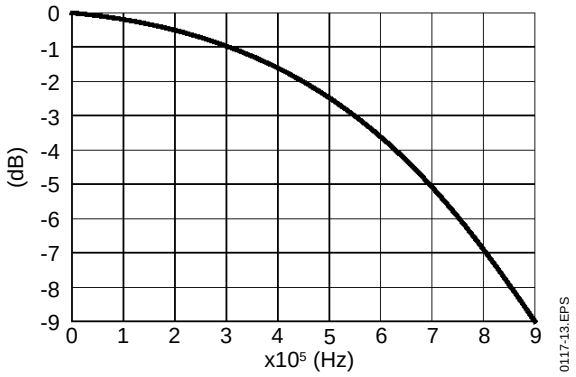


Figure 18 : Chroma Filters

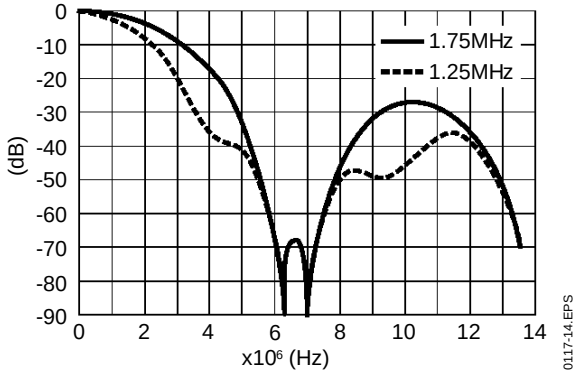
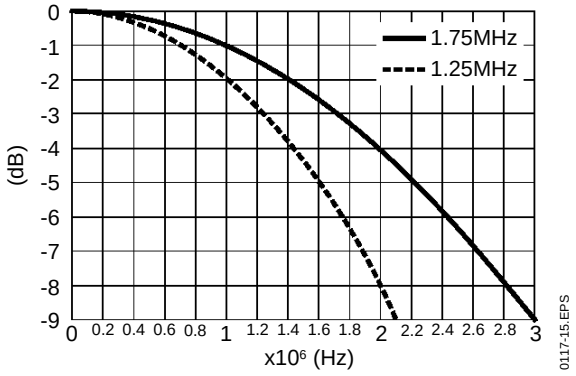


Figure 19 : Chroma Filters (zoom)



Note : Those filter curves include the sinX/X attenuation of DACs.

FUNCTIONAL DESCRIPTION (continued)

7 - Color Subcarrier Generator

A Direct Digital Frequency Synthesizer (DDFS), using a 22-bit phase accumulator, generates the required color subcarrier frequency. This oscillator feeds a quadrature modulator which modulates the baseband chrominance signal components.

Color subcarrier frequency is computed according to the following equation :

$$Fsc = (22\text{-bit increment word}/2^{22}) \times CKREF$$

The phase and frequency of the color subcarrier can be adjusted by software.

The external clock is considered to be sufficiently stable to ensure correct encoding.

When performing external Gen-locking, the frequency reference of the generated clock may slightly deviate depending on the line length measurement. To prevent this drift from corrupting the colors, the color subcarrier frequency control line (CFC Pin) can be used to update the 22-bit increment of the DDFS and keep the color subcarrier stable (see Figure 20).

Internal I^2C options provide a reset of color subcarrier phase every 2, 4 or 8 fields to compensate for any drift introduced by the finite accuracy of the calculations.

8 - Burst Insertion

The start time of the color burst is at the positive zero crossing of the color subcarrier sinusoïdal waveform that follows a burst window. This window location is given in Table 3.
The first and last half cycles have a reduced amplitude so that the burst envelope starts and ends smoothly.

Table 3

Standard	Application	CKREF Frequency (MHz)	Burst Window Location from 0H
PAL-B, D, G, H, I, PAL-N	CCIR601	27	+151 CKREF periods
NTSN-M	CCIR601	27	+137 CKREF periods
PAL-M	CCIR601	27	+146 CKREF periods
PAL-B, D, G, H, I, PAL-N	Square Pixel (Graphics)	29.50	+169 CKREF periods
NTSN-M, PAL-M	Square Pixel (Graphics)	24.5454	+131 CKREF periods

The burst is inserted for 9 (M and PAL-N standards) or 10 (PAL-B, D, G, H, I) subcarrier cycles.

Phase shift is directly performed within the DDFS during the burst insertion as specified in Table 4.

Table 4

Standard	Subcarrier Freq. (MHz) CCIR601/ Square Pixel	Phase Shift per Line (Degrees)
PAL-B, D, G, H, I	4.43361875	-90 (plus line alternance)
PAL-N	3.5820558	+90 (plus line alternance)
NTSC-M	3.5795452	+180
PAL-M	3.57561149	+90 (plus line alternance)

Note that except in square pixel mode, subcarrier frequencies can readily be customized with the following procedure :

- Program the required increment in registers 10 to 12.
- Set bit "selrst" to "1" in register 2.
- Perform a software reset (register 5).

9 - Luminance Encoding

The demultiplexed Y samples are band limited and are interpolated at CKREF clock rate. Then a gain and offset compensation is applied to the luminance signal before inserting closed captions data, Macrovision copy protection signals and synchronization pulses.

A 7.5 IRE pedestal is selected automatically in the 60Hz field rate mode and may be added in 50Hz field rate mode to distinguish 2 PAL-N standards (see I^2C REGISTERS DESCRIPTION).

The interpolation filter compensates the sinx/x attenuation of D/A conversion and greatly simplifies the external output stage filter (see Figures 21 and 22 for curves).

A programmable delay is inserted on the luminance data path to offset any chroma/luma delay introduction by off-chip filtering (see I^2C REGISTERS DESCRIPTION).

By default, luminance and chrominance transitions are aligned on analogue outputs.

FUNCTIONAL DESCRIPTION (continued)

Figure 20 : Color Subcarrier Frequency Control Word Transmission Format

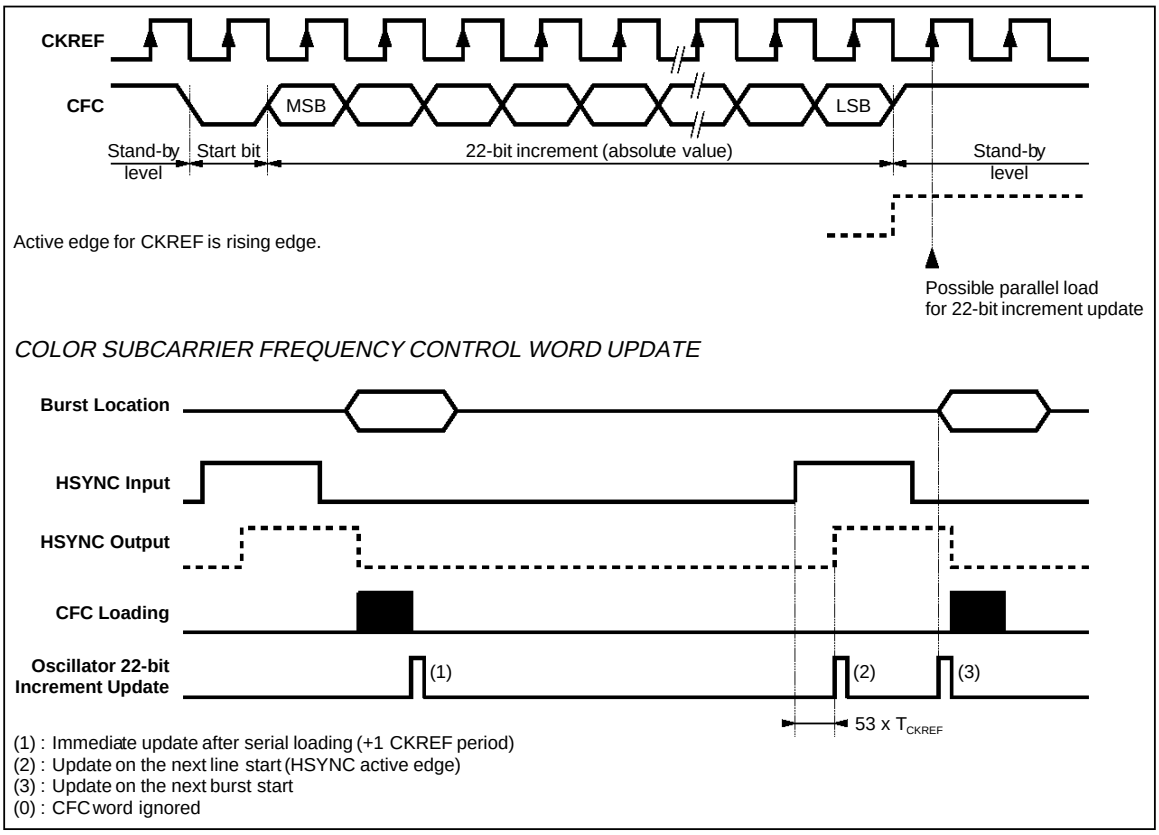


Figure 21 : Luma Filters

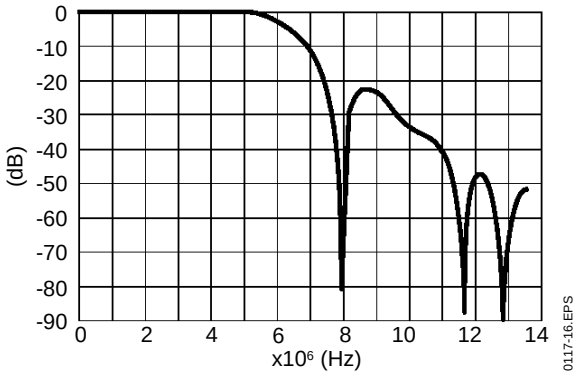
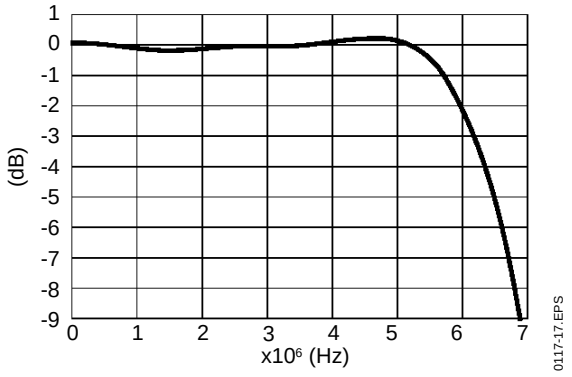


Figure 22 : Luma Filters (zoom)



Note : Those filter curves include the sinX/X attenuation of DACs.

FUNCTIONAL DESCRIPTION (continued)

10 - Closed Captions Encoding

Data, according to the closed caption specifications, or extended data service can be encoded by the circuit. The closed caption data is delivered to the circuit through the I^2C bus control interface. Two dedicated pairs of bytes (two bytes per field), each pair preceded by a clock run-in and a start bit can be encoded and inserted on the luminance path on a selected line. The serial I^2C loading should be performed odd-parity bit first, then MSB of the US-ASCII 7-bit character and LSB last. I^2C Register 39 (resp. register 41) is the first byte sent (LSB first) after the start bit on the appropriate TV line in field1 (resp. field2), and register 40 (resp. register 42) is the second byte. The TV line number where data is to be encoded is programmable (see I^2C REGISTERS DESCRIPTION). A Direct Digital Frequency Synthesizer (DDFS), using a phase accumulator, generates the required run-in frequency. The phase and frequency of the run-in oscillator are generated for different standards. The nominal instantaneous data rate is 503496.5Hz (i.e. 32 times the NTSC line frequency). Should closed-captioning be needed in conjunction with PAL, this same data clock frequency would still be used, and all closed-caption absolute timings would be unchanged. Closed captions can also be encoded in square pixel mode and the nominal data rate keeps the same. Data LOW corresponds nominally to 0 IRE, data HIGH corresponds to 50 IRE at the DAC outputs. When closed-captioning is on, the microcontroller should load the relevant registers (reg. 39 and 40, or 41 and 42) once every frame (possibly less) in average. The closed caption encoder considers that the closed caption data has been loaded and is valid on completion of the write operation into register 40 for field1, into register 42 for field 2. If closed caption encoding is on and no new data bytes have been written into the closed caption data registers when the closed caption data slot starts on the appropriate TV line, then the circuit outputs two US-ASCII NULL characters with odd parity after the start bit (see Figures 23, 24, 25 and 26).

Figure 23 : Closed Caption Line
CKREF = 27MHz - NTSC-M
CVBS Analog Signal

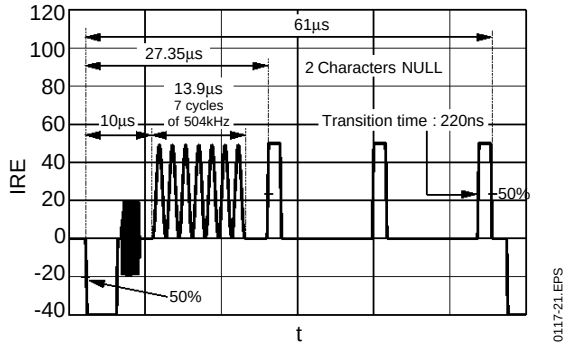


Figure 24 : Closed Caption Line
CKREF = 27MHz - PAL/CCIR
CVBS Analog Signal

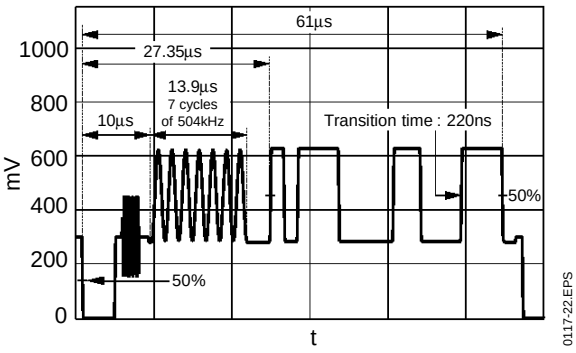


Figure 25 : Closed Caption Line
CKREF = 24.5454MHz - NTSC-M
CVBS Analog Signal - Square Pixel

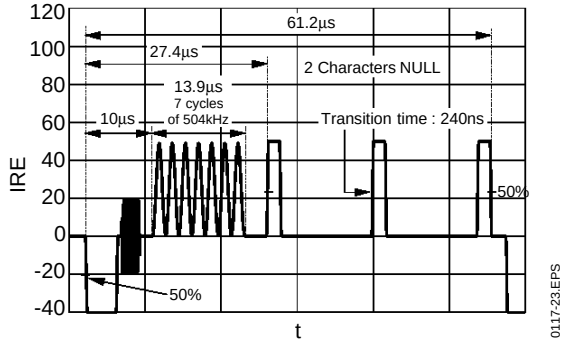
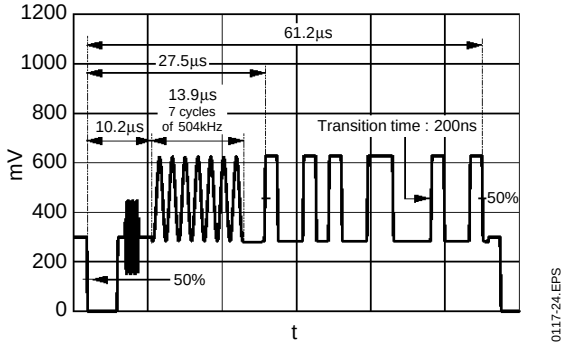


Figure 26 : Closed Caption Line
CKREF = 29.5MHz - PAL 625 Lines
CVBS Analog Signal - Square Pixel



FUNCTIONAL DESCRIPTION (continued)

11 - CVBS and SVHS Outputs

No luminance band-stop filter is implemented to remove chrominance from the luminance part of the composite video channel.

Each digital video signal drives a 9-bit D/A converter operating at CKREF clock rate.

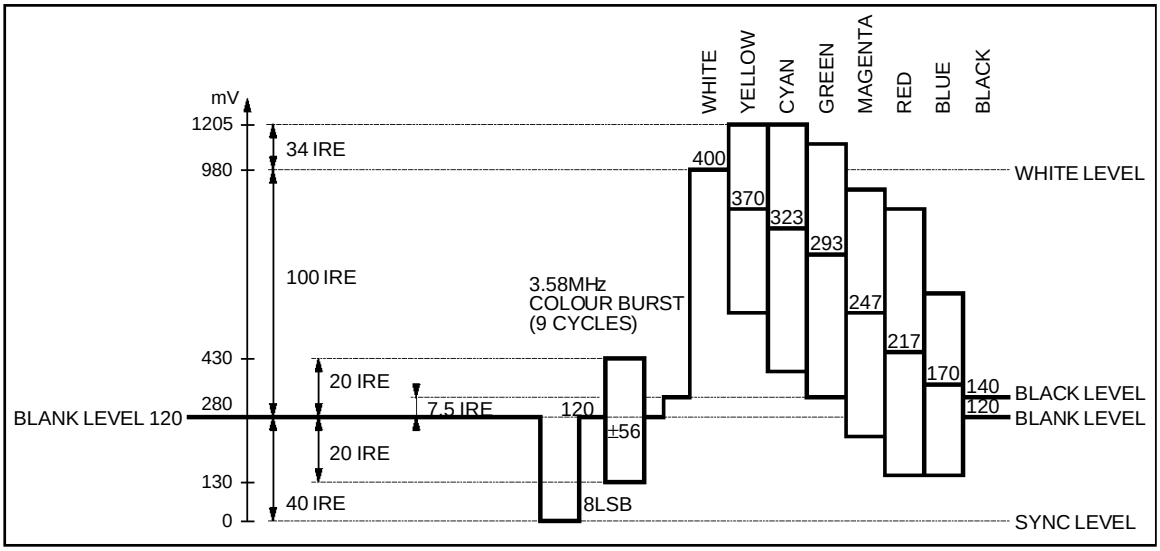
The outputs are current sources and are proportional to the current reference source (I_{REF} Pin). The integrated oversampling stages make the external antialiasing low pass filters simpler (see Figures 27, 28 and 29).

Unused DAC must be connected to ground and disabled via I^2C control (separate power-down modes).

Table 5

Signal	Resolution	Maximum Voltage (I_{REF} = 2mA, R_L= 300Ω)
CVBS	9 bits	$1.24V_{PP}$
C	9 bits	$1.24V_{PP}$ ($0.8V_{PP}$ nominal for 100/0/100 625l color bar)
YS	9 bits	$1.24V_{PP}$ ($1.0V_{PP}$ nominal for 100/0/100 625l color bar)

Figure 27 : M Composite NTSC Output (100% Saturation, 100% Amplitude Color Bars)



FUNCTIONAL DESCRIPTION (continued)

Figure 28 : Composite PAL-B, G, D, H, I, PAL-N (if no setup) Output (100% Saturation, 100% Amplitude Color Bars)

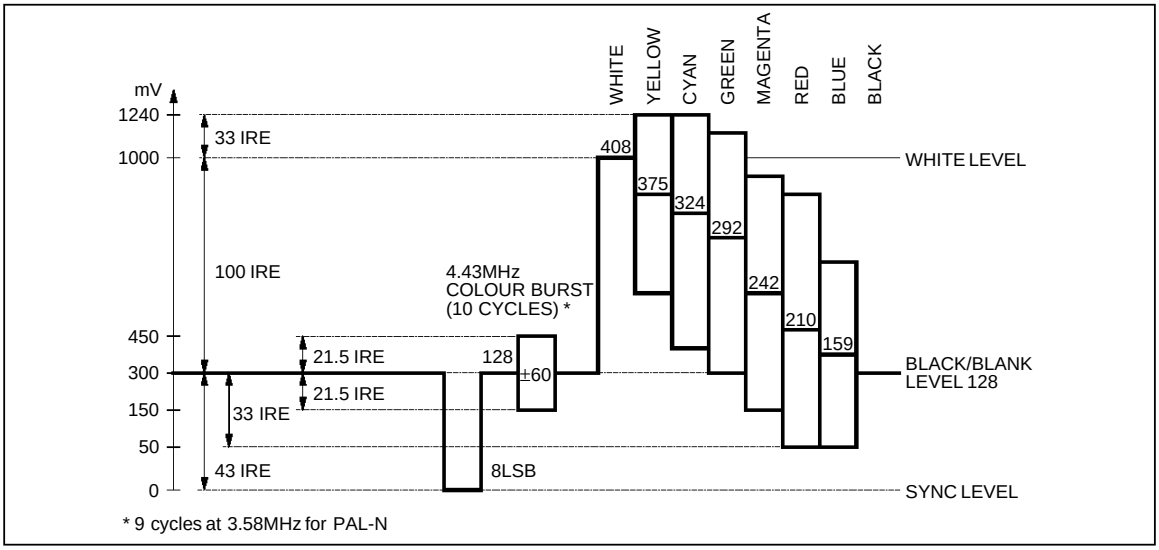
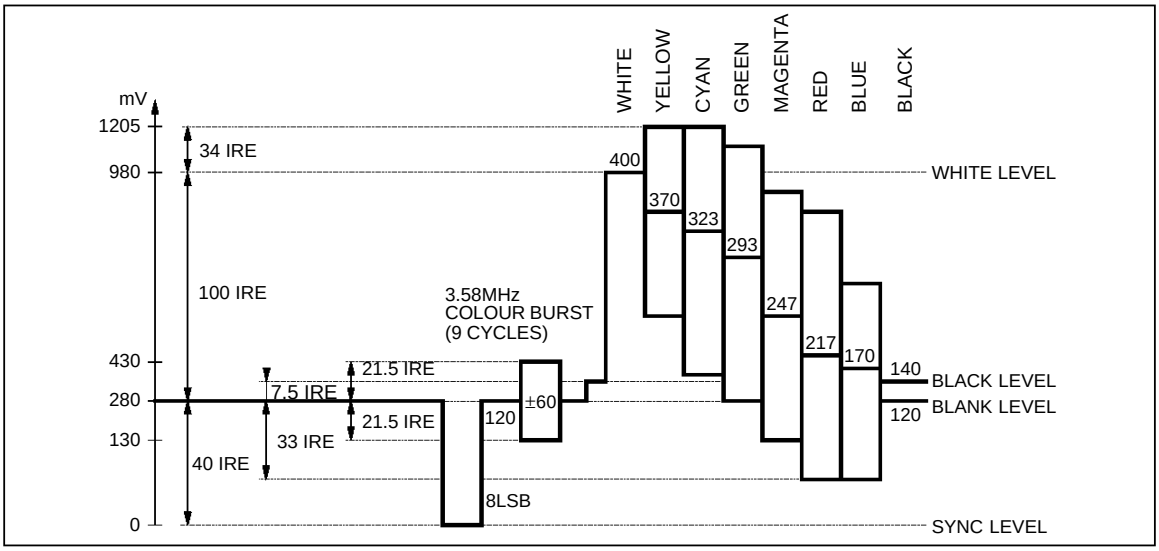


Figure 29 : Composite PAL-M Output (100% Saturation, 100% Amplitude Color Bars)



12 - OSD Inputs

FB (Fast Blanking) input controls the switching from YCRCB normal input data to Ri, Gi, Bi transcoded inputs. These inputs must be locked to HSYNC, ODDEVEN and CKREF or H6OSD signals. They are latched on the rising edge of CKREF clock signal.

Ri, Gi, Bi inputs allow 8 color combinations that will address a 3 x 8 x 6-bit CLUT. Each of the 8 values will address 3 x 6-bit samples CB, Y, CR that will be extended to 8-bit samples to fit with normal input samples. Y samples will be filtered to make sure that their bandwith is similar to YCRCB input samples. Mixing between OSD data and YCRCB normal input is performed before filtering stages.

H6OSD output clock signal is dedicated to output stage of external OSD generator. The latter is synchronized with HSYNC and ODDEVEN (or FSYNC) signals (see Figures 30, 31 and 32).

FUNCTIONAL DESCRIPTION (continued)

Figure 30 : OSD Data Insertion

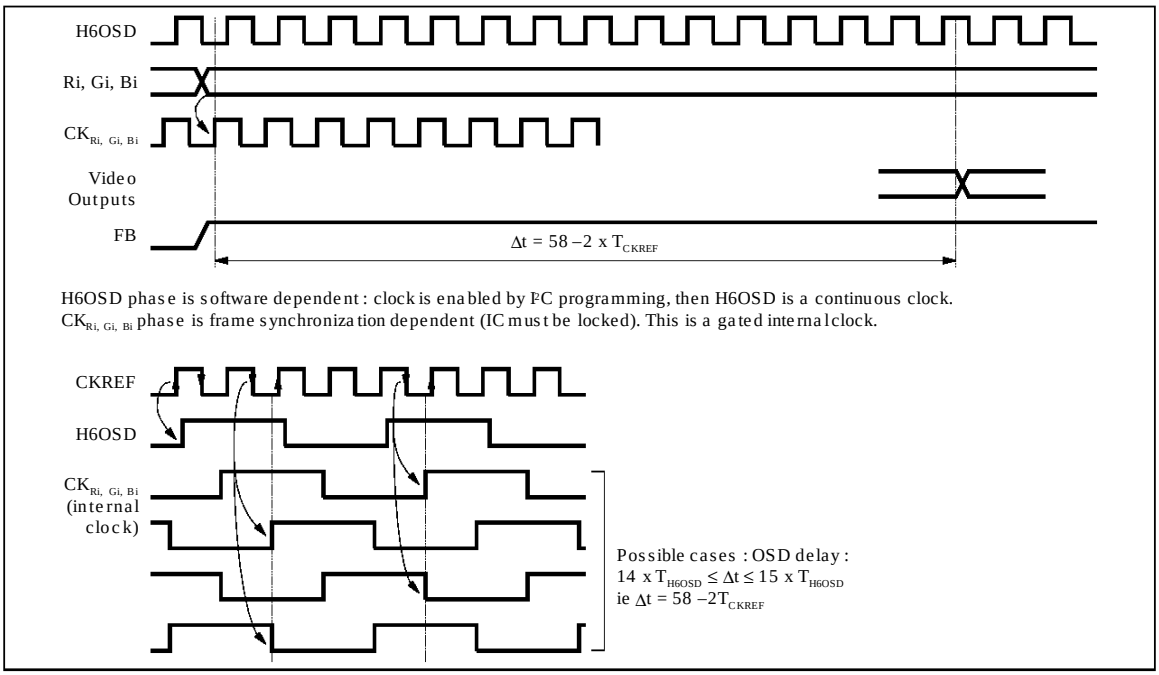
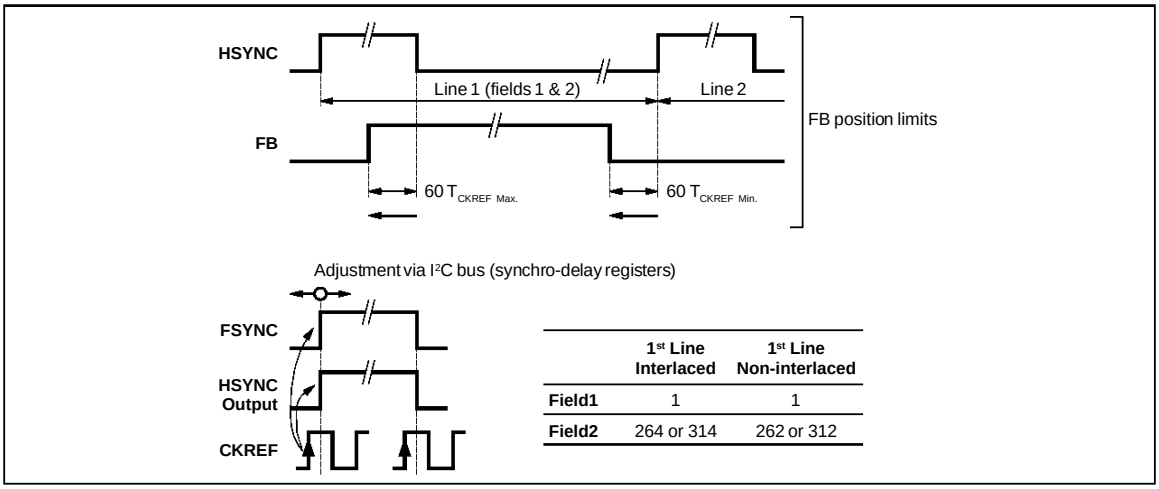
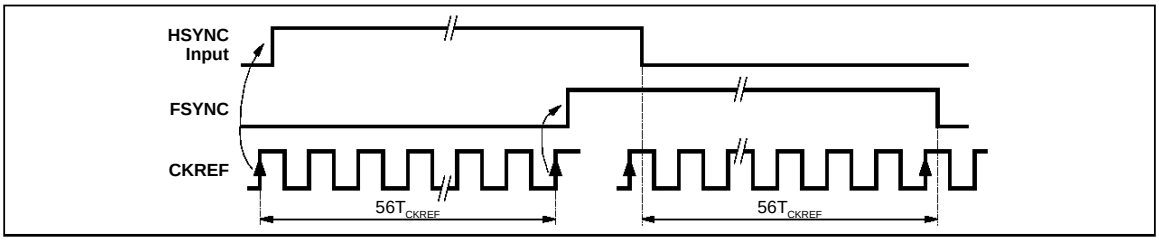


Figure 31 : OSD Synchronization Timing : Master Mode or Slave Mode (by ODDEVEN or F from YCRCB data)



	1st Line Interlaced	1st Line Non-interlaced
Field1	1	1
Field2	264 or 314	262 or 312

Figure 32 : OSD Synchronization Timing : Slave Mode (ODDEVEN and HSYNC)



FUNCTIONAL DESCRIPTION (continued)

13 - Hamming Decoding

If the timing reference sequence is present in YCRCB input data, then EAV and SAV are Hamming decoded. Only F signal is extracted from EAV and can be used in slave mode as the frame synchronization input signal.

Hamming decoding on EAV and SAV words give an information on signal transmission; multiples errors are detected and a flag is set to inform the microcontroller if it is interested in Hamming decoding results (see STATUS I^2C REGISTER).

14 - Digitized Video Input

DVID 9-bit digital input from a digitized analog video source can be directly routed to CVBS DAC input. DVID data is latched on the rising edge of CKREF clock signal.

This access is controlled by hardware (EDVID Pin) or by I^2C programmation (see Figures 33 and 34).

15 - Pinning Compatibility with STV0116

The STV0116 is a PAL/NTSC digital encoder device that has 3 additional D/A converters for R, G, B encoded analog outputs. It does not support either closed captions encoding or MACROVISION™ copy protection process. It is a CCIR601 interlaced mode encoder. It does not offer the possibility to convert a digitized video input into an analog CVBS output, (like DVID in STV0117). It does not support the slave mode by ODDEVEN and HSYNC, (it has no HSYNC input) (see Figure 35).

16 - I^2C Bus Waveforms

STV0117 IC is controlled by an I^2C bus and internal 8-bit registers can be addressed in write or read mode. Write and read operations are detailed in Figures 36 and 37.

Figure 33 : Digitized Video Timing

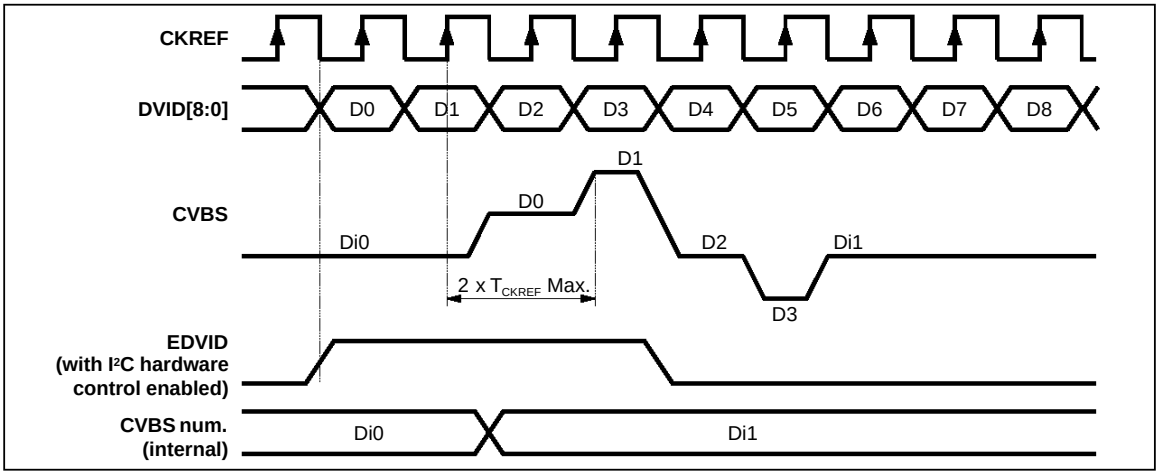
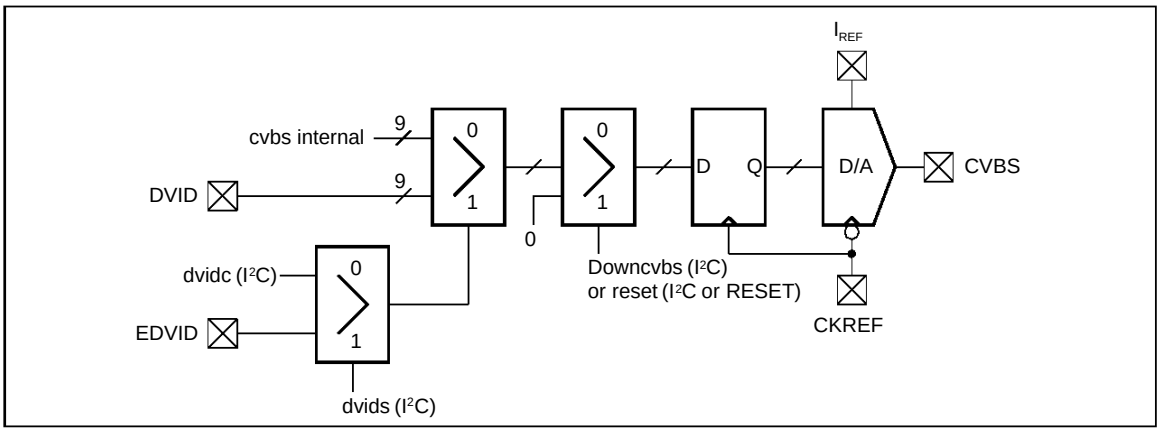
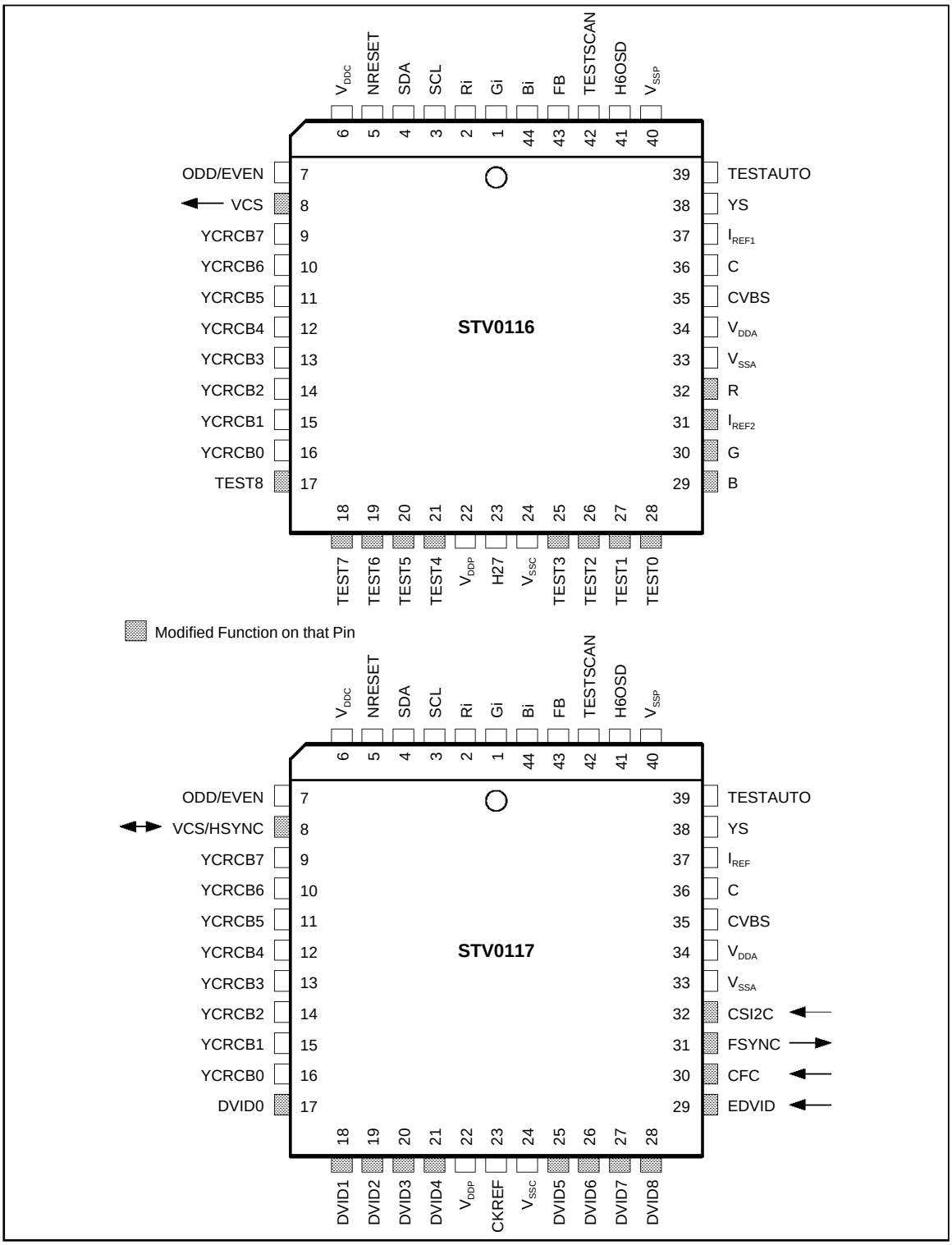


Figure 34 : Digitized Video Interface



FUNCTIONAL DESCRIPTION (continued)

Figure 35 : Pinning Compatibility with STV0116



FUNCTIONAL DESCRIPTION (continued)

Figure 36 : STV0117/I²C Write Operation (CSI2C = 0)

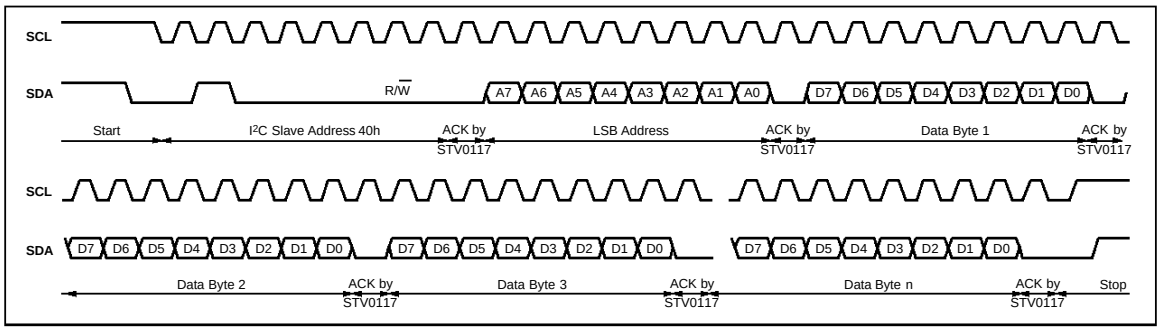
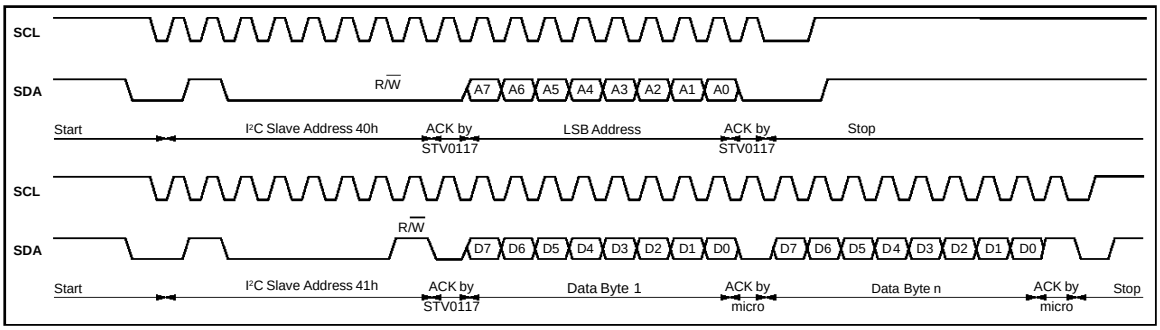


Figure 37 : STV0117/I²C Read Operation (CSI2C = 0)



MACROVISION™ COPY PROTECTION PROCESS

When enabled, the chrominance, the luminance and the composite video signals are simultaneously modified according to the MACROVISION™ copy protection process for PPV applications, revision 6.0/6.1 dated September, 18, 1995.

The control of this process is performed via I²C bus.

For more information , please contact your nearest SGS-THOMSON Microelectronics sales office.

The programming document is provided to ONLY those customers of SGS-THOMSON who have executed a license or a non-disclosure agreement with MACROVISION Corporation. Sample request and sales orders require the following procedure :

Sample Requests Procedure for Non-licensed Customers

- Contact VP Sales & Marketing, ACP-PPV
  MACROVISION Corporation
  Phone : (408) 743-86-00
  Fax : (408) 743-86-10
- MACROVISION will send an NDA to the customer
- The NDA will initiate the sampling process whereby the customer may receive MACROVISION capable ICs from SGS-THOMSON
- Samples will then be sent to the customer

Sales Orders

- If the customer has a MACROVISION™ license :
  The customer provides SGS-THOMSON with a written confirmation of the license.
  Marketing will retain the written confirmation.
  Customer can then purchase part.
- If the customer DOES NOT HAVE a MACROVISION™ license :
  The customer must obtain a license or waiver from MACROVISION.
  The customer must provide SGS-THOMSON with a written confirmation of the license or waiver from MACROVISION.
  Marketing retains the written confirmation.
  Customer purchases part.

Neither parts nor programming information will be sent to the customer until the above conditions are met.

MACROVISION™ 6.0/6.1 copy protection process programming guide *(a confidential document).*

Contact Video Marketing SGS-THOMSON Microelectronics - Grenoble (France) - Fax : (33) 76-58-56-10

Note : For customers who do not need MACROVISION™ copy protection process, a modified version of STV0117 device can be available upon specific request.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DDx}	DC Supply Voltage	-0.3, 7.0	V
V_{IN}	Digital Input Voltage	-0.3, V_{DD} + 0.3	V
V_{OUT}	Digital Output Voltage	0, V_{DD}	V
I_{REF}	Analog Input Reference Current	7	mA
I_{OUT}	Analog Output Current	15	mA
T_{oper}	Operating Temperature	0, +70	°C
T_{stg}	Storage Temperature	-40, +150	°C
P_{tot}	Total Power Dissipation	1000	mW

0117-02.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th(j-a)}$	DC Junction-Ambient Thermal Resistance with sample soldered on a PCB	Typ.	54	°C/W

0117-03.TBL

DC ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C/70°C, V_{DDA} = V_{DDC} = V_{DDP} = 5V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
V_{DDA}	Analog Positive Supply Voltage		4.75	5	5.25	V
V_{DDP}	Digital Output Buffer Supply Voltage		4.75	5	5.25	V
V_{DDC}	Digital Core Supply Voltage		4.75	5	5.25	V
I_{DDA}	Analog Current Consumption	I_{REF} = 3.5mA, R_L = 300Ω, C_L = 50pF, CKREF = 30MHz, autotest mode, static input signals	10		28	mA
I_{DD}	Digital Current Consumption		40		90	mA
DIGITAL INPUTS						
V_{IL}	Input Voltage	Low level (any other pins)	-0.3		0.8	V
V_{IH}	Input Voltage	High level (any other pins)	2.4		V_{DD}-0.5	V
I_L	Input Leakage Current	V_{IL} min or V_{IH} max			± 10	µA
C_{IN}	Input Capacitance				10	pF
SDA OUTPUT						
V_L	Output Voltage	Low level, I_O = 3mA			0.4	V
I_O	Output Current	During Acknowledge	3			mA
DIGITAL OUTPUT						
V_{OH}	Output Voltage	High level (standard TTL load)	2.4		V_{DD}	V
V_{OL}	Output Voltage	Low level (standard TTL load)	0		0.6	V
D/A CONVERTER						
I_{REF}	Reference Current Source for 3 D/A Converters		2	3	6	mA
R_L	External Load Resistance	with I_{REF} = 2.9mA		300		Ω
I_G	Current Gain	I_{REF} = 2.9mA, R_L = 300Ω, Max. code	1.9	2.1	2.3	
GE	DAC to DAC Gain Matching (YS, C)	I_{REF} = 2.9mA, R_L = 300Ω	0.5	3	3.5	%
ILE	LF Integral Non-linearity	I_{REF} = 2.9mA, R_L = 300Ω			± 2	LSB
DLE	LF Differential Non-linearity	I_{REF} = 2.9mA, R_L = 300Ω			± 1	LSB

0117-04.TBL

AC ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C/70°C, V_{DDA} = V_{DDC} = V_{DDP} = 5V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DIGITAL INPUT (YCRCB[7:0], SCL, SDA, NRESET, ODDEVEN, HSYNC, DVID[8:0], EDVID, CFC)						
tsu	Input Data Set-up Time	CKREF rising edge, CKREF = 30MHz	5			ns
tho	Input Data Hold Time	CKREF rising edge, CKREF = 30MHz	5			ns
ACTIVE PERIOD FOR NRESET						
tRSTL	Input Low Time		210			ns
OSD DIGITAL INPUTS : Ri, Gi, Bi, FB (other inputs are static : TESTSCAN, TESTAUTO, CSI2C)						
tsu	Input Data Set-up Time	CKREF rising edge, CKREF = 30MHz	15			ns
tho	Input Data Hold Time	CKREF rising edge, CKREF = 30MHz	0			ns
REFERENCE CLOCK : CKREF						
tC_REF	Clock Cycle Time	CCIR601 application Square pixel/525lines Square pixel/625lines		37.04 40.75 33.90		ns ns ns
tD_REF	Clock Duty Cycle			50		%
tR_REF	Clock Rise Time				5	ns
tF_REF	Clock Fall Time				5	ns
I^2C CLOCK : SCL						
tC_SCL	Clock Cycle Time	Rpull_up = 4.7kΩ			2	MHz
tD_SCL	Clock Duty Cycle			50		%
tL_SCL	LOW Level Cycle	Rpull_up = 4.7kΩ	250			ns
DIGITAL OUTPUTS						
td_H6OSD	Delay Time	CKREF rising edge CKREF = 30MHz, C_L = 50pF	10		25	ns
td_FSYNC	Delay Time	CKREF rising edge CKREF = 30MHz, C_L = 50pF	10		22	ns
td_ODDEVEN	Delay Time	CKREF rising edge CKREF = 30MHz, C_L = 50pF	10		22	ns
td_VCS_HSYNC	Delay Time	CKREF rising edge CKREF = 30MHz, C_L = 50pF	10		22	ns

0117-05.TBL

I²C REGISTERS DESCRIPTION

STV0117 IC is controlled by an I²C bus and internal REGISTERS can be read or written by an external microcontroller.

Encoder addresses are :

if CSI2C Pin = '0' then :	write 8-bit address	is	0	1	0	0	0	0	0	(40 hex)
	read 8-bit address	is	0	1	0	0	0	0	1	(41 hex)
if CSI2C Pin = '1' then :	write 8-bit address	is	0	1	0	0	0	1	0	(42 hex)
	read 8-bit address	is	0	1	0	0	0	1	1	(43 hex)

REGISTERS are organized as follows :

Reg 0	Standard selection, sync mode selection, sync polarity selection, master/slave mode
Reg 1	Sync output selection, VBI lines blanking, filter selection, sync enable in free-run, color killer, PALNsetup, closed caption/extended data encoding mode
Reg 2	Non-interlaced mode, autotest, burst control, square pixel mode, oscillator reset value selection, oscillator reset, phase reset cycle definition
Reg 3	Color frequency control, DVID controls, luma delay adjustment
Reg 4	Software reset, power-down mode for DACs, H6OSD control
Reg 5-6	Programmable delay for time base with reference to data
Reg 7-8	Synchro delay for time base with reference to synchronization mode
Reg 9-10-11	Increment for color subcarrier frequencies
Reg 12-13-14	Offset for color subcarrier phase
Reg 15-...-22	Y clut for Ri, Gi, Bi inputs encoding
Reg 23-...-30	CR clut for Ri, Gi, Bi inputs encoding
Reg 31-...-38	CB clut for Ri, Gi, Bi inputs encoding
Reg 39-40	Closed caption characters/extended data for field 1 (odd)
Reg 41-42	Closed caption characters/extended data for field 2 (even)
Reg 43	Closed caption/extended data line insertion select for field 1 (odd)
Reg 44	Closed caption/extended data line insertion select for field 2 (even)
Reg 45-...-60	Reserved
Reg 61	Chip part identification number
Reg 62	Chip revision identification number
Reg 63	Status : Hamming decoding, frame synchro flag, closed caption data access, field counter, limit of adjustment value in Registers 5-6
Reg 64	I²C read control and reserved modes

I²C REGISTERS DESCRIPTION (continued)

Register	Access	Address	MSB							LSB
control	R/W	00	std1	std0	sym2	sym1	sym0	sys1	sys0	mod
configuration1	R/W	01	syncsel	blkli	filred	syncok	coki	PALNsetup	cc2	cc1
configuration2	R/W	02	nintrl	testauto	bursten	sqpix	selrst	rstosc	valrst1	valrst0
configuration3	R/W	03	cfc1	cfc0	dvids	dvidc	del3	del2	del1	del0
configuration4	R/W	04	softrst	downcvbs	downys	downc	enh6osd	xx	xx	xx
delay_msb	R/W	05	d11	d10	d9	d8	d7	d6	d5	d4
delay_lsb	R/W	06	d3	d2	d1	d0	xx	xx	xx	xx
sync_delay_msb	R/W	07	d11	d10	d9	d8	d7	d6	d5	d4
sync_delay_lsb	R/W	08	d3	d2	d1	d0	xx	xx	xx	xx
increment Fsc	R/W	09	xx	xx	d21	d20	d19	d18	d17	d16
increment Fsc	R/W	10	d15	d14	d13	d12	d11	d10	d9	d8
increment Fsc	R/W	11	d7	d6	d5	d4	d3	d2	d1	d0
phase Fsc	R/W	12	xx	xx	o21	o20	o19	o18	o17	o16
phase Fsc	R/W	13	o15	o14	o13	o12	o11	o10	o9	o8
phase Fsc	R/W	14	o7	o6	o5	o4	o3	o2	o1	o0
palety	R/W	15	y75	y74	y73	y72	y71	y70	xx	xx
palety	R/W	16	y65	y64	y63	y62	y61	y60	xx	xx
palety	R/W	17	y55	y54	y53	y52	y51	y50	xx	xx
palety	R/W	18	y45	y44	y43	y42	y41	y40	xx	xx
palety	R/W	19	y35	y34	y33	y32	y31	y30	xx	xx
palety	R/W	20	y25	y24	y23	y22	y21	y20	xx	xx
palety	R/W	21	y15	y14	y13	y12	y11	y10	xx	xx
palety	R/W	22	y05	y04	y03	y02	y01	y00	xx	xx
paletcr	R/W	23	cr75	cr74	cr73	cr72	cr71	cr70	xx	xx
paletcr	R/W	24	cr65	cr64	cr63	cr62	cr61	cr60	xx	xx
paletcr	R/W	25	cr55	cr54	cr53	cr52	cr51	cr50	xx	xx
paletcr	R/W	26	cr45	cr44	cr43	cr42	cr41	cr40	xx	xx
paletcr	R/W	27	cr35	cr34	cr33	cr32	cr31	cr30	xx	xx
paletcr	R/W	28	cr25	cr24	cr23	cr22	cr21	cr20	xx	xx
paletcr	R/W	29	cr15	cr14	cr13	cr12	cr11	cr10	xx	xx
paletcr	R/W	30	cr05	cr04	cr03	cr02	cr01	cr00	xx	xx
paletcb	R/W	31	cb75	cb74	cb73	cb72	cb71	cb70	xx	xx
paletcb	R/W	32	cb65	cb64	cb63	cb62	cb61	cb60	xx	xx
paletcb	R/W	33	cb55	cb54	cb53	cb52	cb51	cb50	xx	xx
paletcb	R/W	34	cb45	cb44	cb43	cb42	cb41	cb40	xx	xx
paletcb	R/W	35	cb35	cb34	cb33	cb32	cb31	cb30	xx	xx
paletcb	R/W	36	cb25	cb24	cb23	cb22	cb21	cb20	xx	xx
paletcb	R/W	37	cb15	cb14	cb13	cb12	cb11	cb10	xx	xx
paletcb	R/W	38	cb05	cb04	cb03	cb02	cb01	cb00	xx	xx
c. c. char F1	R/W	39	opc11	c117	c116	c115	c114	c113	c112	c111
c. c. char F1	R/W	40	opc12	c127	c126	c125	c124	c123	c122	c121
c. c. char F2	R/W	41	opc21	c217	c216	c215	c214	c213	c212	c211
c. c. char F2	R/W	42	opc22	c227	c226	c225	c224	c223	c222	c221
c. c. line F1	R/W	43	xx	xx	xx	l14	l13	l12	l11	l10
c. c. line F2	R/W	44	xx	xx	xx	l24	l23	l22	l21	l20
reserved reg	...	45	reserved							
...	...	...	...							
reserved reg	...	60	reserved							
chipID	R	61	0	1	1	1	0	1	0	1
revID	R	62	x	x	x	x	x	x	x	x
status	R	63	hok	atfr	b2_free	b1_free	fldct2	fldct1	fldct0	over_delay
test	R/W	64	t7	t6	t5	t4	t3	t2	t1	t0
reserved reg	...	...								

I²C REGISTERS DESCRIPTION (continued)

I²C Format

WRITE MODE (all Registers except STATUS, chipID, revID) :

In case of CSI2C Pin = '0' :

S	Slave address	W	A	Sub-address	A	Data 0	A	...	Data N	A	P

S Start condition
Slave address 0100000
W = '0' Write flag
A Acknowledge, generated by slave (STV0117) when OK A = '0' else '1'
Sub-address Sub-address Register (content is made of one byte)
Data 0 First data byte
Data N Continued data bytes (address is automaticaly incremented) and A's
P Stop condition

READ MODE (STATUS, chipID and revID Registers) :

In case of CSI2C Pin = '0' :

S	Slave address	W	AC	Sub-address N	AC	P

then :

S	Slave address	R	AC	Data N	AM	Data N + 1	...	AM	P

S Start condition
Slave address 7-bit address for STV0117 : 0100000
W = '0' Write flag
AC Acknowledge, generated by slave (STV0117) when OK A = '0', else '1'
R = '1' Read flag
Sub-address N 8-bit register sub-address
Data N Data byte of Register N, sent by STV0117
Data N +1 Data byte of Register N+1 (address automaticaly incremented)
AM Acknowledge, generated by the microcontroller AM = '0' when Acknowledge is OK, else '1'
P Stop condition (when last AM = '1')

Remarks

In case of CSI2C Pin = '0' :

Writing of a Register : Registers 0, 1, ..., 44 dec can be loaded sequentially with only one start/stop condition followed by the sub-address of the first Register desired.
Example : loading of the 4 configuration Registers : start followed by address 40 hexa and sub-address 1 and then 4 bytes of data and stop.

As specified, the I²C registers can be loaded sequentially in one run in most cases. However, when this would involve performing a soft reset by writing a "1" into the "softrst" bit of register 4, it is necessary to stop after register 4 and start a new I²C transfer sequence to send the next registers.

Reading of a REGISTER :

Example : reading of Register 63 dec (STATUS) : start followed by address 40 hexa, AC = '0' then sub-address 63 dec, AC= 0' and stop. Then start, address 41 hexa, AC = '0', and then data of Register 63 dec, AM = '1' and stop condition.

REGISTERS MAPPING AND DESCRIPTION

(*) Default Mode when NRESET Pin is active (LOW level)

Register 0 : Control (read/write)

MSB LSB

std1	std0	sym2	sym1	sym0	sys1	sys0	mod

	std1	std0	Standard Selection (see Note 1)
	0	0	PAL BDGHI
	0	1	PAL N (Argentina or Paraguay/Uruguay - see setup bit in Register1)
(*)	1	0	NTSC M
	1	1	PAL M

	sym2	Synchronization Source in Slave Mode
	0	Synchro source defined by sym0, VCS/HSYNC is output only
(*)	1	Line-based synchronization, STV0117 locks on HINPUT + ODDEVEN inputs

	sym1	Must contains same value as sym2
	0	
(*)	1	

	sym0	Frame Synchronization Input Source in Slave Mode (see Note 2)
(*)	0	ODDEVEN is the synchro input, VCS/HSYNC is an output
	1	YCRCB[7:0] input (extraction of F from EAV) : ODDEVEN and VCS/HSYNC are output signals

	sys1	Synchro : polarity of outputs : VCS/HSYNC (when sym2 = '0'), FSYNC
(*)	0	Positive (leading edge is the rising edge)
	1	Negative (leading edge is the falling edge)

	sys0	Synchro polarity selection 0 : defines the polarity of ODDEVEN in all cases, and of HSYNC when HSYNC is an input (i.e. sym2 = 1 and mod = 0)
	0	ODDEVEN falling edge flags start of field 1 (odd field) and (if sym2 = 1 and mod = 0) HSYNC falling edge is line synchro input active edge
(*)	1	ODDEVEN rising edge flags start of field 1 (odd field) and (if sym2 = 1 and mod = 0) HSYNC rising edge is line synchro input active edge

	mod	
(*)	0	slave
	1	master (freerun forced) (see Note 3)

Notes : 1. Standard on hardware reset is NTSC ; any standard modification must be followed by a software reset in order to select the right parameters for color subcarrier frequency.
2. sym0 is not taken into account when sym2 = '1', or when master mode is active (mod = '0' or testauto = '1').
3. Master mode is forced when TESTAUTO Pin is HIGH or when bit testauto of REGISTER2 is set to '1'.

REGISTERS MAPPING AND DESCRIPTION (continued)

(*) Default Mode when NRESET Pin is active (LOW level)

Register 1 : Configuration 1 (read/write)

MSB							LSB
syncsel	blkli	filred	syncok	coki	PALNsetup	cc2	cc1

syncsel — Signal Selection for VCS/HSYNC Output :
Useful in master mode, or in slave mode with sym2 = '0'
0 — Composite sync : VCS/HSYNC = VCS
(*) 1 — Horizontal sync : VCS/HSYNC = HSYNC

blkli — Blanking Lines Selection for Active Video Lines Area (see **Note 1**)
(*) 0 — Only following lines inside Vertical Interval are blanked
- in 525/60 system : lines 1-9 and lines 263 (half)-272 (SMPTE line number convention)
- in 625/50 system : lines 623 (half)-5 and lines 311-318 (CCIR line number convention)

1 — All lines inside VBI are blanked
- in 525/60 system : lines 1-19 and lines 263 (half)-282 (SMPTE line number convention)
- in 625/50 system : lines 623(half)-22 and lines 311-335 (CCIR line number convention)

filred — Chroma Pass Band Filter Select (see **Note 2**)
1 — 1.3MHz (for U/V in PAL), in NTSC : 1.3MHz for I and 0.5MHz for Q
(*) 0 — 1.8MHz (extended bandwidth for U/V in PAL, or Q/I in NTSC)

syncok — Synchros availability in case of input synchronization loss with no free-run active (if sym1 = 0)
(*) 0 — No synchro output signals
1 — Output synchros available on VCS/HSYNC, ODDEVEN, YS, CVBS : i.e same behaviour as free-run except that video output is still blanked (luminance and chrominance are at black level)

coki — Color Killer
(*) 0 — Color ON
1 — Color suppressed on CVBS output signal (CVBS = YS) but color still exists on C output

PALNsetup — Pedestal to make difference between 2 PAL-N when std[1:0] = 01
0 — Blanking level and black level are identical on all lines.
This is only valid for PAL-N (Argentina).
(*) 1 — Black level is 7.5 IRE above blanking level on all un-blanked lines.
This is only valid for PAL-N (Paraguay and Uruguay). In PAL-N (Paraguay and Uruguay), black level is 28 LSB above blanking level for lines 23-310 and 336-623 only (CCIR line number convention).

In all cases, gain factor is fixed to obtain chrominance required levels. For other standards, this bit is ignored and setup is automatically performed for PAL-M and NTSC-M

	cc2	cc1	Closed caption/extended data encoding mode
(*)	0	0	Closed caption/extended data encoding disabled
	0	1	Closed caption/extended data encoding enabled in field 1 (odd)
	1	0	Closed caption/extended data encoding enabled in field 2 (even)
	1	1	Closed caption/extended data encoding enabled in both fields

Notes : 1. blkli must be set to '0' when closed captions are to be encoded :
- in 525/60 system : before line 20 (SMPTE) or before line 283 (SMPTE)
- in 625/50 system : before line 23 (CCIR) or before line 336 (CCIR)
(reduced blanking allows preservation of analogue Wide Screen Signalling (line 23), Video Programing Service (line 16), etc)

2. Three filters for encoding : with CKREF = 27MHz (Chroma BW becomes 1.7MHz/1.2MHz, 0.45MHz with sin(x)/x DAC).
When synchro is lost (frame synchro flag (=atfr bit) is low), filred is forced to '0'.

REGISTERS MAPPING AND DESCRIPTION (continued)

(*) Default Mode when NRESET Pin is active (LOW level)

Register 2 : Configuration 2 (read/write)

MSB LSB

nintrl	testauto	bursten	sqpix	selrst	rstosc	valrst1	valrst0

nintrl — Non-interlaced Mode Select (see Note 1)
(*) 0 — Interlaced mode (625/50 or 525/60 system)
1 — Non-interlaced mode

testauto — Color Bar Pattern Software Control
(*) 0 — Color bar pattern is OFF if hardware testauto (Pin 39) is low.
1 — Color bar pattern is enabled (100% luma, 75% chroma), whatever the value on Pin TESTAUTO.

bursten — Chrominance Burst Control
0 — Burst is turned OFF, chrominance output is not affected by this bit
(*) 1 — Burst is enabled

sqpix — Square Pixel Mode Select (see Note 2)
(*) 0 — CCIR 601 pixel rate (13.5MHz) (pixel with 4:3 aspect ratio)
1 — Square pixel rate (pixel with 1:1 aspect ratio , pixel clock frequency is defined according to PAL or NTSC)

selrst — Selects Set of Reset Values for Direct Digital Frequency Synthesizer (see Note 5)
(*) 0 — Hardware reset values for phase and increment of subcarrier oscillator
1 — I^2C loaded reset values selected (see contents of Registers 9 up to 14)

rstosc — Software Phase Reset of DDFS (Direct Digital Frequency Synthesizer) (see Note 3)
0 to 1 — Transition generates a pulse reset for oscillator phase (only)
(*) 0

	valrst1	valrst0	Selects the Phase Reset Cycle of DDFS (see Note 4)
(*)	0	0	No reset on the phase of the oscillator
	0	1	Reset of the oscillator with phase_value every 2 fields
	1	0	Reset of the oscillator with phase_value every 4 fields
	1	1	Reset of the oscillator with phase_value every 8 fields

Notes : 1. In non-interlaced mode, it is a 624/2 = 312 line mode or a 524/2 = 262 line mode with waveforms same as the first field of CCIR or SMPTE. nintrl update is synchronized to beginning of next frame.
To use the circuit in non-interlaced mode in conjunction with one of the 625-line PAL standards, the circuit should first be initialised in PAL interlaced mode, and then switched to non-interlaced mode.

2. sqpix update is synchronized to beginning of next frame.
3. rstosc is automatically disabled (rstosc forced to '0') after generation of phase reset pulse; rstosc is active during 1 CKREF period.
4. Phase_value is the DEFAULT phase or that one loaded in REGISTERS 12,13 and 14.
5. In square pixel format, it is not possible to modify by I^2C loading the D.D.F.S. increment used for color subcarrier frequency generator.

REGISTERS MAPPING AND DESCRIPTION (continued)

(*) Default Mode when NRESET Pin is active (LOW level)

Register 3 : Configuration 3 (read/write)

MSB LSB

cfc1	cfc0	dvids	dvidc	del3	del2	del1	del0

	cfc1	cfc0	Color Frequency Control via CFC Line
(*)	0	0	Disable (update is done by loading of Registers 9, 10 and 11)
	0	1	Update of increment for DDFS just after serial loading via CFC
	1	0	Update of increment for DDFS on next active edge of HSYNC
	1	1	Update of increment for DDFS just before next color burst

	dvids	Digitized Video Data Control Select
(*)	0	Software control (see bit dvidc)
	1	Hardware control (Pin EDVID, same role as bit dvidc)

	dvidc	Digitized Video Data Multiplexer controlled by software : dvidc is taken into account when dvids = '0'
(*)	0	DVID[8:0] ignored
	1	DVID[8:0] selected

	del(3:0)	Delay on Luma Path with Reference to Chroma Path
	0 1 0 0	+ 4 pixel clock period delay on luma
	0 0 1 1	+ 3 pixel clock period delay on luma
	0 0 1 0	+ 2 pixel clock period delay on luma
	0 0 0 1	+ 1 pixel clock period delay on luma
(*)	0 0 0 0	+ 0 pixel clock period delay on luma
	1 1 1 1	- 1 pixel clock period delay on luma
	1 1 1 0	- 2 pixel clock period delay on luma
	1 1 0 1	- 3 pixel clock period delay on luma
	1 1 0 0	- 4 pixel clock period delay on luma
	others	+ 0 pixel clock period delay on luma

In CCIR601 mode, one pixel clock period is 1/13.5MHz (74.04ns)

In square pixel 525 lines mode, a pixel clock period is 1/12.27MHz (81.5ns)
In square pixel 625 lines mode, a pixel clock period is 1/14.75MHz (67.8ns)

REGISTERS MAPPING AND DESCRIPTION (continued)

(*) Default Mode when NRESET Pin is active (LOW level)

Register 4 : Configuration 4 (read/write)

MSB LSB

softrst	downcvbs	downys	downc	enh6osd	xx	xx	xx

softrst — Software Reset
(*) 0 — No reset
1 — Software reset

downcvbs — Down Mode on 9-bit DAC CVBS
(*) 0 — CVBS DAC in normal operation
1 — CVBS DAC input forced to 000000000 to reduce consumption and have lowest analog output

downys — Down Mode on 9-bit DAC YS
(*) 0 — YS DAC in normal operation
1 — YS DAC input forced to 000000000 to reduce consumption and have lowest analog output

downc — Down Mode on 9-bit DAC C
(*) 0 — C DAC in normal operation
1 — C DAC input forced to 000000000 to reduce consumption and have lowest analog output

enh6osd — H6OSD Output Enable Control
(*) 0 — H6OSD is not generated (H6OSD = '0')
1 — H6OSD is generated (phase is defined by reset operation) clock period is equal to CKREF/4 clock period

Note : softrst bit is automatically reset at I^2C stop condition, software reset is active during 4 CKREF periods when softrst is activated, all the device is reset as with hardware reset except for the first five I^2C REGISTERS (control and configurations).

REGISTERS MAPPING AND DESCRIPTION (continued)

(*) Default Mode when NRESET Pin is active (LOW level)

Register 5 : Delay_msb (read/write)
Register 6 : Delay_lsb (read/write)

	MSB							LSB
Register 5	d11	d10	d9	d8	d7	d6	d5	d4
Register 6	d3	d2	d1	d0	xx	xx	xx	xx

Note : When adjustment is needed (DEFAULT values do not fit the application), these delay Registers can be loaded anytime (remember however that a software reset forces the default values).

In MASTER mode (mod = 1 or autotest modes) (see Figure 13)

Position of ODDEVEN as output signal is adjusted with reference to analog horizontal sync according to the 2's complement value loaded in these Registers :
The value must be within range : [-1536,+1536].
If it is not the case, the value taken into account is the maximum allowed depending on d11 for sign.

ODDEVEN transition occurs on sample number :
(max line length + 1 + delay(11:0) + 2) modulo [max line length].
Thus, by changing "delay", it is possible to shift the location of ODDEVEN with reference to the analogue video outputs (or equivalently, to the YCRCB input data samples).

d[11:0] is a 2's complement value
d[11] : when '0' ODDEVEN lags with reference to main sample counter of N (=d[10:0]) samples. ODDEVEN is closer to analog horizontal sync output signal.
d[11] : when '1' ODDEVEN leads with reference to main sample counter of N (=not d[10:0] + 1) samples. ODDEVEN is further away from analog horizontal sync output signal.

Default value is d[11:4] = 00 hexa, d[3:0], xxxx = 00 hexa, so that ODDEVEN signal toggles when main sample 11-bit-counter value is 003 hexa.

In SLAVE mode (mod = 0)

If sym2 = 0 (VCS/HSYNC is not an input) :
Main sample counter is loaded with value d[10:0] when either ODDEVEN (as input signal), or F signal (extracted from EAV on YCRCB[7:0] input) changes with the programmed transition for the frame beginning.

Main sample counter is loaded with the value:(max line length + 1 + delay(11:0)) modulo [max line length], 2 CKREF clock periods after frame synchro input (F or ODDEVEN).

Thus position of analog synchronization output signal can be adjusted with reference to YCRCB[7:0] input data.

Position of ODDEVEN (as output signal, only when in slave by F from YCRCB) is also defined with d[11:0] as in master mode (see Figure 14).
d[11:0] is a 2's complement value
d[11] : when '0', analog synchronization output signal leads with reference to YCRCB[7:0] input data of N (= d[10:0]) samples.
d[11] : when '1', analog synchronization output signal lags with reference to YCRCB[7:0] input data of N (= not d[10:0] + 1) samples.

(*) Hardware Reset Values :
when sym0 = 0 (synchro by ODDEVEN), DEFAULT value of delay REGISTERS is 0000h
when sym0 = 1 (synchro by F from EAV in YCRCB[7:0]), DEFAULT value of delay REGISTERS is :
in 525/60 systems :FE60 hexa (1st byte:254 2nd byte:96)
in 625/50 systems :FEE0 hexa (1st byte:254 2nd byte:224)
With these DEFAULT values, ODDEVEN output signal is the image of timing reference frame transmitted on YCRCB[7:0] input data (EAV decoding))

If sym2 = 1 (VCS/HSYNC = HSYNC is a synchro input with ODDEVEN) :
The allowed values for delay REGISTERS are within range : [-44..-1,0,..+43].
If it is not the case, the value taken into account is the maximum allowed depending on d11 for sign.

REGISTERS MAPPING AND DESCRIPTION (continued)

(*) Default Mode when NRESET Pin is active (LOW level)

Register 7 : Synchro_delay_msb (read/write)
Register 8 : Synchro_delay_lsb (read/write)

	MSB							LSB
Register 7	d11	d10	d9	d8	d7	d6	d5	d4
Register 8	d3	d2	d1	d0	xx	xx	xx	xx

If sym2 = 0 (VCS/HSYNC is a synchro output) :

The synchro_delay register is used to adjust the position of the VCS/HSYNC and FSYNC output signals with reference to the analog video outputs.

VCS/HSYNC and FSYNC are decoded from a fixed reference value of an auxillary sample counter. It is possible to change the relation between this auxillary counter and the main sample counter, thus causing the VCS/HSYNC and FSYNC locations to be shifted. The synchro_delay register codes the shift required in terms of clock periods with reference to the default position. Figures 14 and 15 illustrate this default position.

d[11:0] is the 2's complement value that codes the desired shift, i.e :
d[11] : when '0', VCS/HSYNC and FSYNC output signals lead with reference to default location by N (= d[10:0]) samples.
d[11] : when '1', VCS/HSYNC and FSYNC output signals lag with reference to default location by N (= not d[10:0] + 1) samples.

If sym2 = 1 (VCS/HSYNC = HSYNC is a synchro input) :

The synchro_delay register has no effect. In that particular case, the FSYNC output is synchronous with the analog synchronization present in the output analog video signals (Y and CVBS).

The default value of the synchro delay register is 0000 hex, but they should be set to FCE0 hex for direct compatibility with an SGS-THOMSON MPEG application.

Caution : changing the synchro delay **from its default value** (0000 hex) to a new value must be done whilst the chip is **not** in master mode and is **out of sync**.

REGISTERS MAPPING AND DESCRIPTION (continued)

(*) Default Mode when NRESET Pin is active (LOW level)

Registers 9-10-11 : Increment for Direct Digital Frequency Synthesizer (read/write)

	MSB							LSB
Register 9	xx	xx	d21	d20	d19	d18	d17	d16
Register 10	d15	d14	d13	d12	d11	d10	d9	d8
Register 11	d7	d6	d5	d4	d3	d2	d1	d0

22-bit increment of sinus ROM address : 1 LSB ~ 6.44Hz in CCIR
~ 7.03Hz in square pixel-625
~ 5.85Hz in square pixel-525

Hardware reset values with reference to standard selected : these values are those selected when selrst bit equals '0', (in that case, content of Registers 9-10-11 is not taken into account).
Moreover, Registers 9-10-11 are never reset and must be explicitly written into to contain sensible information.

	Rectangular Pixel Mode :			Synthesized Subcarrier Frequency	Ref. Clock
(*)	d(21:0) : 087C1F	hexa, 556063	dec for NTSC M	f = 3.5795452MHz	27MHz
	d(21:0) : 0A8263	hexa, 688739	dec for PAL BGHIN	f = 4.43361875MHz	27MHz
	d(21:0) : 087DA5	hexa, 556453	dec for PAL N	f = 3.5820558MHz	27MHz
	d(21:0) : 0879BC	hexa, 555452	dec for PAL M	f = 3.57561149MHz	27MHz
	Square Pixel Mode :			Synthesized Subcarrier Frequency	Ref. Clock
	d(22:0) : 095555	hexa, 611669	dec for NTSC M	f = 3.579545MHz	24.5454MHz
	d(22:0) : 099E63	hexa, 630371	dec for PAL BGHIN	f = 4.43361875MHz	29.50MHz
	d(22:0) : 07C570	hexa, 509296	dec for PAL N	f = 3.582056MHz	29.50MHz
	d(22:0) : 0952B5	hexa, 610997	dec for PAL M	f = 3.575610MHz	24.5454MHz

These hard-wired values being out of any user register, they cannot be read out from the STV0117.

Note : The value loaded in these registers are taken into account after a software reset with selrst equals '1' (see register 2, bit selrst) (refer to Figure 12).

Registers 12-13-14 : Static Phase Offset for Direct Digital Frequency Synthesizer (read/write)

	MSB							LSB
Register 12	xx	xx	o21	o20	o19	o18	o17	o16
Register 13	o15	o14	o13	o12	o11	o10	o9	o8
Register 14	o7	o6	o5	o4	o3	o2	o1	o0

Hardware reset values with reference to standard selected : these values are those selected when selrst bit equals '0', (in that case, content of Registers 12-13-14 is not taken into account).
Moreover, Registers 12-13-14 are never reset and must be explicitly written into to contain sensible information.

Hard-wired values being out of register ; they cannot be read out from the STV0117. The hard-wired values fro phase offset are the following :

Rectangular Pixel Format :

(*) o(21:0) : 1E2DE8 hexa for NTSC M
o(21:0) : 000F40 hexa for PAL BGHIN, M

Square Pixel Format :

o(21:0) : 000000 hexa for all standards

The recommended values are : 05BFA0 for BGI-N-MPAL and 17F4FF for M-NTSC.

Note : The value loaded in these registers are taken into account after an oscillator reset (bit rstosc of Register 2) with selrst equals '1' (see Register 2, bit selrst).

REGISTERS MAPPING AND DESCRIPTION (continued)

(*) Default Mode when NRESET Pin is active (LOW level)

Registers 15-16-17-18-19-20-21-22 : Palety (read/write)

	MSB							LSB
Register 15	y75	y74	y73	y72	y71	y70	xx	xx
Register 16	y65	y64	y63	y62	y61	y60	xx	xx
Register 17	y55	y54	y53	y52	y51	y50	xx	xx
Register 18	y45	y44	y43	y42	y41	y40	xx	xx
Register 19	y35	y34	y33	y32	y31	y30	xx	xx
Register 20	y25	y24	y23	y22	y21	y20	xx	xx
Register 21	y15	y14	y13	y12	y11	y10	xx	xx
Register 22	y05	y04	y03	y02	y01	y00	xx	xx

8 x 6-bit words for Y component

(*) DEFAULT value	Y(hexa)	Y(dec)	Color (100% white to black)	Ri, Gi, Bi (OSD index inputs)
Register15	y7x=EC	236	white	111
Register16	y6x=A0	160	yellow	110
Register17	y5x=50	80	magenta	101
Register18	y4x=40	64	red	100
Register19	y3x=84	132	cyan	011
Register20	y2x=74	116	green	010
Register21	y1x=24	36	blue	001
Register22	y0x=10	16	black	000

DEFAULT color bar pattern display is from left to right :
white, yellow, cyan, green, magenta, red, blue, black

Registers 23-24-25-26-27-28-29-30 : Paletcr (read/write)

	MSB							LSB
Register 23	cr75	cr74	cr73	cr72	cr71	cr70	xx	xx
Register 24	cr65	cr64	cr63	cr62	cr61	cr60	xx	xx
Register 25	cr55	cr54	cr53	cr52	cr51	cr50	xx	xx
Register 26	cr45	cr44	cr43	cr42	cr41	cr40	xx	xx
Register 27	cr35	cr34	cr33	cr32	cr31	cr30	xx	xx
Register 28	cr25	cr24	cr23	cr22	cr21	cr20	xx	xx
Register 29	cr15	cr14	cr13	cr12	cr11	cr10	xx	xx
Register 30	cr05	cr04	cr03	cr02	cr01	cr00	xx	xx

8 x 6-bit words for CR component

(*) DEFAULT value	CR(hexa)	CR(dec)	Color (75% R, G, B)	Ri, Gi, Bi (OSD index inputs)
Register23	cr7x=80	128	white	111
Register24	cr6x=8C	140	yellow	110
Register25	cr5x=C4	196	magenta	101
Register26	cr4x=D4	212	red	100
Register27	cr3x=2C	44	cyan	011
Register28	cr2x=38	56	green	010
Register29	cr1x=70	112	blue	001
Register30	cr0x=80	128	black	000

REGISTERS MAPPING AND DESCRIPTION (continued)

(*) Default Mode when NRESET Pin is active (LOW level)

Registers 31-32-33-34-35-36-37-38 : Paletcb (read/write)

	MSB							LSB
Register 31	cb75	cb74	cb73	cb72	cb71	cb70	xx	xx
Register 32	cb65	cb64	cb63	cb62	cb61	cb60	xx	xx
Register 33	cb55	cb54	cb53	cb52	cb51	cb50	xx	xx
Register 34	cb45	cb44	cb43	cb42	cb41	cb40	xx	xx
Register 35	cb35	cb34	cb33	cb32	cb31	cb30	xx	xx
Register 36	cb25	cb24	cb23	cb22	cb21	cb20	xx	xx
Register 37	cb15	cb14	cb13	cb12	cb11	cb10	xx	xx
Register 38	cb05	cb04	cb03	cb02	cb01	cb00	xx	xx

8 x 6-bit words for CB component

(*) DEFAULT value	CB(hexa)	CB(dec)	Color (75% R, G, B)	Ri, Gi, Bi (OSD index inputs)
Register31	cb7x=80	128	white	111
Register32	cb6x=2C	44	yellow	110
Register33	cb5x=B8	184	magenta	101
Register34	cb4x=64	100	red	100
Register35	cb3x=9C	156	cyan	011
Register36	cb2x=48	72	green	010
Register37	cb1x=D4	212	blue	001
Register38	cb0x=80	128	black	000

Registers 39-40 : cccf1 (read/write) : closed caption characters/extended data for field 1 (see Note)

First byte to encode :

	MSB							LSB
Register 39	opc11	c117	c116	c115	c114	c113	c112	c111

opc11 : odd-parity bit of US-ASCII 7-bit character c11(7:1)

Second byte to encode :

	MSB							LSB
Register 40	opc12	c127	c126	c125	c124	c123	c122	c121

opc12 : odd-parity bit of US-ASCII 7-bit character c12(7:1)

Default value : none, but closed captions enabling without loading these registers will issue character NULL. Registers 39-40 are never reset.

Note : There is a one bit rotation when reading the values stored in these registers. If register 39 or 40 contains the following 8 bits : b8.b7.b6.b5.b4.b3.b2.b1, the value read will be : b1.b8.b7.b6.b5.b4.b3.b2.

REGISTERS MAPPING AND DESCRIPTION (continued)

(*) Default Mode when NRESET Pin is active (LOW level)

Registers 41-42 : cccf2 (read/write) : closed caption characters/extended data for field 2 (see Note)

First byte to encode :

	MSB							LSB
Register 41	opc21	c217	c216	c215	c214	c213	c212	c211

opc21 : odd-parity bit of US-ASCII 7-bit character c21(7:1)

Second byte to encode :

	MSB							LSB
Register 42	opc22	c227	c226	c225	c224	c223	c222	c221

opc22 : odd-parity bit of US-ASCII 7-bit character c22(7:1)

Default value : none, but closed captions enabling without loading these registers will issue character NULL. Registers 41-42 are never reset.

Note : There is a one bit rotation when reading the values stored in these registers. If register 41 or 42 contains the following 8 bits : b8.b7.b6.b5.b4.b3.b2.b1, the value read will be : b1.b8.b7.b6.b5.b4.b3.b2.

Register 43 : cclif1 (read/write) : closed caption/extended data line insertion for field 1

TV field1 line number where closed caption/extended data is to be encoded is programmable through the following Register :

MSB							LSB
xx	xx	xx	l14	l13	l12	l11	l10

- 525/60 system : (525-SMPTE line number convention). Only lines 10 through 22 should be used for closed caption or extended data services (line 1 through 9 contain the vertical sync pulses with equalizing pulses).
  l1(4:0) = 00000 no line selected for closed caption encoding
  l1(4:0) = 000xx do not use these codes
  l1(4:0) = 00100 line 10 (SMPTE) selected for encoding
  ....
  l1(4:0) = 10000 line 22 (SMPTE) selected for encoding
  l1(4:0) = others from line 23 upto 37 (SMPTE)
- 625/50 system : (625-CCIR line number convention). Only lines 7 through 23 should be used for closed caption or extended data services.
  l1(4:0) = 00000 no line selected for closed caption encoding
  l1(4:0) = 00001 line 7 (CCIR) selected for encoding
  ....
  l1(4:0) = 10001 line 23 (CCIR) selected for encoding
  l1(4:0) = others from line 24 upto 37 (CCIR)

(*) DEFAULT value = 01111 line 21 (525/60, 525-SMPTE line number convention)
line 21 (625/50, 625-CCIR line number convention)

Note : See also Note 1 concerning "blkli" bit in configuration register 1.

REGISTERS MAPPING AND DESCRIPTION (continued)

(*) Default Mode when NRESET Pin is active (LOW level)

Register 44 : cclif2 (read/write) : closed caption/extended data line insertion for field 2

TV field2 line number where closed caption/extended data is to be encoded is programmable through the following Register :

MSB							LSB
xx	xx	xx	I24	I23	I22	I21	I20

- 525/60 system : (525-SMPTE line number convention). Only lines 273 through 284 should be used for closed caption or extended data services (preceding lines contain the vertical sync pulses with equalizing pulses), although it is possible to program over a wider range.
  I2(4:0) = 00000 no line selected for closed caption encoding
  I2(4:0) = 000xx do not use these codes
  I2(4:0) = 00100 line 273 (SMPTE) selected for encoding
  ....
  I2(4:0) = 01111 line 284 (SMPTE) selected for encoding
  I2(4:0) = others from line 285 upto 292 (SMPTE)
- 625/50 system : (625-CCIR line number convention). Only lines 319 through 336 should be used for closed caption or extended data services (preceding lines contain the vertical sync pulses with equalizing pulses), although it is possible to program over a wider range.
  I2(4:0) = 00000 no line selected for closed caption encoding
  I2(4:0) = 00001 line 319 (CCIR) selected for encoding
  I2(4:0) = 00010 line 320 (CCIR) selected for encoding
  ....
  I2(4:0) = 10010 line 336 (CCIR) selected for encoding
  I2(4:0) = others from line 337 upto 349 (CCIR)

(*) DEFAULT value = 01111 line 284 (525/60, 525-SMPTE line number convention)
line 333 (625/50, 625-CCIR line number convention)

Note : See also Note 1 concerning "blkli" bit in configuration register 1.

Registers 45 up to 60 : Reserved Registers

Register 61 : chipID (read only) : chip part identification number

MSB							LSB
0	1	1	1	0	1	0	1

Register 62 : revID (read only) : chip revision identification number

MSB							LSB
x	x	x	x	x	x	x	x

May be used by the manufacturer to indicate revision level of the silicon (the revID register for version 1.0 contains 0000 0001).

REGISTERS MAPPING AND DESCRIPTION (continued)

(*) Default Mode when NRESET Pin is active (LOW level)

Register 63 : Status (read only)

MSB LSB

hok	atfr	buf2_free	buf1_free	fieldct2	fieldct1	fieldct0	over_delay

hok : Hamming Decoding of odd/even Signal from YCRCB (see Note)
0 multiple errors
(*) 1 0 or 1 error

atfr : Frame Synchronization Flag
(*) 0 encoder not synchronized
1 in slave mode : encoder synchronized

buf2_free : Closed Caption Field2-Registers Access Condition.
Closed caption data is buffered before being output on the relevant TV line ; buf2_free is reset if the buffer is temporarily unavailable. If the microcontroller can guarantee that Registers 41 and 42 (cccf2) are never written more than once between two frame reference signals, then the buf2_free bit will always be true (set). Otherwise, closed caption field2 register access might be temporarily forbidden by resetting the buf2_free bit until the next field2 closed caption line occurs.
Note that this bit is false (reset) when 2 pairs of data bytes are awaiting to be encoded, and is set back immediately after one of these pairs has been encoded (so at that time, encoding of the last pair of bytes is still pending)
(*) Reset value = 1 (access authorized)

buf1_free : Closed Caption Field1-Registers Access Condition.
Same signification of buf2_free bit but for closed caption of field1.
(*) Reset value = 1 (free access)

fieldct[2:0] : Digital Field Identification Number
000 indicates field 1
...
(*) 111 indicates field 8
fieldct[0] is the odd/even information ('0' for odd field, '1' for even field)

over_delay : Limit of Registers 5-6 Adjustment Value
(*) 0 no overflow with loaded value in Registers 5-6
1 value loaded in Registers 5-6 is outside allowed limits, but forced to maximum authorized

Note : Signal quality detector issued from Hamming decoding on EAV, SAV from YCRCB.

Registers 64-65-66-67 : Reserved Registers

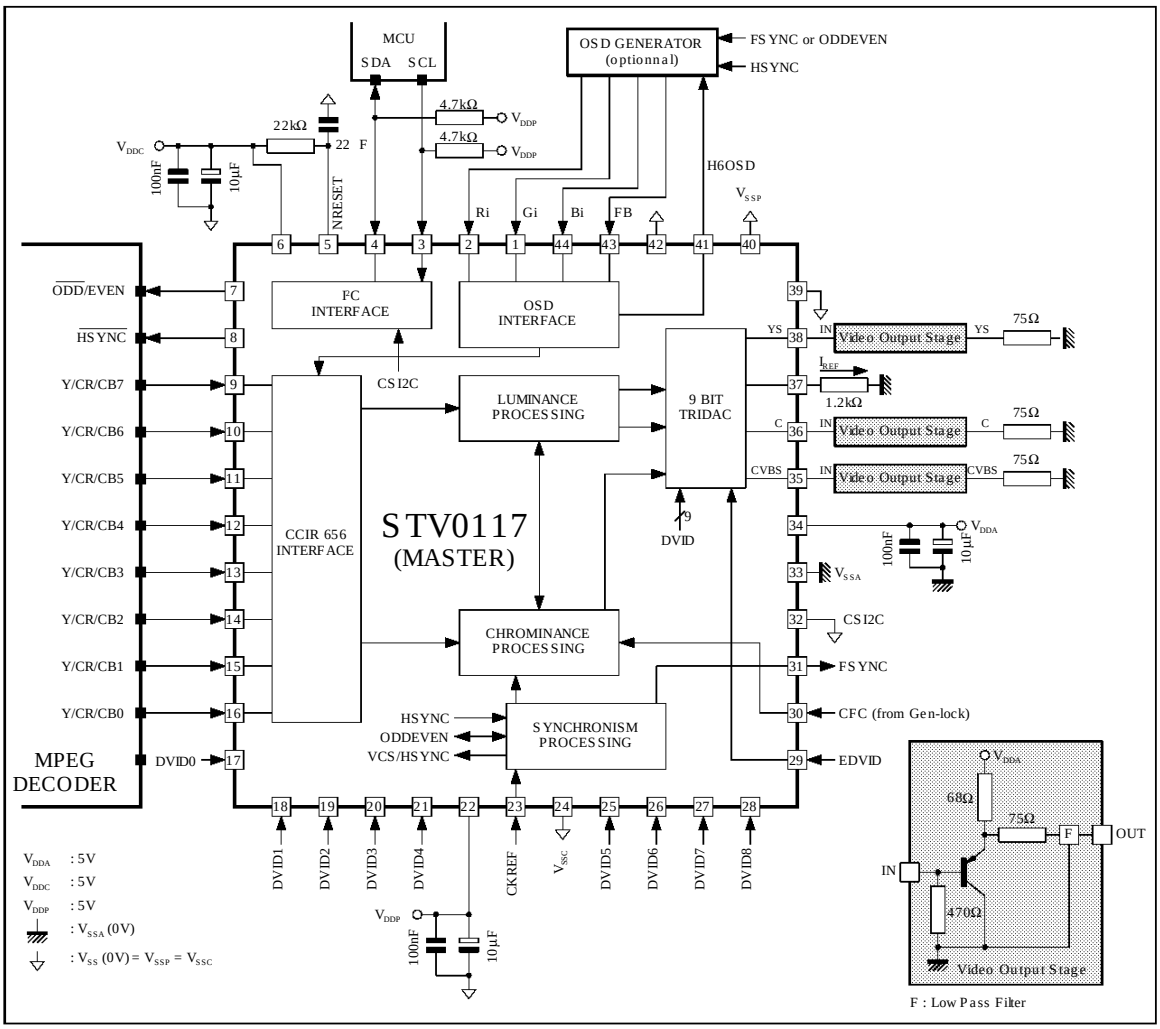
Register 64 : Test (read/write)

MSB LSB

t7	t6	t5	t4	t3	t2	t1	t0

Default value is 40 hex. I^2C registers can be accessed in read mode by writing 60 hex in this register. All other values are reserved and should not be used.

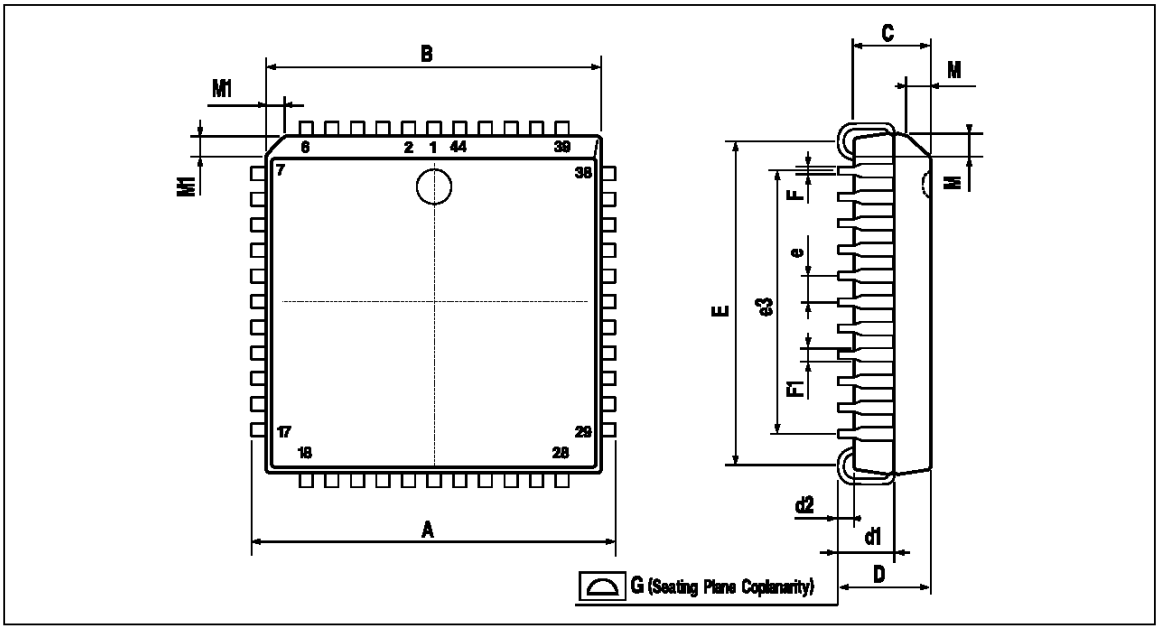
TYPICAL APPLICATION DIAGRAM



Note : When unused, DVID (8:0), EDVID, FB, Ri, Gi, Bi inputs must be tied to ground (VSSP) ; and CFC input must be tied to VDDp.

PACKAGE MECHANICAL DATA

44 PINS - PLASTIC CHIP CARRIER



PMPLCC44.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	

PLCC44.TBL