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SSI 32R2103R/04R/05R
8/10 Channel Thin Film Read/Write Devices

June 1996

DESCRIPTION

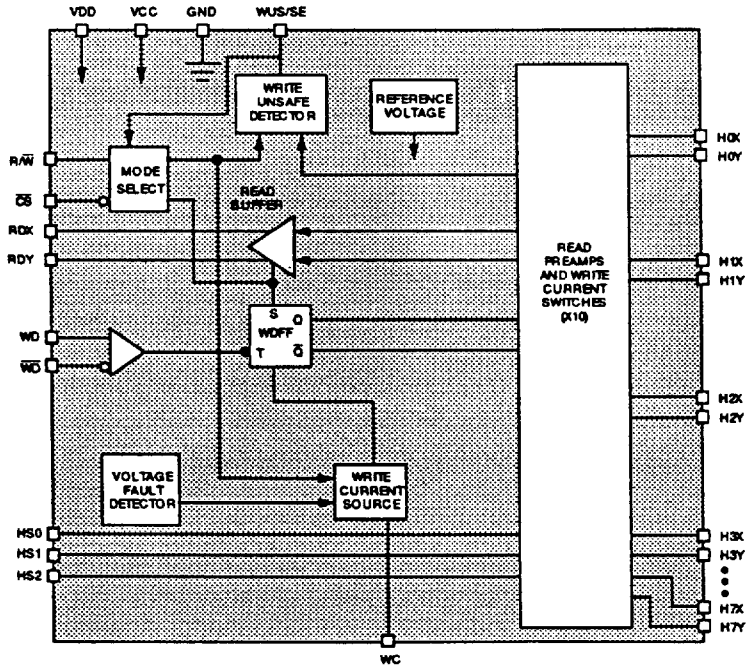
The SSI 32R2103R/04R/05R are BiCMOS monolithic integrated circuits designed for use with two-terminal recording heads. They provide a low noise read amplifier, a high performance write driver, write current control, and data protection circuitry for up to 10 channels. The SSI 32R2103R/04R/05R option provides internal 250 Ω damping resistors. Damping resistors are switched in during write mode and switched out during read mode. The SSI 32R2103/04/05 option does not provide damping resistors. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by making the read channel outputs high impedance. The device also offers multiple channel "servo bank write" capability to assist in servo writing operations.

The SSI 32R2103R/04R/05R requires 5 V and 12 V power supplies. The SSI 32R2103R/2105R provides PECL write data input with flip-flop. The SSI 32R2104R provides PECL direct write data input without flip-flop.

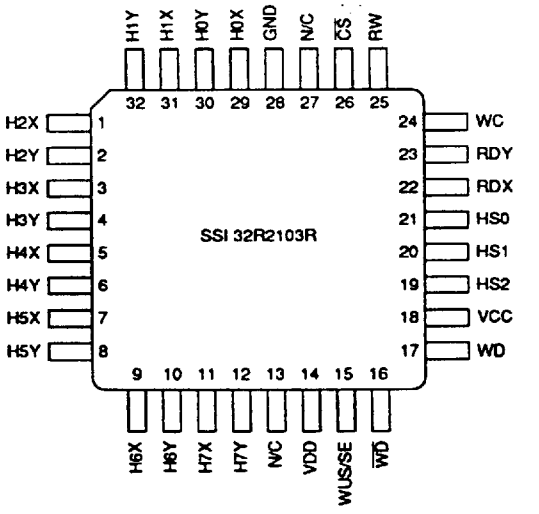
FEATURES

- **5 V ±10%, 12 V ±10% supply**
- **Low power**
  - **PD = 235 mW read mode (nominal)**
  - **PD = 12 mW idle mode (maximum)**
- **High Performance:**
  - **Read mode gain = 250 V/V**
  - **Input noise = 0.45 nV/√Hz (nominal)**
  - **Input capacitance = 10 pF (nominal)**
  - **Write current range = 10-35 mA**
  - **Maximum write current rise/fall time = 7 ns (typical head)**
  - **Head voltage swing = 11 Vp-p minimum**
- **Servo bank write capability**
- **Self-switching damping resistance**
- **Write unsafe detection**
- **Power supply fault protection**
- **Head short to ground protection**
- **With write data flip-flop (SSI 32R2103R/2105R) or without write data flip-flop (SSI 32R2104R)**

SSI 32R2103R BLOCK DIAGRAM



PIN DIAGRAM



32-Lead, PECL Write Data Input 8-Channel TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32R2103R/04R/05R have the ability to address up to 10 two-terminal heads and provide write drive or read amplification. Mode control and head selection are described in Tables 1, 2 and 3. The TTL inputs R/$\overline{W}$, and $\overline{CS}$ have internal pull-up circuitry to prevent an accidental write condition. HS0, HS1, HS2 and HS3 have internal pull-down circuitry. Internal current limit circuitry will protect the IC from a head short to ground condition in any write mode.

TABLE 1: Head Select*

HEAD SELECTED	32R2103R/04R/05R - 10				32R2103R/04R/05R - 8		
	HS3	HS2	HS1	HS0	HS2	HS1	HS0
0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	1
2	0	0	1	0	0	1	0
3	0	0	1	1	0	1	1
4	0	1	0	0	1	0	0
5	0	1	0	1	1	0	1
6	0	1	1	0	1	1	0
7	0	1	1	1	1	1	1
8	1	0	0	0	NA	NA	NA
9	1	0	0	1	NA	NA	NA

*Do not use invalid head select combinations.

TABLE 2: Mode Select

$\overline{CS}$	R/$\overline{W}$	WUS/SE	MODE
0	0	*	Single Channel Write (see Table 1)
0	0	**	Servo/Bank Write (see Table 3)
0	1	X	Single Channel Read (see Table 1)
1	X	X	Idle

* WUS/SE is a WUS output unless pulled above VCC.
** Servo write mode is activated through the WUS pin as described in the servo write mode section.

TABLE 3: Servo Write Mode*

HEAD SELECTED	HEAD SELECTED (SERVO BANK WRITE)	HS3	HS2	HS1	HS0
0	No Heads Selected	0	0	0	0
1	H0, H1	0	0	0	1
2	H2, H3	0	0	1	0
3	H0, H1, H2, H3	0	0	1	1
4	No Heads Selected	0	1	0	0
5	H4, H5	0	1	0	1
6	H6, H7,	0	1	1	0
7	H4, H5, H6, H7	0	1	1	1
8	No Heads Selected	1	0	0	0
9	H8, H9	1	0	0	1

*Do not use invalid head select combinations.

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the SSI 32R2103R/04R/05R as a current switch and activates the write unsafe (WUS) detector circuitry. On the SSI 32R2103R/05R, head current is toggled between the X and Y side of the selected head on each low to high transition of WD-$\overline{WD}$. Note that a preceding read to write transition or idle to write transition initializes the write data flip-flop to pass write current into the "X" side of the device. In this case, the Y side is higher potential than the X side. With the SSI 32R2104R, head current is toggled between the X and Y side of the head on each WEX–WDY transition. When the potential of WDX is higher than WDY, the potential on the X side of the head is higher than the Y side (HNY is sinking current). The magnitude of the write current (0-pk) is given by:

$$Iw = Aw \cdot \frac{Vwc}{Rwc} = K/Rwc$$

where Aw is the write current gain.

RWC is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

where:

Rh = head resistance plus external wire resistance; and

Rd = damping resistance.

In write mode a 250 Ω damping resistor is switched in across the Hx, Hy ports (SSI 32R2103R/04R/05R only). Unselected heads are at ground potential.

FUNCTIONAL DESCRIPTION (continued)

SERVO WRITE MODE

This mode allows for writing to multiple channels at once, which is useful during servo formatting.

To enable servo write mode follow these steps:

(1) Place the device in the read mode (R/W high).

(2) Set the head select lines to an address that corresponds to the bank of heads desired for servo write (see Table 3).

(3) Pull the WUS/SE output above VCC by sourcing 10 mA of current into the pin. Two ways to source this current are: (a) use a voltage source set to VCC +1.9 V limited to 10 mA current, or (b) use a resistor tied between WUS/SE and a supply above VCC to source the current. With 10 mA of current, WUS/SE will rise to approximately VCC +1.5 V.

(4) Allow at least 1 µs set-up.

(5) While maintaining steps (2) and (3) above make R/W low, placing the device in servo write mode.

POWER SUPPLY FAULT PROTECTION

A voltage fault detection circuit improves data security by disabling the write current generator during a voltage fault or power start-up regardless of mode.

HEAD SHORT TO GROUND PROTECTION

The SSI 32R2103R/04R/05R provide a head short to ground protection circuit in any mode. In idle or read mode, or for an unselected head in write mode, current out of the head port will not exceed 3 mA. If a selected head in write mode is shorted to ground, the write current generator will turn off, and remain off until the user exits write mode and then returns to write mode.

WRITE UNSAFE

Any of the following conditions will be indicated as a high level on the write unsafe (WUS) open collector output.

- WDI frequency too low
- Device in read mode
- Device not selected
- Device in servo write mode
- No head current
- Open head
- Head short to ground
- Power supply fault

To prevent false WUS flags, the head inductance and resistance should be less than 1 µH and 50 Ω, respectively.

WDI frequency too low is detected if the WDI frequency falls below 1 MHz (typ). Consult the WUS safe to unsafe timing for range of frequency detection.

Device in read mode, device in servo write mode and device not selected will flag WUS if R/$\overline{W}$ is high, if $\overline{SE}$ is low, or $\overline{CS}$ is high.

No head current will flag WUS if Rwc > 50 kΩ.

Head opened will flag WUS if Rh = ∞. To prevent false WUS flags, the open head detect is disabled when write data frequency is greater than 20 MHz.

Head short to ground is described in the preceding paragraph.

Upon entering write mode, WUS is valid within the specified R/$\overline{W}$ timing.

After the low frequency fault condition is removed, one positive transition of WD-WD (SSI 32R2103R/2105R), or one positive transition of WDX–WDY (SSI 32R2104R) is required to clear WUS.

READ MODE

The read mode configures the SSI 32R2103R/04R/05R as a low noise differential amplifier and deactivates the write current generator. The damping resistor is switched out of the circuit allowing a high impedance input to the read amplifier. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The HnX, HnY inputs are non-inverting to the RDX, RDY outputs.

Note that in idle or write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage change when switching from write to read mode. Note also that the write current source is deactivated for both the read and idle mode.

In read mode, unselected heads are at ground potential.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

In idle mode, all heads are at ground potential.

PIN DESCRIPTION

CONTROL/STATUS

NAME	TYPE	DESCRIPTION
$\overline{CS}$	I	CHIP SELECT INPUT: A logical low level enables the device.
R/$\overline{W}$†	I	READ/WRITE: A logical high level enables read mode. A logical low level enables write mode.
HS0, HS1, HS2, HS3	I	HEAD SELECT: Decoded address selects one of 8 or 10 channels (see Table 2).
WUS/SE†	O	WRITE UNSAFE/SERVO ENABLE: When in servo bank write mode, pulling this pin above VCC, enables servo bank write (see servo write mode section). Otherwise, a high level indicates an unsafe writing condition (see WUS section).
WC†	I	WRITE CURRENT: Sets the write current through the recording head.

† When more than one read/write device is used, signals can be wire OR'ed.

HEAD TERMINAL CONNECTIONS

H0X-H9X H0Y-H9Y	I	X,Y HEAD CONNECTIONS

DATA INPUT/OUTPUT

WD, $\overline{WD}$†	I	DIFFERENTIAL WRITE DATA IN: A positive transition of WD-$\overline{WD}$ changes the direction of current in the recording head. (SSI 32R2103R/2105R)
WDX, WDY	I	DIFFERENTIAL WRITE DATA IN: Each transition of WDX–WDY changes the direction of current in the recording head. (SSI 32R2104R)
RDX,RDY†	O	DIFFERENTIAL READ DATA OUT: Emitter follower output.

POWER

VCC		5 V Power Supply
VDD		12 V Power Supply
GND		Ground

ELECTRICAL SPECIFICATIONS

Current maximums are currents with the highest absolute value.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER			RATING
DC Supply Voltage		VCC	-0.3 to 6 VDC
		VDD	-0.3 to 14.0 VDC
Write Current		Iw	100 mA
Digital Input Voltage		Vin	-0.3 to VCC +0.3 V
Head Port Voltage		VH	-0.3 to VDD +0.3 V
WUS Pin Voltage		Vwus	-0.3 to VCC +2 V
Output Current	RDX,RDY	Io	-6 mA
	$\overline{\text{WUS}}$	Iwus	12 mA
Junction Operating Temperature		Tj	125° C
Storage Temperature			-65 to 150° C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage	VCC	5 ± 10% V
	VDD	12 ± 10% V
Ambient Operating Temperature	Ta	0° < Ta < 75° C
Head Inductance	Lh	Lh < 1 µH
Head Resistance, Valid WUS	Rh	Rh < 50 Ω

TEST CONDITIONS

Recommended operating conditions apply.

Write Current	Iw	20 mA
Head Inductance	Lh	1 µH
Head Resistance	Rh	30 Ω
WD Frequency		5 MHz
WD, $\overline{\text{WD}}$ Rise/Fall Time (SSI 32R2103R/2103/2105/2105R)		1 ns
WDI Rise/Fall Time (SSI 32R2104/2104R)		1 ns

POWER DISSIPATION
Recommended operating conditions apply.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VCC Supply Current	Read Mode		46	60	mA
	Write Mode		20	22	mA
VCC Supply	SBW Mode (4 Heads)		50	65	mA
	Idle Mode		0.6	1	mA
VDD Supply Current	Read Mode		0.4	0.7	mA
	Write Mode		Iw + 7	Iw + 10	mA
VDD Supply	SBW Mode (4 Heads)		28 + (4 • Iw)	40 + (4 • Iw)	mA
	Idle Mode		0.3	0.6	mA
Power Dissipation	Read Mode		235	340	mW
	Write Mode		184 mW + (Iw • VDD)	253 mW + (Iw • VDD)	mW
Total Power Dissipation	SBW Mode (4 Heads)		645 + 4 • (Iw • VDD)	886 + 4 • (Iw • VDD)	mW
	Idle Mode		6.6	13	mW

DIGITAL INPUTS

Input High Voltage HSX, $\overline{CS}$, R/$\overline{W}$	Vih		2			VDC
Input Low Voltage HSX, $\overline{CS}$, R/$\overline{W}$	Vil				0.8	VDC
Input High Current HSX, $\overline{CS}$, R/$\overline{W}$	Iih	Vih = 2 V			100	µA
Input Low Current HSX, $\overline{CS}$, R/$\overline{W}$	Iil	Vil = 0.8 V	-400			µA
(WD/$\overline{WD}$) and (WDX/WDY) Input High Voltage	Vih		2		VCC -0.2	VDC
(WD/$\overline{WD}$) and (WDX/WDY) Input Low Voltage	Vil		Vih -2		Vih -0.3	VDC
(WD/$\overline{WD}$) and (WDX/WDY) Input Voltage Difference			0.3		2	V
(WD/$\overline{WD}$) and (WDX/WDY) Input High Current		Vih = VCC -0.75 V		85	110	µA
(WD/$\overline{WD}$) and (WDX/WDY) Input Low Current		Vih = VCC -1.75 V		70	100	µA

ELECTRICAL SPECIFICATIONS (continued)

DIGITAL OUTPUTS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
WUS Output Low Voltage Vol	Iol = 2 mA maximum			0.5	VDC
WUS Output High Current Ioh	Voh = VCC	-100	0	100	µA

WRITE CHARACTERISTICS

Test conditions apply unless otherwise specified.

Write Current Range		10		35	mA
Write Current Voltage Vwc			2		V
Write Current Gain Awc	Iw = Aw • Vwc/Rwc		20		mA/mA
Write Current Constant "K"	Iw = K/Rwc	36	40	44	V
Differential Head Voltage Swing	Open Head, Iw = 20 mA	11	13		Vp-p
Head Differential Load Resistance Rd	SSI 32R2103R/2104R	200	250	300	Ω
	SSI 32R2103/2104	1000	1500	2000	Ω
	SSI 32R2105R	400	500	600	Ω
	SSI 32R2105	1000	1500	2000	Ω
WD Pulse Width	PWH	5			ns
	PWL	5			ns
Unselected Head Voltage				0.1	VDC
Unselected Head Current				0.2	mA
VCC Fault Voltage	Iw ≤ 0.2 mA	3.9	4.1	4.3	V
VDD Fault Voltage	Iw ≤ 0.2 mA	8.5	9.3	10	V
Head Current HnX, HnY	VCC, VDD Low Voltage Fault Condition	-0.2		0.2	mA

SERVO WRITE CHARACTERISTICS

Write Current Range		10		20	mA
Write Current Matching	Between Channels		±10		%
WUS/SE Voltage	Servo Bank Write Enabled		VCC +1.5	VCC +1.9	V
WUS/SE Sink Current	Servo Bank Write Enabled	10			mA

READ CHARACTERISTICS

Test conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Differential Voltage Gain		Vin = 1 mVp-p @ 1 MHz	210	250	300	V/V
Voltage BW SSI 32R2103R/04R	-1 dB	|Zs| < 5 Ω, Vin = 1 mVp-p	45			MHz
	-3 dB		85			MHz
SSI 32R2105R	-1 dB		35			MHz
	-3 dB		75			MHz
Input Noise Voltage		BW = 20 MHz, Lh = 0, Rh = 0		0.45	0.63	nV/√Hz
Input Noise Current		BW = 20 MHz, Lh = 0, Rh = 0		4	10	pA/√Hz
Differential Input Capacitance		Vin = 1 mVp-p, f = 5 MHz		10	14	pF
Differential Input Resistance		Vin = 1 mVp-p, f = 5 MHz	450	750	1800	Ω
Dynamic Range		AC Input Voltage Where Gain Falls to 90% of its Small Signal Gain Value, f = 5 MHz	2	4		mVp-p
Common Mode Rejection Ratio		Vin = 0 VDC + 100 mVp-p @ 5 MHz	50	60		dB
Power Supply Rejection Ratio		100 mVp-p @ 5 MHz on VCC	50	70		dB
Channel Separation		Unselected Channels Driven With Vin = 0 VDC + 100 mVp-p	50	60		dB
Output Offset Voltage AV = 250		Lh = 0, Rh = 0	-300		300	mV
Single-Ended Output Resistance		f = 5 MHz		30		Ω
Output Current (p-p)		AC Coupled Load, RDX to RDY	3	5		mA
RDX, RDY Common Mode Output Voltage				VCC -2.2		VDC

ELECTRICAL SPECIFICATIONS (continued)

SWITCHING CHARACTERISTICS

Test conditions apply unless otherwise specified.

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
R/$\overline{W}$	Read to Write	R/$\overline{W}$ to 90% of Write Current			0.15	µs
	Write to Read	R/$\overline{W}$ to 90% of 100 mV Read Signal Envelope			0.20	µs
$\overline{CS}$	Unselect to Select	CS to 90% of 100 mV 10 MHz Read Signal Envelope			0.20	µs
	Select to Unselect	CS to 10% of Write Current			0.15	µs
HS0,1, 2, 3 to any Head		To 90% of 100 mV 10 MHz Read Signal Envelope			0.15	µs
WUS	Safe to Unsafe (TD1)	Write Mode, Loss of WD Transitions; Defines Maximum WD Period for WUS Operation	0.6	2	3.6	µs
	Unsafe to Safe (TD2)	Fault Cleared: From First WD Transition		0.1	0.2	µs
WDI	Frequency Range	Valid WUS	1		100	MHz
Head Current		Lh = 0, Rh = 0				
	WD - $\overline{WD}$ to Ix - Iy (TD3)	50% to 50%		3	5	ns
	WDX - WDY to Ix - Iy (TD3)	50% to 50%		3	5	ns
	Asymmetry	WD has 1 ns Rise/Fall Time			0.5	ns
	Rise/Fall Time	10% to 90% Points Iw = 20 mA, Rh = 0, Lh = 0			3	ns
		Iw = 20 mA, Rh = 20 Ω, Lh = 600 nH			7	ns

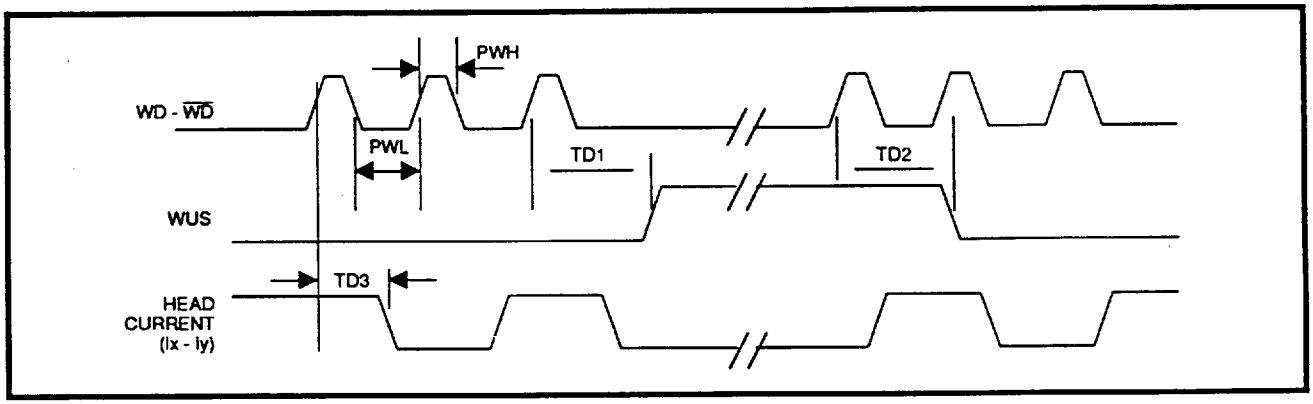


FIGURE 1: Write Mode Timing Diagram (SSI 32R2103R/05R)

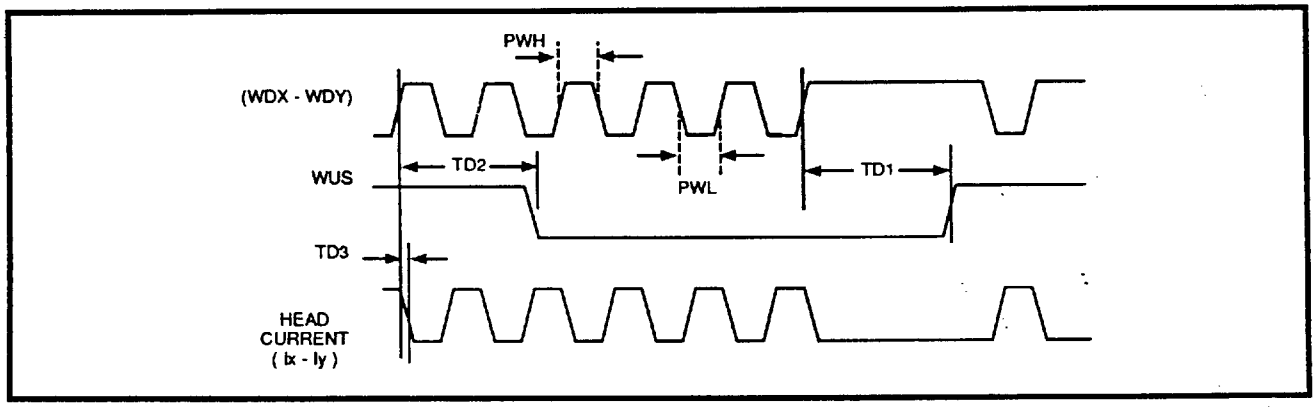
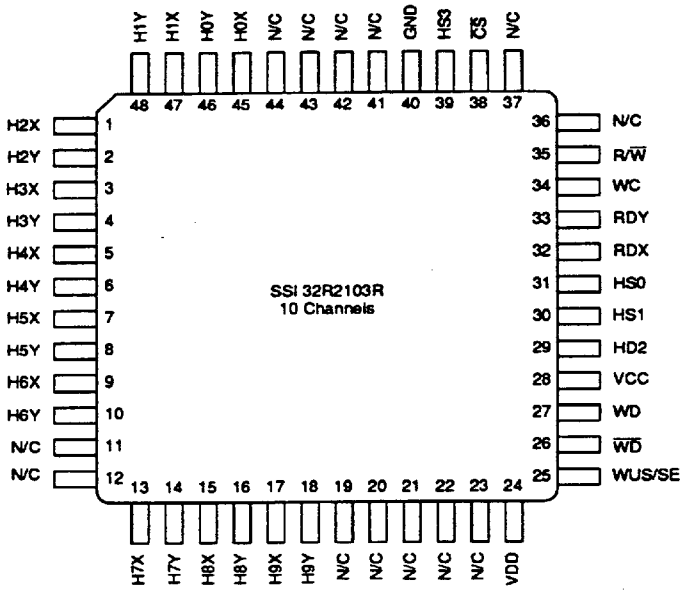


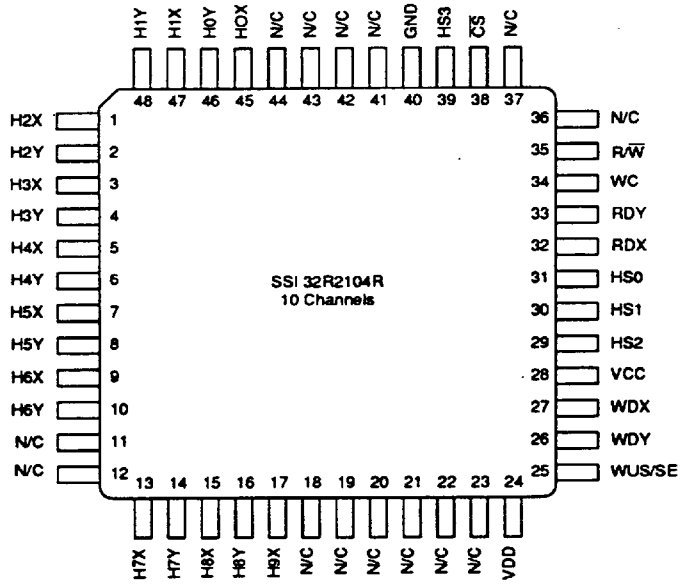
FIGURE 2: Write Mode Timing Diagram (SSI 32R2104R)

PACKAGE PIN DESIGNATIONS

(Top View)



48-Lead
10-Channel TQFP

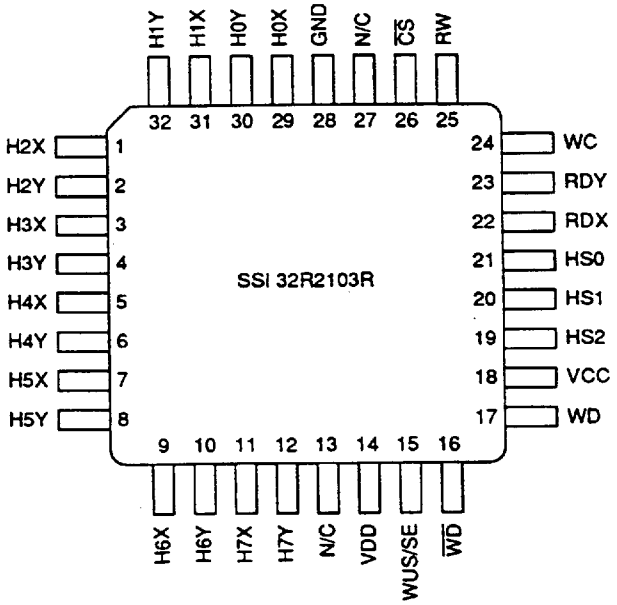


48-Lead
10-Channel TQFP

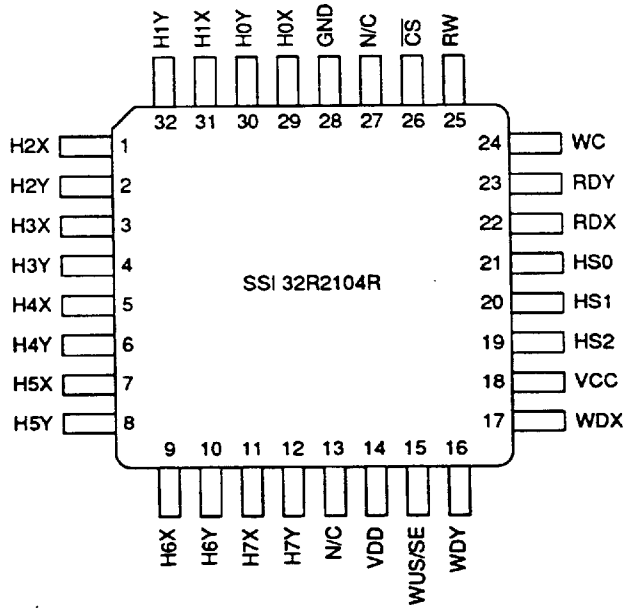
CAUTION: Use handling procedures necessary for a static sensitive component.

PACKAGE PIN DESIGNATIONS

(Top View)



32-Lead, PECL Write Data Input
8-Channel TQFP



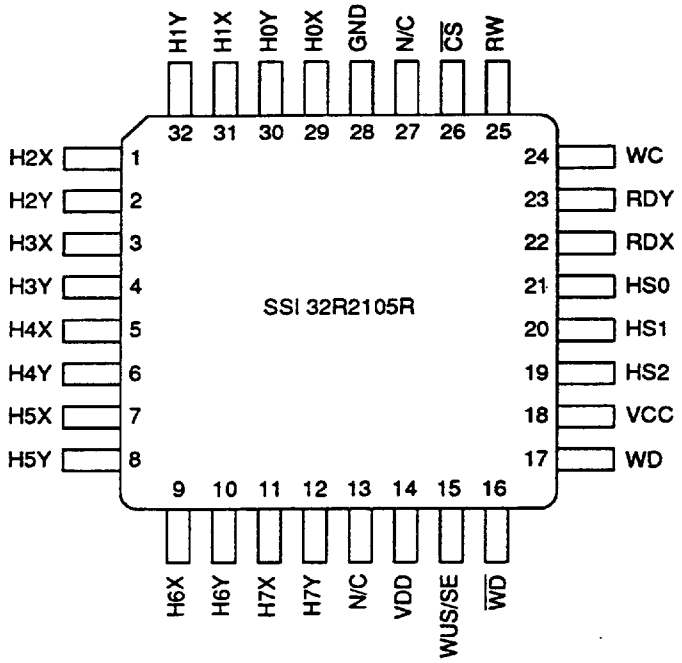
32-Lead, TTL Input Without Flip-Flop
8-Channel TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



32-Lead, PECL Write Data Input
8-Channel TQFP

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 32R2103R 8 Channel	32-Lead TQFP	32R2103RX-8CGT	32R2103RW-8
10 Channel	48-Lead TQFP	32R2103RW-10CG	32R2103RW-10
SSI 32R2104R 8 Channel	32-Lead TQFP	32R2104RW-8CGT	32R2104RW-8
10 Channel	48-Lead TQFP	32R2104RW-10CG	32R2104RW-10
SSI 32R2105R 8 Channel	32-Lead TQFP	32R2105RW-8CGT	32R21054RW-8

NOTE: These devices can be ordered with and without damping resistors. To specify devices without damping resistors, remove the "R" suffix: e.g., 32R2103W-8CGT.

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