HI-8573,4,5

Quad CMOS Op Amp/Comparator

General Description

The HI-8573, HI-8574, and HI-8575 devices are designed using low power CMOS technology. The operating current is externally programmable with a resistor to give the optimum tradeoff between power dissipation and slew rate. The operational amplifiers are internally compensated.

All three versions offer a high degree of versatility and are well suited for both line-powered and battery-powered systems. Features include a typical offset voltage of ±5mV, high input impedance and low current drain. Either single or dual power supply operation may be used up to 15VDC. The comparators are CMOS and TTL compatible. The three devices are direct replacements for the Motorola MC14573, MC14574 and MC14575, respectively.

Some typical applications include oscillators, function generators, active filters, logic level converters, A to D converters, voltage reference, zero cross detectors, limit set alarm detectors, and instrumentation.

Features

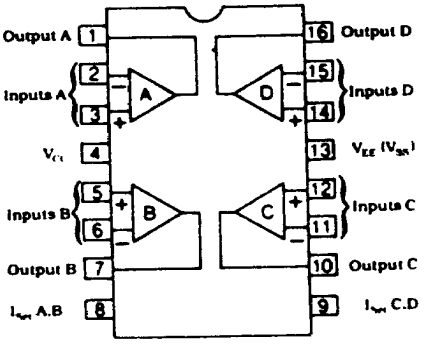
- Single or Dual Power Supply — +3 to 15Vdc or ±1.5 to ±7.5Vdc
- Wide Input Voltage Range
- Common Mode Range Ø to V_{CC} - 2 Vdc, single supply
- Adjustable Current/Slew Rate
- Typical Offset, ±5mV
- Internally Compensated Op Amps
- High Input Impedance
- CMOS and TTL Compatible Comparators
- MIL-STD-883C Equivalent Processing Available
- Direct Replacements for Motorola MC14573, MC14574, and MC14575

Ordering Information

HI-857_ _ _

- C Commercial Processing
- M MIL-STD-883C, Class B, Method 5004
- P Plastic DIP
- D Ceramic DIP
- 3 Quad Op Amp
- 4 Quad Comparator
- 5 Dual Op Amp (Circuits A & B) and Dual Comparator (Circuits C & D)

Pin Configuration



Top View

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Absolute Maximum Ratings (Voltages Referenced to V_{EE})

DC Supply Voltage, V_{CC} ..... −0.5V to +18V	Operating Temperature Range: Plastic ..... −40°C to +85°C Ceramic ..... −55°C to +125°C
Input Voltage, All Inputs ..... −0.5V to V_{CC} +0.5V	Storage Temperature Range: Plastic ..... −40°C to +125°C Ceramic ..... −65°C to +150°C
DC Current Drain Per Input Pin 10mADC	

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operational Amplifier Electrical Characteristics (V_{EE} = 0V, T_A = 25°C)

Parameter	Symbol	V_{CC} (Vdc)	Min.	Typ.	Max.	Units
Recommended Operating Range (V_{CC} - V_{EE})	—	—	3	—	15	Vdc
Input Common Mode Voltage Range (I_{SET} = 200 μA)	V_{ICR}	5 10 15	0 0 0	— — —	3 8 13	Vdc
Output Voltage Range (I_{SET} = 50 μA) (R_L = 100K connected to V_{EE})	V_{OR}	5 10 15	1.05 1.05 1.05	— — —	4 9 14	Vdc
Input Offset Voltage (I_{SET} = 50 μA)	V_{IO}	10	—	±5	±25	mVdc
Average Temperature Coefficient of Input Offset Voltage	—	—	—	20	—	μV/°C
Input Bias Current	I_{IB}	10	—	—	1	nA
Input Offset Current	I_{IO}	10	—	—	200	pA
Open Loop Voltage Gain (I_{SET} = 50 μA)	A_{VOL}	10	—	90	—	dB
Power Supply Rejection Ratio	PSRR	10	—	70	—	dB
Common Mode Rejection Ratio	CMRR	10	—	80	—	dB
Channel Separation	—	10	—	−100	—	dB
Slew Rate (I_{SET} = 40 μA)	SR	10	—	2.5	—	V/μs
Phase Margin	Φ_M	10	—	45	—	Degrees
Supply Current — Per Pair (R_{SET} = 1MΩ)	I_{CC}	5 10 15	— — —	50 100 150	— — —	μA
Supply Current — Per Pair (R_{SET} = 100K)	I_{CC}	5 10 15	— — —	0.5 1.2 1.8	— — —	mA
Gain x Bandwidth Product (I_{SET} = 40 μA)	GBP	10	—	1.4	—	MHz

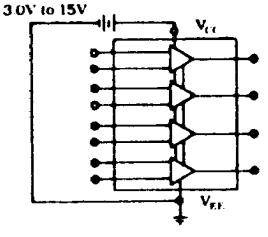
Comparator
Electrical Characteristics (V_{EE} = OV, T_A = 25°C)

Parameter	Symbol	V_{CC} (Vdc)	Min.	Typ.	Max.	Units
Recommended Operating Range (V_{CC} - V_{EE})	—	—	3	—	15	Vdc
Input Common Mode Voltage Range (I_{SET} = 200 μA)	V_{ICR}	5 10 15	0 0 0	— — —	3 8 13	Vdc
Output Low Voltage, "0" Level	V_{OL}	5 10 15	— — —	0 0 0	0.05 0.05 0.05	Vdc
Output High Voltage, "1" Level	V_{OH}	5 10 15	4.95 9.95 14.95	5 10 15	— — —	Vdc
Output Source Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5 5 10 15	−0.24 −0.51 −1.3 −3.4	−0.42 −0.88 −2.25 −8.8	— — — —	mAdc
Output Sink Current (V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5 10 15	1.25 3.25 8.5	2.25 5.6 20		mAdc
Input Offset Voltage (I_{SET} = 50 μA)	V_{IO}	10	—	±5	±25	mVdc
Average Temperature Coefficient of Input Offset Voltage	—	—	—	20	—	μV/°C
Input Bias Current	I_{IB}	10	—	—	1	nA
Input Offset Current	I_{IO}	10	—	—	200	pA
Open Loop Voltage Gain (I_{SET} = 50 μA)	A_{VOL}	10	—	96	—	dB
Power Supply Rejection Ratio	PSRR	10	—	70	—	dB
Common Mode Rejection Ratio	CMRR	10	—	80	—	dB
Channel Separation	—	10	—	−100	—	dB
Output Rise and Fall Time (C_L = 50pF)	t_{TLH} t_{THL}	10	—	100	—	ns
Propogation Delay Time, 5 mV Overdrive (I_{SET} = 50 μA, C_L = 50 pF)	t_D	10	—	1000	—	ns
Supply Current — Per Pair (R_{SET} = 1MΩ)	I_{CC}	5 10 15	— — —	50 100 150	— — —	μA
Supply Current — Per Pair (R_{SET} = 100K)	I_{CC}	5 10 15	— — —	0.45 1.0 1.5	— — —	mA

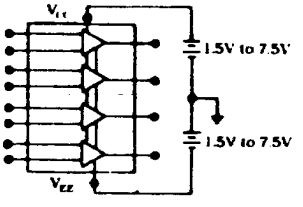
NOTE: Unused inputs should always be tied to either V_{DD} or V_{EE}

Power Options

Single Supply

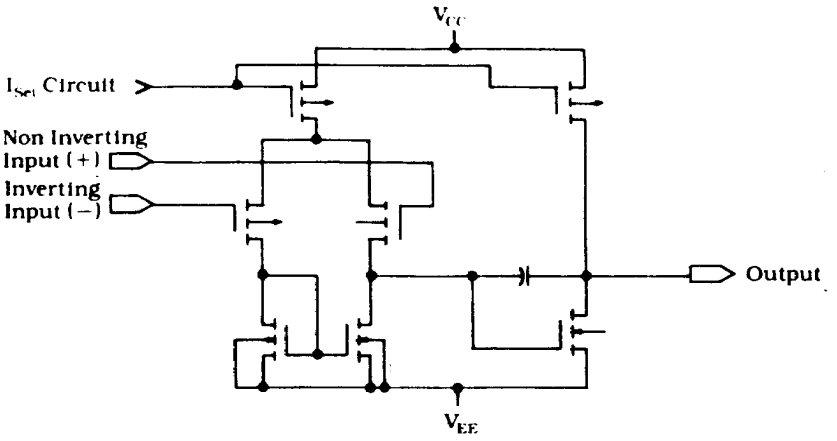


Split Supply

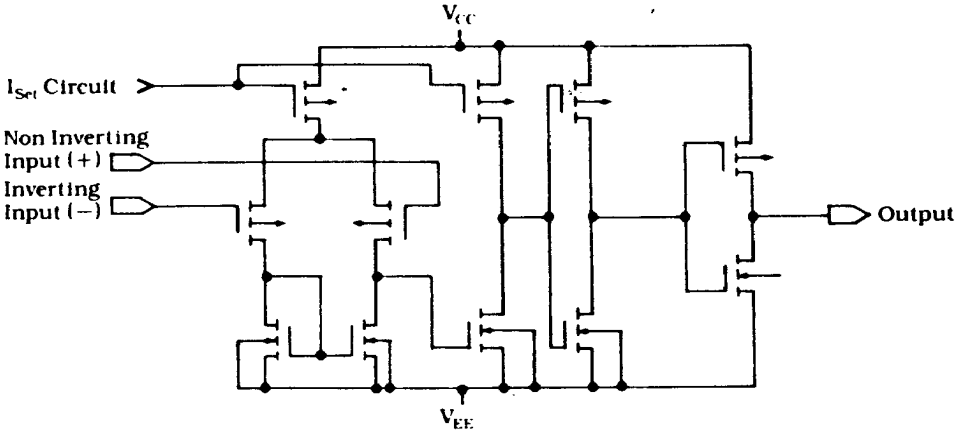


Circuit Diagrams

Operational Amplifier



Comparator



Programming Current

The programming current I_{Set} is fixed by an external resistor R_{Set} connected between V_{EE} and either one or both of the I_{Set} pins (8 and 9). When two external programming resistors are used, the set currents for each op amp pair or comparator are given by:

$$I_{Set}\,(\mu A) \cong \frac{V_{CC} - V_{EE} - 1}{R_{Set}\,(M\Omega)}$$

Pins 8 and 9 may be tied together for use with a single programming resistor. The set currents for each op amp pair or comparator pair are then given by:

$$I_{Set\,A,B} = I_{Set\,C,D}\,(\mu A) \cong \frac{V_{CC} - V_{EE} - 1}{2\,R_{Set}\,(M\Omega)}$$

If a pair of op amps or comparators are not used, the I_{Set} pin for that pair may be tied to V_{CC} for minimum power consumption.

It should be noted that increasing I_{Set} for comparators will decrease propogation delay for that comparator.

For operational amplifiers, the maximum obtainable output voltage (V_{OH}) for a given load resistor connected to V_{EE} is given by:

$$V_{OH} = (4 \times 10^{-3}\, I_{Set})\, R_L - 0.05 \text{ v. } R_L \text{ in K}\Omega$$

$$\text{if } (4 \times 10^{-3}\, I_{Set})\, R_L < V_{DD}.\ I_{Set} \text{ in } \mu A$$

Typical op amp slew rates are given by:

$$S_R \cong 0.05\, I_{Set}\ (V/\mu s),\ I_{Set} \text{ in } \mu A$$

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