HB561409 Series

262,144-word x 9-bit Dynamic Random Access Memory Module

The HB561409 is a 256k x 9 dynamic RAM module, mounted 9 pieces of 256k-bit DRAM (HM51256CP) sealed in PLCC package. An outline of the HB561409 is 30-pin single in-line package having two types; Lead type (HB561409A) and Socket type (HB561409B). Therefore, the HB561409 makes high density mounting possible without surface mount technology. The HB561409 provides common data input and output, and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors to reduce noise.

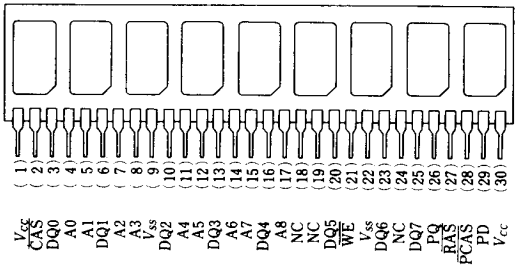
Features

- 262,144 words x 9 bits organization
- Industry standard 30-pin Single In-line Package Memory Module
- Single 5V (±10%)
- Utilizes nine 256K Dynamic RAMs in PLCC (HM51256CP)
- HB561409A/B operates as nine HM51256CPs as shown in the functional block diagram
- Low Power: Operating . . . . . 1,800mW (typ) (t_{RC} = 180ns)
  Standby . . . . . 60mW (typ)
- High speed: Access time from $\overline{RAS}$ (max) = 100ns
  Access time from address (max) = 55ns
  Read or write cycle (min) = 180ns
- High speed page mode capability (t_{PC} = 65ns)
- TTL compatible
- 256 refresh cycles/4ms
- 3 variations of refresh
  $\overline{RAS}$-only refresh
  $\overline{CAS}$-before-$\overline{RAS}$ refresh
  Hidden refresh
- Operating Ambient Air Temperature . . . . . 0°C to +70°C.

Ordering Information

Type No.	Access Time	Package
HB561409A-10	100ns	30-pin SIP Lead Type
HB561409B-10	100ns	30-pin SIMM Socket Type

Pin Arrangement



(Side View)

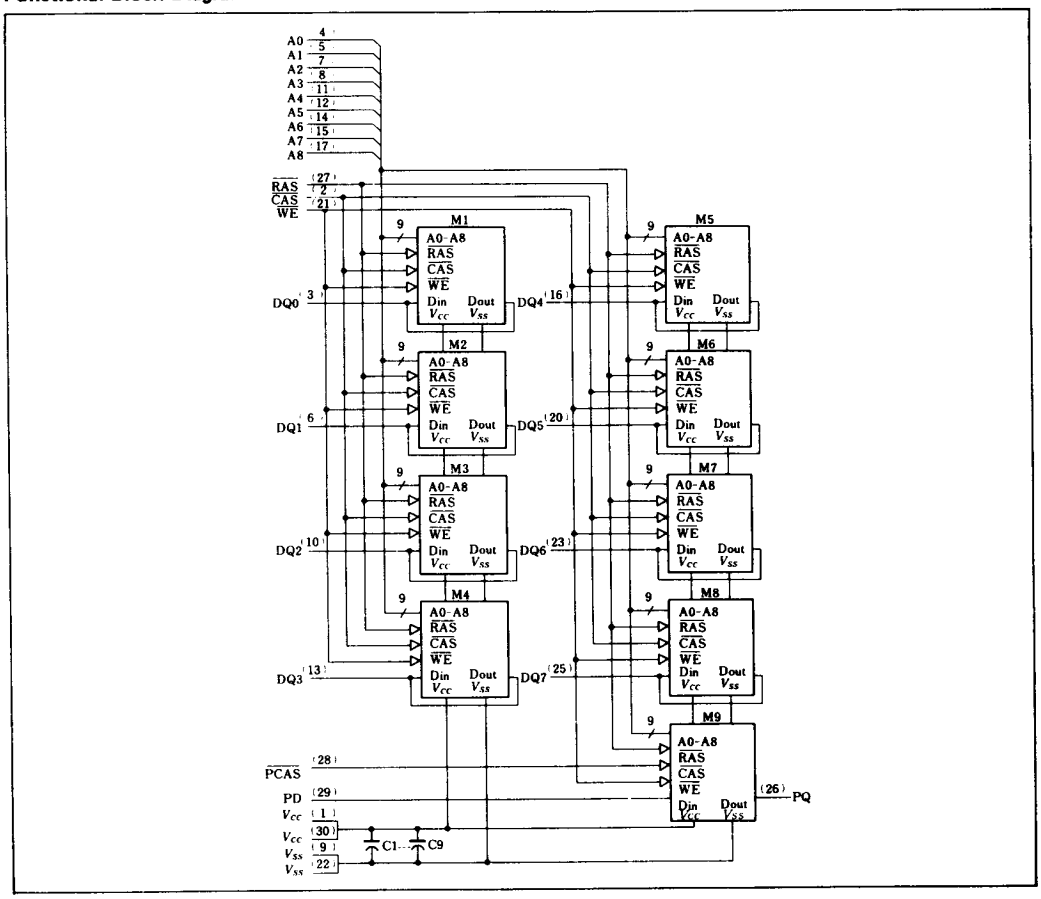
Notes:
1. HB561409B's pin arrangement is same as HB561409A's.
2. Common $\overline{CAS}$ control for eight common Data-In and Data-Out lines.
3. Separate $\overline{PCAS}$ control for one separate pair of Data-In and Data-Outlines.
4. The common I/O feature dictates the use of only early write operations to prevent contention on Din and Dout.

Pin Description

A0-A8	Address Inputs
$\overline{CAS}$, $\overline{PCAS}$	Column Address Strobe
DQ0-DQ7	Data In/Data Out
PD	Data In
NC	No Connection
PQ	Data Out
$\overline{RAS}$	Row Address Strobe
Vcc	+5V Supply
Vss	Ground
$\overline{WE}$	Write Enable

HITACHI
Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

Functional Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to V_{SS} . . . . . −1V to +7V
Operating temperature, T_a (Ambient) . . . . . 0°C to +70°C
Storage temperature (Ambient) . . . . . −55°C to +125°C
Power dissipation 9W
Short circuit output current 50mA

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	Vcc	4.5	5.0	5.5	V	1
Input High voltage	V_{IH}	2.4	—	5.5	V	1
Input Low voltage	V_{IL}	−1.0	—	0.8	V	1

Note) 1. All voltages referenced to V_{SS}.

DC Electrical Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min	Max	Unit	Notes
Operating current t_{RC} = 180ns	Icc1	—	540	mA	*1
Standby current	Icc2	—	18	mA	
Refresh current t_{RC} = 180ns	Icc3	—	540	mA	$\overline{RAS}$ only refresh
Standby current (Dout Enable)	Icc4	—	54	mA	*1
Refresh current t_{RC} = 180ns	Icc5	—	495	mA	$\overline{CAS}$ before $\overline{RAS}$ refresh
Operating current t_{PC} = 65ns	Icc6	—	540	mA	*1, High speed page mode
Input leakage 0 < Vin < 7V	I_{LI}	−10	10	μA	
Output leakage 0 < Vout < 7V	I_{LO}	−10	10	μA	Dout is disabled
Output levels High Iout = −5mA	V_{OH}	2.4	Vcc	V	
Low Iout = 4.2mA	V_{OL}	0	0.4	V	

Notes: *1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.

Capacitance (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter	Symbol	Type	Max	Unit	Notes
Address	C_{I1}	—	60	pF	*1
Clocks	C_{I2}	—	75	pF	*1,2
DQ	$C_{I/O}$	—	17	pF	*1,2
PQ	C_O	—	12	pF	*1,2
PD	C_{I3}	—	10	pF	*1

Notes: *1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
*2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics

Read, Write and Refresh Cycles (Common Parameter) (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min	Max	Unit	Notes
Random Read or Write Cycle Time	t_{RC}	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	75	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	30	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	ns	
Column Address Hold Time	t_{CAH}	25	—	ns	
Column Address Hold Time to $\overline{RAS}$	t_{AR}	80	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	70	ns	*8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	20	45	ns	*9
$\overline{RAS}$ Hold Time	t_{RSH}	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	ns	*7
Refresh Period	t_{REF}	—	4	ms	

• Read Cycle

Parameter	Symbol	Min	Max	Unit	Notes
Access Time from $\overline{RAS}$	t_{RAS}	—	100	ns	*2, *3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	ns	*3, *4
Access Time from Address	t_{AA}	—	55	ns	*3, *5
Read Command Set-up Time	t_{RCS}	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	30	ns	*6

• Write Cycle

Parameter	Symbol	Min	Max	Unit	Notes
Write Command Set-up Time	t_{WCS}	0	—	ns	*10
Write Command Hold Time	t_{WCH}	30	—	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	85	—	ns	
Write Command Pulse Width	t_{WP}	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	ns	
Data-in Set-up Time	t_{DS}	0	—	ns	*11
Data-in Hold Time	t_{DH}	25	—	ns	*11
Data-in Hold Time to $\overline{RAS}$	t_{DHR}	80	—	ns	

• Refresh Cycle

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	15	—	ns	

• High Speed Page Mode Cycle

Parameter	Symbol	Min	Max	Unit	Notes
High Speed Page Mode Cycle Time	t_{PC}	65	—	ns	*12
High Speed Page Mode $\overline{RAS}$ Pulse Width	t_{RAPC}	75	75000	ns	*13
$\overline{CAS}$ Precharge Time	t_{CP}	20	—	ns	
Write Invalid Time	t_{WI}	15	—	ns	
Access Time from Column Precharge Time	t_{CAP}	—	60	ns	*14

Notes) *1. AC measurements assume t_T = 5ns.
*2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
*3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
*4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max).
*5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \geqq t_{RAD}$ (max.)
*6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage level.
*7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

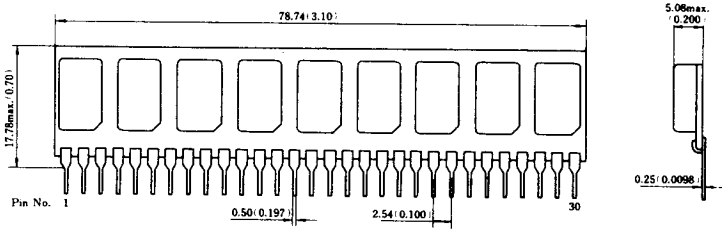
8. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
10. Only early write cycle to prevent contention on Data in and out ($t_{WCS} \geqq 0$).
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycle.
12. Assumes that $t_{ASC} = t_{CP}$-5ns.
13. t_{RAPC} defines $\overline{RAS}$ pulse width in High Speed Page mode cycle.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CAP}.
15. An initial pause of 100μs is required after power-up then execute at least 8 initialization cycles.
16. At least, 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required before using an internal refresh counter.

Timing Waveforms

Refer to the HM51256CP data sheet.

Package Outline, Unit; mm (inch)

HB561409A



HB561409B