ESS Technology, Inc.

ES56-I Series
56K / V.90 Modem Solutions
Data Sheet

DESCRIPTION

The ES56 chipset series is a highly integrated solution which brings advanced modem functionality to notebook and desktop systems. The ES56-I from ESS Technology provides a complete 56k (V.90) data/fax solution, while the ES56T-I adds a Telephone Answering Machine (TAM) feature and the ES56V-I adds a full-duplex speakerphone feature.

The ES56 series data pump algorithms run on the ES2890S DSP along with the echo-cancellation required for implementing a full-duplex speakerphone feature. The host CPU is utilized to run the modem controller functions, including the standard AT command set, V.42*bis* data compression features, Classes 1 and 2 fax and ITU-T V.80 sync access to support H.324 video conferencing applications. The ES2890S DSP offers an integrated ISA/ PnP bus interface. The ES56-I and the ES56T-I chipsets feature the ES2818 AFE, while the ES56V-I features the ES2819 AFE.

The ES2818 AFE is a single sigma-delta CODEC that provides the analog phone line interface only, while the ES2819 AFE is a dual-sigma delta CODEC that provides both the analog phone line and speakerphone interfaces. The ES2890S DSP is availabe in a 100-pin TQFP package, while both the ES2818 and ES2819 AFEs are available in 52-pin PQFP packages. The ES2818 AFE is also available in a 28-pin SOIC package.

MODEM FEATURES

- Data Mode capabilities
  - V.90 56K bps
  - V.34 33.6 kbps and fallbacks
  - Standard AT command set
  - V.42 (LAPM) and MNP error correction
  - V.42bis/MNP 5 data compression
  - 3.3 V power supply, 5 V – input tolerant
- Fax Mode capabilities
  - ITU-T V.17, V.21 ch2, V.27ter, V.29
  - Group 3 (TIA/EIA 578 Class 1 and Class 2)
- Telephony capabilities
  - Telephone Answering Machine
  - Full Duplex Speakerphone
  - Caller ID
- TIES escape sequence
- ISA/PnP
- Windows 95
  - UNIMODEM V
  - TAPI
- Windows NT
- DOS box compatible
- V.80 (H.324 software stack compatible)
- Small real estate for economical notebook design

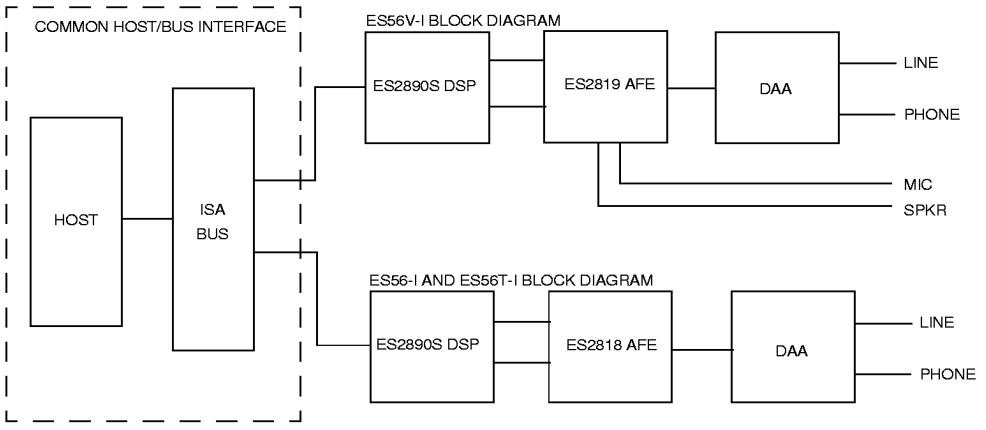

Figure 1 ES56-I Series Block Diagrams

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FIGURES

TABLES

CHIPSET BLOCK DIAGRAMS

Figure 2 depicts the ES2890S DSP device internals.

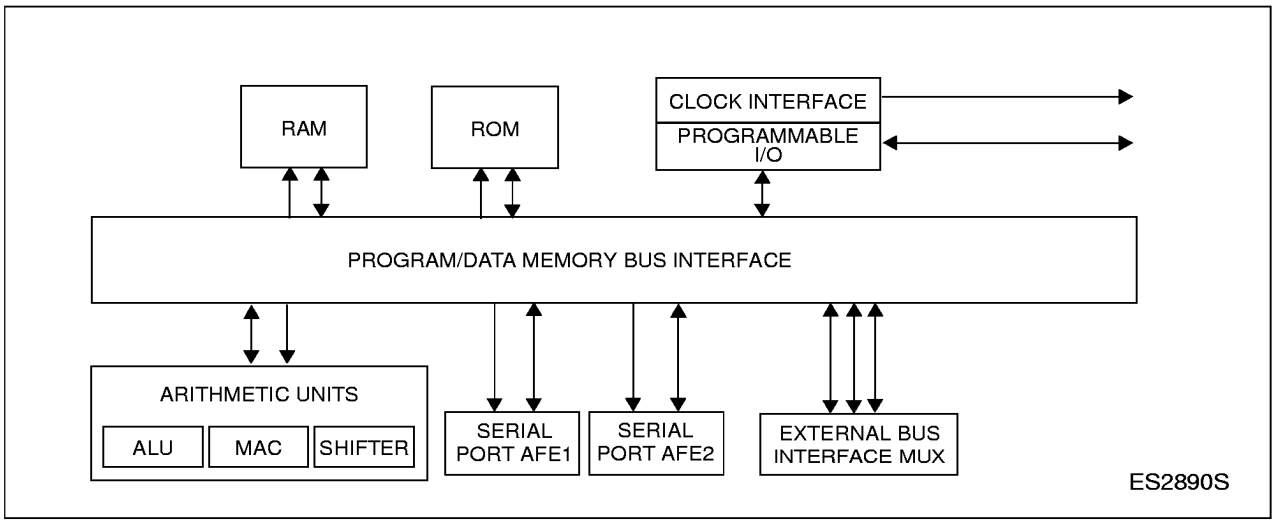

Figure 2 ES2890S Block Diagram

Figure 3 depicts the ES2818 AFE device internals for both package outlines. The ES2819 AFE device has two sets of the same components as the ES2818 AFE and is otherwise identical in functionality.

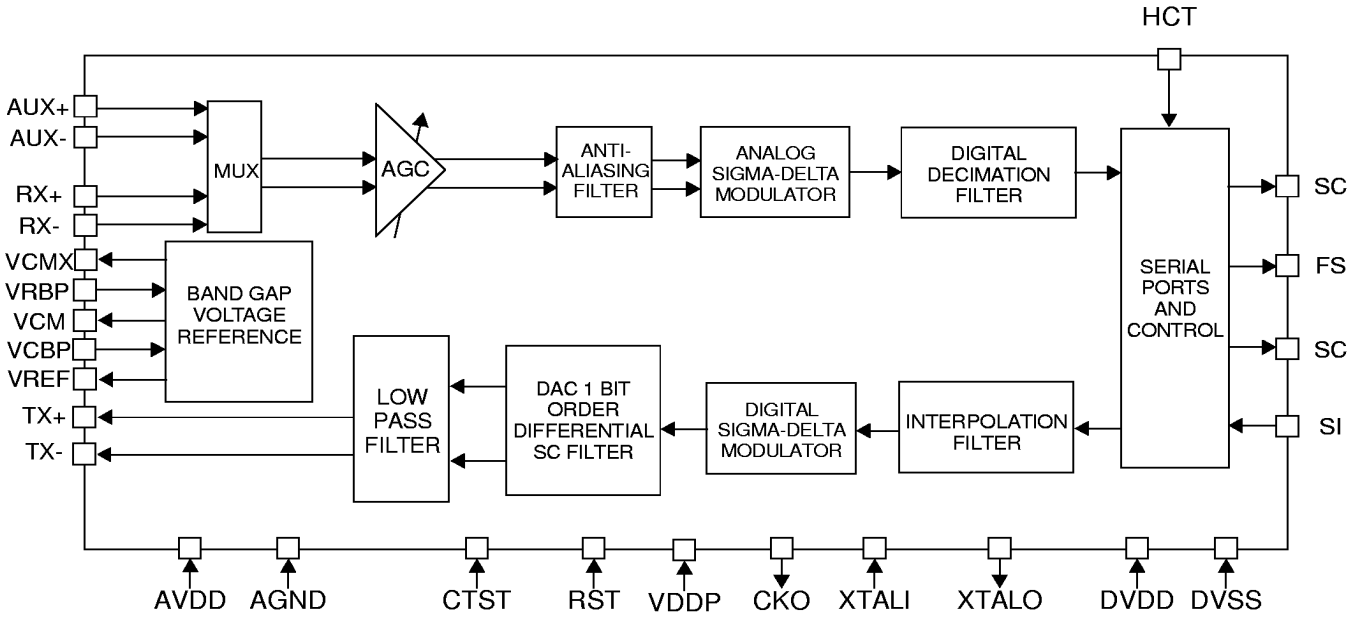

Figure 3 Modem AFE Block Diagram

FUNCTIONAL DESCRIPTION

The ES56-I series chipsets from ESS Technology include the ES2890S DSP and either the ES2818 AFE or the ES2819 AFE.

Each ES56-I series chipset is designed to support 56k (V.90), V.34 and all legacy communication standards, including V.42, MNP 2-4, V.42*bis*/MNP 5 and Group 3 Fax.

ES2890S Digital Signal Processor

The ES2890S digital signal processor is a single-modem device designed to work with both the ES2818 and ES2819 AFEs to provide a hardware-based modem solution. A modem with the ES2890S and driver creates a hardware accelerated modem with minimal impact on the host processor. Less than 5 percent of the available MIPS of a 233 MHz Pentium™ processor with MMX™ is necessary to run the host-based controller function. This solution is ideal for high performance systems or for systems with processors fully taxed from running other applications.

Clock and Reset

The ES2890S can be clocked by either a crystal or a TTL-compatible clock signal. The CLKIN input cannot be halted, changed during operation or operated below its programmed frequency except when the ES2890S is in the D2 or D3 powerdown state. The CLKOUT pin of the ES2890S may also be disabled to reduce external power dissipation. Using the CLKOUT pin allows the clock out frequency to be programmed using the equation:

$$\text{Freq} = \text{DSP clock}/2n$$

where *n* is any value between 1 and 255.

The RESET signal initiates a master reset of the ES2890S and is asserted during power-up to assure proper initialization. The RESET signal must be held at least 10 DSP clock cycles to allow the internal clock to stabilize.

IDMA Transfer Using the ISA Bus

When the ES2890S interfaces to an ISA bus, pins 1:13, 23:40 and 98:100 function as the 16-bit bus input address path, while pins 23:40 function as the 16-bit bus I/O data path for communicating with the host when the IDMA select function is enabled.

Operating Modes

The ES2890S has user-configurable dual-purpose pins that are used in PnP mode to generate an internal chip select if desired. Setting BSEL pins 61 (BSEL0) and 45 (BSEL1) in the 00 state configures the devices to be in ISA PnP mode with internal chip select. Setting the BSEL[1:0] pins (pins 61 and 45) in the 01 state configures the devices to be in ISA mode with external chip select. See Table 1 for a complete list of all available operating modes.

Table 1 Basic Operating Mode Selection

BSEL[1:0]	Basic Operating Mode
00	ISA mode with internal chip select.
01	ISA mode with external chip select.
11	Generic 16-bit host interface.

ES2890S Internal Registers

The ES2890S DSP chip contains 16 internal configuration registers and a series of PnP support registers divided into card-control registers and device registers. The internal registers are accessed by adding an offset to the ISA base address. Internal memory-mapped and non memory-mapped registers are included in the ES2890S, but are not visible to the user.

The sixteen internal registers are divided into two sets of eight registers, defined as I/O[0] and I/O[1]. When an external PnP chip select is used, only the eight I/O[0] registers are visible. When an internal PnP chip select is used, both the I/O[0] and I/O[1] register sets are visible. However, the first four registers of I/O[0] are not used as they are dedicated for use in external PnP chip select mode.

In the I/O[0] register set, the Base + 0 and Base + 1 registers are not used.

I/O[0] Register Set

EDSP Control **(Base+2h, W)**

		APM mode	EDSP RST	Reserved			
7	6	5	4	3	2	1	0

External Chip Select, write-only.

Bit Definitions:

Bits	Name	Description
5	APM mode	1 = Sleep mode.
4	EDSP RST	1 = Reset.

Hardware Configuration (Base+3h, R)

	PDN	Reserved	AFE
7	6	5 4 3 2	1 0

External Chip Select, read-only.

Bit Definitions:

Bits	Name	Description
5	PDN	Power-down status.
1:0	AFE	AFE type.

DSP Address Cycle (Base+4h, R/W)

Lower byte
7 6 5 4 3 2 1 0

DSP Address Cycle (Base+5h, R/W)

Upper byte
7 6 5 4 3 2 1 0

DSP Data Cycle (Base+6h, R/W)

Lower byte
7 6 5 4 3 2 1 0

DSP Data Cycle (Base+7h, R/W)

Upper byte
7 6 5 4 3 2 1 0

I/O[1] Register Set

PnP Configuration Address (Base+0h, R/W)

7 6 5 4 3 2 1 0

PnP Configuration Data (Base+1h, R/W)

7 6 5 4 3 2 1 0

EEPROM Data Port (Base+2h, R/W)

7 6 5 4 3 2 1 0

EEPROM Command Port (Base+3h, R/W)

Reserved	Command
7 6 5 4	3 2 1 0

Command Field Encoding.

Bit Definitions:

Bits	Name	Description				
3:0	Command	Bit 3	Bit 2	Bit 1	Bit 0	Function
		0	0	0	0	Write disable
		0	0	0	1	Write all
		0	0	1	0	Erase all
		0	0	1	1	Write enable
		0	1	0	0	Write
		0	1	0	1	Reserved
		0	1	1	0	Reserved
		0	1	1	1	Reserved
		1	0	0	0	Read
		1	0	0	1	Reserved
		1	0	1	0	Reserved
		1	0	1	1	Reserved
		1	1	0	0	Erase
		1	1	0	1	Reserved
		1	1	1	0	Reserved
		1	1	1	1	Reserved

Reset EEPROM Address (Base+4h, R/W)

7 6 5 4 3 2 1 0

Status (Base+5h, R/W)

IN	IE	EET	PPS	PPE	BR
7	6	5 4	3 2	1	0

Bit Definitions:

Bits	Name	Description	
7	IN	Interrupt.	
6	IE	Interrupt enable.	
5:4	EET	Bit 5	Bit 4
		0	0 Internal ROM
		0	1 External EERPOM
		1	0 Reserved
		1	1 Reserved
3:2	PPS	Bit 3	Bit 2
		0	0 Wait-for-key
		0	1 Sleep
		1	0 Isolation
		1	1 Configuration
1	PPE	PnP enable.	
0	BR	Byte ready for EEPROM data.	

EDSP Control (Base+6h, W)

		APM	RST	Reserved			
7	6	5	4	3	2	1	0

Internal Chip Select, write-only.

Bit Definitions:

Bits	Name	Description
5	APM mode	1 = Sleep mode.
4	EDSP RST	1 = Reset.

EDSP Status (Base+7h, R)

	PDN	Reserved				AFE	
7	6	5	4	3	2	1	0

External Chip Select, read-only.

Bit Definitions:

Bits	Name	Description
5	PDN	Power-down status.
1:0	AFE	AFE type.

PnP Registers

The PnP registers are a set of eight-bit registers divided into two categories. These categories are card control registers and device registers.

There are eight registers in the card control category and six registers in the device register category.

Card control registers, located at logical device number 0, control status and configuration information. Device registers, located at logical device number 1, contain I/O address and interrupt information.

Card Control Registers

Set RD_DATA Port (00h, R/W)

Bits 9:2 of the PnP RD_DATA port							
7	6	5	4	3	2	1	0

The PnP Read port can be written only when the card is in Isolation mode. It is set low by hardware reset. It can be read only from Configuration mode.

Serial Isolation (01h, R)

Data							
7	6	5	4	3	2	1	0

Read-only during serial isolation state.

Configuration Control (02h, R)

					RESET_CSN	WFK	SWR
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
2	RESET_CSN	RESET_CSN command.
1	WFK	WAIT_FOR_KEY command.
0	SWR	Software reset command. Does not work in WAIT_FOR_KEY state.

Wake[CSN] (03h, W)

Data							
7	6	5	4	3	2	1	0

If data written is 00h and it:

- matches the CSN:
  this card goes from Sleep mode to Isolation mode.
- does not match the CSN:
  this card goes from Configuration mode to Sleep mode.

If the data written is non-zero, and it:

- matches the CSN:
  this card goes from Sleep mode to Configuration mode.
- does not match the CSN:
  this card goes from Isolation mode to Sleep mode.

Resource Data (04h, R)

Resource data							
7	6	5	4	3	2	1	0

Returns next byte of resource data. Only works in Configuration mode.

Status (05h, R)

Reserved							Status
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
0	Status	1 = Ready to read resource data. Only works in Configuration mode. 0 = Not ready.

CSN **(06h, R/W)**

Card select number							
7	6	5	4	3	2	1	0

Read/write card select number. Writes to the CSN register can only occur in Isolation mode and cause a transition to Configuration mode. Reads to the CSN register can only occur in Configuration mode.

LDN **(07h, R/W)**

Logical device number							
7	6	5	4	3	2	1	0

Logical device number register. Can only be accessed in Configuration mode.Device Registers

Device Registers

Activate **(30h, R/W)**

Reserved							Activate
7	6	5	4	3	2	1	0

There is one activate register associated with each logical device. After a reset or after a 1 is written to the card's configuration control bit, the default for this register is 0.

Bit Definitions:

Bits	Name	Description
0	Activate	1 = Activate. 0 = Deactivate (default).

I/O Range Check **(31h, R)**

Reserved						Enable range check	Pattern select
7	6	5	4	3	2	1	0

There is one I/O range check register associated with each logical device. The I/O Range Check register verifies that the I/O range assigned to a logical device does not conflict with the I/O range used by another device.

Bit Definitions:

Bits	Name	Description
1	Enable range check	1 = Enable range check. 0 = Disable.
0	Pattern select	1 = 55h. 0 = AAh.

I/O Decoder Base Address **(60h, R/W)**

Upper byte							
7	6	5	4	3	2	1	0

This register comprises the most-significant byte of the I/O base address of the device. If written as zero, the device is disabled.

I/O Decoder Base Address **(61h, R/W)**

Lower byte							
7	6	5	4	3	2	1	0

This register comprises the least-significant byte of the I/O base address of the device.

Interrupt Request Level Select 0 **(70h, R/W)**

Data							
7	6	5	4	3	2	1	0

Interrupt Request Type Select **(71h, R)**

0	0	0	0	0	0	1	0
7	6	5	4	3	2	1	0

This read-only register returns 2 (low-to-high transition) when read.

ES2818/ES2819 AFE

The ES2818 and ES2819 AFEs are single- and dual-CODEC devices which integrate low-pass continuous anti-aliasing filters, 16-bit resolution analog-to-digital converters (ADC), 16-bit digital-to-analog converters (DAC), low-pass output-reconstruction filters and a serial port interface. The major functions of the ES2818 and ES2819 include ADC and DAC conversion of modem signal data and to provide the interface and contol logic to transfer data between its serial I/O terminals and the ES2890S.

The ES2818 and ES2819 both include ADC signal processing channels, DAC signal processing channels and the associated digital controls for each channel. The two channels operate synchronously so that data reception at the DAC channel and data transmission from the ADC channel occur during the same time interval.

The internal circuit configuration and performance parameters are determined by reading control and configuration/test information from the Control and Configuration/Test registers. The data from the registers sets up either the ES2818 or the ES2819 for a given mode of operation and application. Data transfer is in 2's complement format.

AFE RESET

During reset, the clock divider and the Command and Configuration registers are driven to a known state. All data-path pipeline registers and accumulators are set to zero. The serial port clock defaults to a 1 MHz rate. The serial output SO is tri-stated.

AFE/HOST SERIAL PORT INTERFACE

The host interface supports a 4-pin serial interface consisting of FS, SC, SI, and SO (The slew rate of these signals is controlled to reduce the amount of Electromagnetic Interference (EMI)). Both the ES2818 and the ES2819 AFEs act as the bus master and drives the FS, SC, and SO signals. Data transfers use the first 16 bits, with the most-significant bit (MSB) first and left-aligned. This is followed by unused bits which are driven as zeros.

If HCT = 0, the least-significant bit (LSB) of the 16-bit data indicates whether the data is input for the CODEC, or a control word. A logic zero on the LSB indicates CODEC input data, while a logic one on the LSB indicates a control word. Therefore, when HCT = 0, the effective input data is only 15 bits wide. Internal control registers can only be accessed when HCT = 0. When HCT = 1, all 16 bits of data transferred to the AFE.

DATA AND FAX MODES

The ES56-I series modem chipsets support all data modem standards up to 56 Kb/s. Modulations and data rates conform to the following standards:

- ITU V.90
- ITU V.34
- ITU V.32bis
- ITU V.32
- ITU V.22bis
- ITU V.22
- ITU V.21
- Bell 212A
- Bell 103

V.42/MNP 2-4 error correction and V.42bis/MNP 5 data correction reduce error transmission and improve data throughput. The default AT command set is TIES (Time Independent Escape Sequence).

The Hayes escape sequence, which is time dependent, is optionally supported. Both escape sequences are universally accepted by communications software programs.

The Fax AT command set is compatible with EIA/TIA-578 Class 1 and Class 2 standards.Fax transmit and receive speeds up to 14.4 Kb/s are available. Fax modulations and data rates conform to the standards appearing in Tables 3 and 4.

Table 2 Fax Modes Supported

ITU Mode	Data Rate (kb/s)	Modulation
Fax Mode		
V.17	14.4	TCM
	12.0	TCM
	9.6	TCM
	7.2	TCM
V.21ch2	0.3	FSK
V.27ter	4.8	DPSK
	2.4	DPSK
V.29	9.6	QAM
	7.2	QAM
	4.8	QAM

Table 3 Data Modes Supported

ITU Mode	Data Rate (kb/s)	Modulation
Data Mode		
V.90	56	PCM
V.34	33.6	TCM
	31.2	TCM
	28.8	TCM
	26.4	TCM
	24.0	TCM
	21.6	TCM
	19.2	TCM
	16.8	TCM
	14.4	TCM
	12.0	TCM
	9.6	TCM
	7.2	TCM
	4.8	TCM
	2.4	TCM
V.32bis	14.4	TCM
	12.0	TCM
	9.6	TCM
	7.2	TCM
	4.8	TCM
V.32	9.6	TCM
	9.6	QAM
	4.8	QAM
V.22bis	2.4	QAM
V.22	1.2	DPSK
V.21	0.3	FSK
Bell 212A	1.2	DPSK
Bell 103	0.3	FSK

ES2890S DSP PINOUT

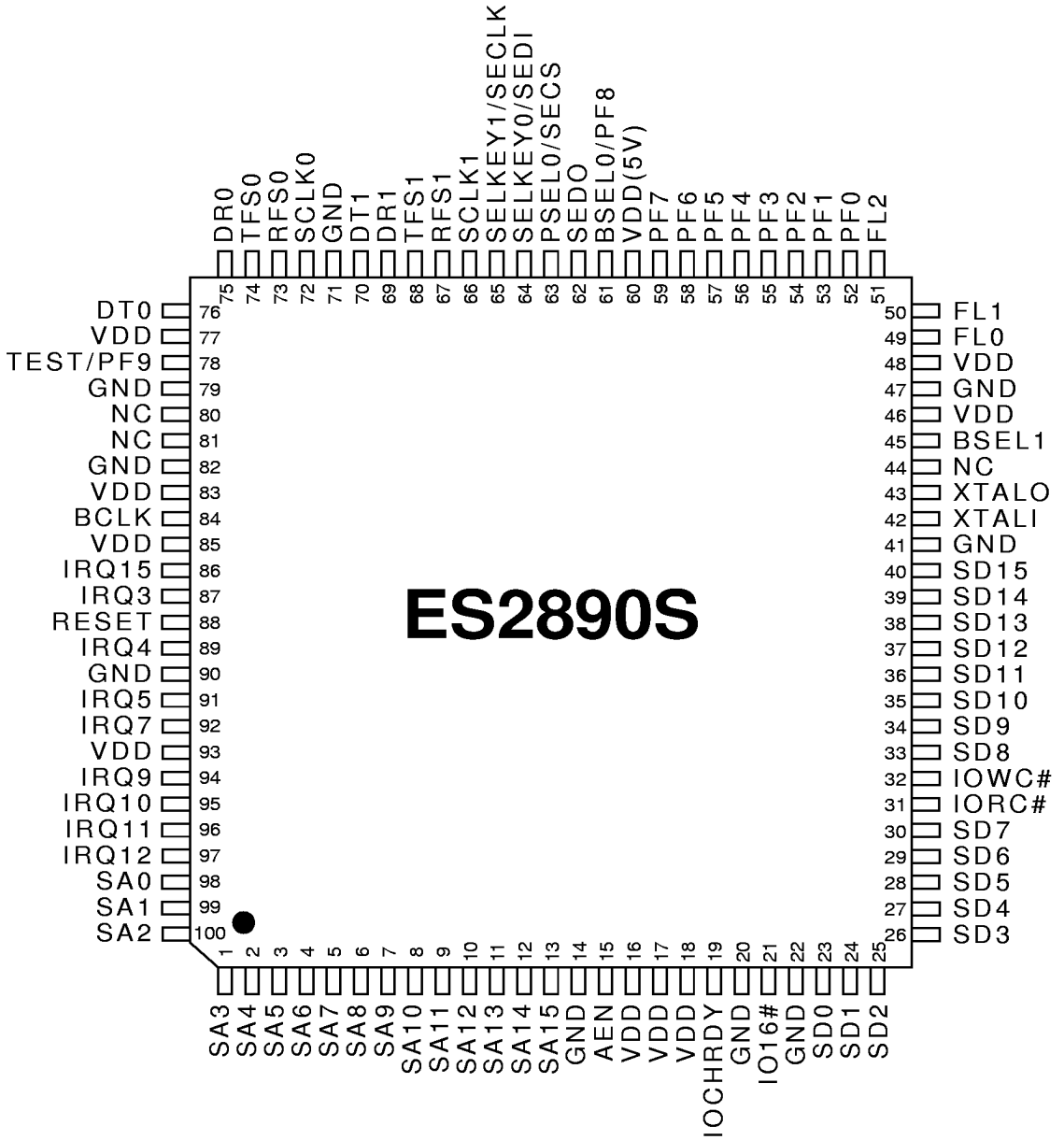

Figure 4 ES2890S DSP Pinout

ES2890S PIN DESCRIPTION

Name	Number	I/O	Definition
SA[15:0]	13,12,11,10,9,8, 7,6,5,4,3,2,1, 100,99,98	I	SA[15:0] comprise the ISA bus address inputs.
GND	14,20,22,41,47, 71,79,82,90	–	Ground.
AEN / IAL	15	I	Active-high address enable input driven by the ISA bus.
VDD	16,18,46,48,77, 83,85,93	I	Digital supply voltage, 3.3 V.
CS# / IS#	17	I	This pin is the ES2890S chip select when the device is in non-PnP mode, which requires an external chip select.When the device is in PnP mode, use an internal chip select and tie the CS pin to VDD through a 10 KΩ resistor.
IOCHRDY / IACK#	19	O	I/O channel ready output driven to the ISA bus to indicate that the I/O channel is ready to complete the I/O Read/Write bus cycle.
IO16#	21	O	IO16# is driven to the ISA bus and indicates a 16-bit I/O transfer.
SD[15:0]	40,39,38,37,36, 35,34,33,30,29, 28,27,26,25,24, 23	I/O	SD[15:0] are the system data pins of the ISA bus.
IORC#	31	I	IOR# is the I/O read signal driven by the ISA bus during a read operation.
IOWC#	32	I	IOW# is the I/O write signal driven by the ISA bus during a write operation.
XTALI	42	I	ES2890S clock input. This pin can be driven by either a crystal or an oscillator. When using a crystal, XTALO is used as the other crystal pin. When using an oscillator, the output of the oscillator is connected to XTALI. An internal clock doubler doubles the frequency at XTALI.
XTALO	43	O	Works in conjunction with XTALI when a crystal is used. When an oscillator is used, XTALO is left unconnected.
CLKOUT	44	O	Using this output pin allows the clock out frequency to be programmed. To program the frequency, refer to the following equation: Freq = DSP Clock/2n (n = 1-255)
BSEL1 / BSEL0	45,61	I	Used to determine the operating mode of the ES2890S. These pins are sampled at the falling edge of reset and are encoded as follows. Tie these pins to ground for most configurations. Refer to “Operating Mode selection” on page 37 for more information. **Configuration** / **BSEL1 (pin 45)** / **BSEL0 (pin 61)** ISA PnP mode with internal chip select / 0 / 0 ISA mode with external chip select / 0 / 1 PCI interface / 1 / 0 Generic 16-bit host interface / 1 / 1
FL0	49	O	This pin is used as the Flag 0 output during normal operation.
FL1	50	O	This pin is used as the Flag 1 output during normal operation while the bypass circuitry is included. Will be activated during power down mode.
FL2	51	O	This pin functions as the Flag 2 output during normal operation, and can also be used to provide a pass-through reset to the ES2818 AFE. The ISA interface in the ES2890S provides an I/O address, located at ISA base + 0, for resetting both the ES2890S and the ES2818 AFE. To reset these devices through the ISA interface, write a logic one to ISA base + 0. To bring the devices out of reset, write a logic zero. FL2 carries the reset signal for the ES2818 AFE.

Name	Number	I/O	Definition
PF[7:0]	52,53,54,55,56, 57,58,59	I/O	General-purpose programmable bi-directional flag pins. These pins can be used for interfacing with a telephone or other device, performing such functions as phone off-hook, phone on-hook, ring, caller ID, and so on. PF[0] is specially designed to support the ring function.
VDD(5V)	60	I	Digital supply voltage. If the ES2890S interface with a 5 V input, tie this pin to 5 V. Otherwise, tie this pin to 3.3 V.
SEDO	62	I	Data input when an external EEPROM is used. If an EEPROM is not used, connect this pin to ground.
SECS	63	I/O	This dual-purpose pin indicates the presence of an external EEPROM in PnP mode. If sampled low at reset (EEPROM not present), the pin is left unconnected. If sampled high at reset, the pin functions as the SECS output, which is connected to the chip select input of the EEPROM.
SEDI	64	I/O	This dual-purpose pin is used in PnP mode when the ES2890S generates an internal chip select. The pin can be configured either as an input or an output depending on its state at the falling edge of reset. If sampled low at reset, the pin functions as the SELKEY0 input, which is used along with BSEL[1:0] to configure the device. If sampled high at reset, the pin functions as the SEDI output, which connects to the data input of an external EEPROM. If the EEPROM is present, tie this pin to ground through a 10 KΩ resistor. If an external EEPROM is not present, tie this pin directly to ground, to indicate SELKEY0 mode. Refer to “Operating Mode selection” on page 37 for more information.
SECLK	65	I/O	This dual-purpose pin is used in PnP mode. Functionality is determined at the falling edge of reset. If sampled low at reset, the pin functions as the SELKEY1 input, which is used along with BSEL[1:0] to configure the device. If sampled high at reset, the pin functions as the clock input to an external EEPROM. If the EEPROM is present, tie this pin to ground through a 10 KΩ resistor. If the external EEPROM is not present, tie this pin directly to ground to indicate SELKEY1 mode. Refer to “Operating Mode selection” on page 37 for more information.
SCLK1	66	I/O	One of two serial clock inputs. This clock can be generated either internally by the ES2890S, or externally by the ES2818. Leave this pin unconnected for the ES2808.
RFS1	67	I/O	Receive frame for serial port 1. Can be generated either internally or externally. This signal is asserted one clock before data is sent on the DR1 pin. Leave this pin unconnected for the ES2808.
TFS1	68	I/O	Transmit frame for serial port 1. Can be generated either internally or externally.
DR1	69	I	Data receive pin for serial port 1.
DT1	70	O	Data transmit pin for serial port 1.
SCLK0	72	I/O	One of two serial clock inputs. This clock can be generated either internally by the ES2890S, or externally by the ES2818.
RFS0	73	I/O	Receive frame for serial port 0. Can be generated either internally or externally. This signal is asserted one clock before data is sent on the DR0 pin.
TFS0	74	I/O	Transmit frame for serial port 0. Can be generated either internally or externally.
DR0	75	I	Data receive pin for serial port 0.
DT0	76	O	Data transmit pin for serial port 0.
TEST / PF9	78	I	This pin is used during device test. Tie this pin to ground through a 10KΩ resistor.
RING_IN	79	I	This pin is used for ring detect input during the $D3_{cold}$ state to drive the device back to its default powerup state.
V_{AUX}	80	I	Power to device during implementation of the $D3_{cold}$ state required by PCI Power Management Interface Specification.

Name	Number	I/O	Definition
PME#	81	O	PME# output.
BCLK	84	I	ISA bus input clock. This pin is tied to the SYSCLK pin on the ISA bus and operates between 6 and 12 MHz.
IRQ [3,4,5,7,9,10, 11,12,15]	87,89,91,92, 95,96,97,86	O	Interrupt request outputs. These pins are driven to the ISA bus and indicate an interrupt request on the specified pin. All interrupt request outputs are active-high. Unselected IRQ outputs are high-impedance. If the ES2890S interfaces to a PCI bus, the IRQ pins each have a specific function.
RESET	88	I	Active-high ES2890S reset input.
DAA_PM	94	O	DAA power control output.

ES2818F MODEM AFE PINOUT

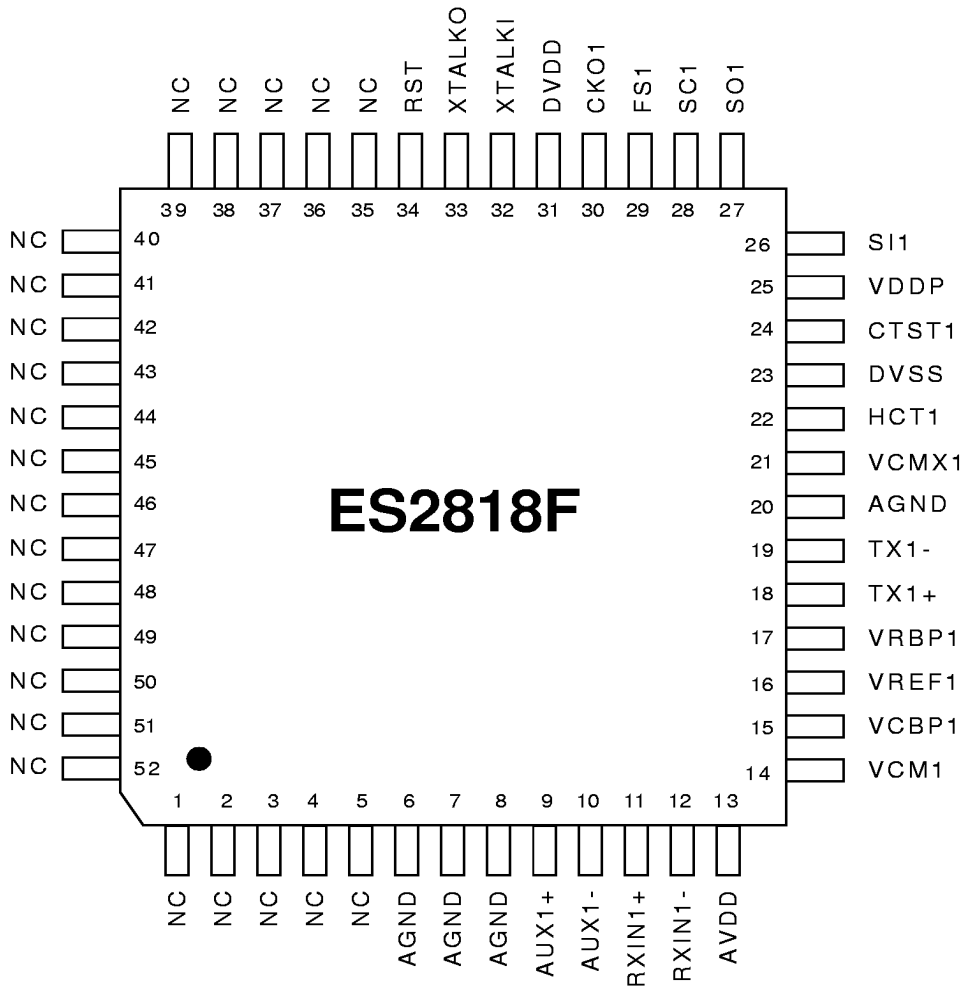

Figure 5 ES2818F Modem AFE Pinout

ES2818F PIN DESCRIPTION

Name	Number	I/O	Description
NC	52:35, 5:1	–	No connection.
AGND	8:6	I	Analog ground.
AUX1+	9	I	CODEC 1 analog auxiliary differential positive input. The DC level is V_{cm} and the full scale ac input is either 2.2 V_{p-p} ± 5% or 1.1 V_{p-p} ± 5% depending on the gain setting.
AUX1-	10	I	CODEC 1 analog auxiliary differential negative input. The DC level is V_{cm} and the full scale ac input is either 2.2 V_{p-p} ± 5% or 1.1 V_{p-p} ± 5% depending on the gain setting.
RXIN1+	11	I	CODEC 1 analog auxiliary differential positive input. The DC level is V_{cm} and the full scale ac input is either 2.2 V_{p-p} ± 5% or 1.1 V_{p-p} ± 5% depending on the gain setting.
RXIN1-	12	I	CODEC 1 analog differential negative input. The DC level is V_{cm} and the full scale ac input is either 2.2 V_{p-p} ± 5% or 1.1 V_{p-p} ± 5% depending on the gain setting.
AVDD	13	I	Analog 5 V supply.
VCM1	14	O	Common mode voltage bypass 1. Has a range of 2.16 volt ± 5%. Bypass to VCBP1 with 0.1 µF ceramic chip capacitor parallel with 10 µF tantalum capacitor.
VCBP1	15	I	Ground pin for VCM1.
VREF1	16	O	Voltage reference bypass 1. Has a range of 1.235 volt ± 5%. Bypass to GND2 with 0.1 µF ceramic chip capacitor parallel with 10 µF tantalum capacitor.
VRBP1	17	I	Ground pin for VREF1.
TX1+	18	O	CODEC 1 positive analog output. The DC level is V_{cm} and the full scale ac output is either 2.8 V_{p-p} ± 5% or 1.4 V_{p-p} ± 5% depending on the gain setting. The maximum loading is 20kΩ in parallel with 20 pF for modem applications. For audio applications with low-impedance load, the maximum distortion-free (THD < -60 dB) current is 10 mA_{rms}.
TX1-	19	O	CODEC 1 negative analog output. The DC level is V_{cm} and the full scale ac output is either 2.8 V_{p-p} ± 5% or 1.4 V_{p-p} ± 5% depending on the gain setting. The maximum loading is 20kΩ in parallel with 20 pF for modem applications. For audio applications with low-impedance load, the maximum distortion-free (THD < -60 dB) current is 10 mA_{rms}.
AGND	20	I	Analog ground.
VCMX1	21	O	CODEC 1 common mode reference voltage output pin. 2.16 ± 5% volt, maximum current ± 500 µA, maximum capacitive load 20 pF.
HCT1	22	I	CODEC 1 digital input mode control pin.
DVSS	23		Digital ground.
CTST1	24	I	CODEC 1 Sigma Delta Modulator test port output enable.
VDDP	25	I	3.3 V for clock output.
SI1	26	I	Serial port 1 input.
SO1	27	O	Serial port 1 output.
SC1	28	O	Serial port 1 clock output.
FS1	29	O	Serial port 1 frame synchronize.
CKO1	30	O	18.816 MHz clock output.
DVDD	31	I	Digital 5 V power supply.
XTALK1	32	I	18.816 MHz crystal oscillator input.
XTALKO	33	O	Crystal oscillator output.
RST	34	I	Reset pin.

ES2818P MODEM AFE PINOUT

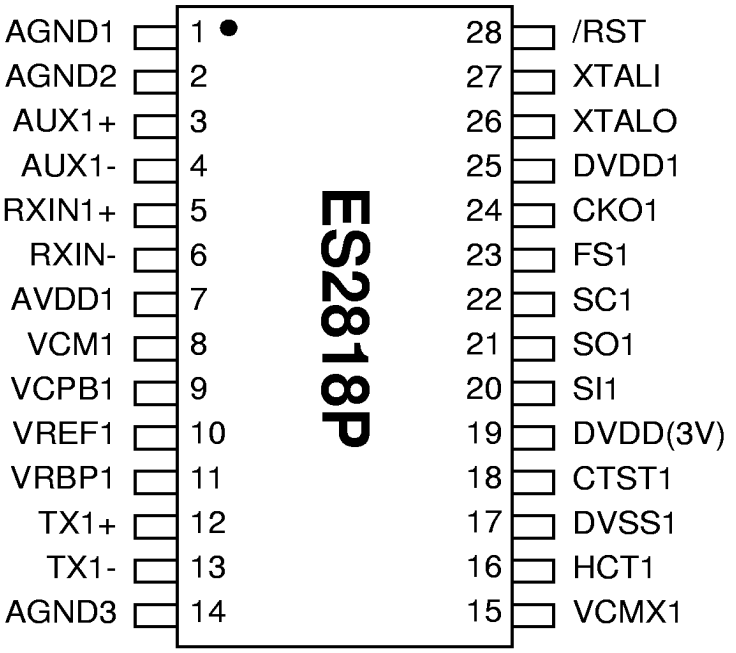

Figure 6 ES2818P Modem AFE Pinout

ES2818P PIN DESCRIPTION

Name	Number	I/O	Description
AGND	1,2,14	I	Analog ground
AUX1+	3	I	CODEC 1 analog auxiliary differential positive input. The DC level is V_{cm} and the full scale ac input is either 2.2 V_{p-p} ± 5% or 1.1 V_{p-p} ± 5% depending on the gain setting.
AUX1-	4	I	CODEC 1 analog auxiliary differential negative input. The DC level is V_{cm} and the full scale ac input is either 2.2 V_{p-p} ± 5% or 1.1 V_{p-p} ± 5% depending on the gain setting.
RXIN1+	5	I	CODEC 1 analog auxiliary differential positive input. The DC level is V_{cm} and the full scale ac input is either 2.2 V_{p-p} ± 5% or 1.1 V_{p-p} ± 5% depending on the gain setting.
RXIN1-	6	I	CODEC 1 analog differential negative input. The DC level is V_{cm} and the full scale ac input is either 2.2 V_{p-p} ± 5% or 1.1 V_{p-p} ± 5% depending on the gain setting.
AVDD	7	I	Analog 5 V supply.
VCM1	8	O	Common mode voltage bypass 1. Has a range of 2.16 volt ± 5%. Bypass to VCBP1 with 0.1 µF ceramic chip capacitor parallel with 10 µF tantalum capacitor.
VCBP1	9	I	Ground pin for VCM1.
VREF1	10	O	Voltage reference bypass 1. Has a range of 1.235 volt ± 5%. Bypass to GND2 with 0.1 µF ceramic chip capacitor parallel with 10 µF tantalum capacitor.
VRBP1	11	I	Ground pin for VREF1.
TX1+	12	O	CODEC 1 positive analog output. The DC level is V_{cm} and the full scale ac output is either 2.8 V_{p-p} ± 5% or 1.4 V_{p-p} ± 5% depending on the gain setting. The maximum loading is 20kΩ in parallel with 20 pF for modem applications. For audio applications with low-impedance load, the maximum distortion-free (THD < -60 dB) current is 10 mA $_{rms}$.
TX1-	13	O	CODEC 1 negative analog output. The DC level is V_{cm} and the full scale ac output is either 2.8 V_{p-p} ± 5% or 1.4 V_{p-p} ± 5% depending on the gain setting. The maximum loading is 20kΩ in parallel with 20 pF for modem applications. For audio applications with low-impedance load, the maximum distortion-free (THD < -60 dB) current is 10 mA $_{rms}$.
VCMX1	15	O	CODEC 1 common mode reference voltage output pin. 2.16 ± 5% volt, maximum current ± 500 µA, maximum capacitive load 20 pF.
HCT1	16	I	CODEC 1 digital input mode control pin.
DVSS (3V)	17		3V digital ground.
CTST1	18	I	CODEC 1 Sigma Delta Modulator test port output enable.
DVDD (3V)	19, 25	I	3.3 V for clock output.
SI1	20	I	Serial port 1 input.
SO1	21	O	Serial port 1 output.
SC1	22	O	Serial port 1 clock output.
FS1	23	O	Serial port 1 frame synchronize.
CKO1	24	O	18.432 MHz clock output.
XTALKO	26	O	18.432 MHz crystal oscillator output.
XTALKI	27	I	18.432 MHz crystal oscillator input.
RST	28	I	Reset pin.

ES2819F MODEM AFE PINOUT

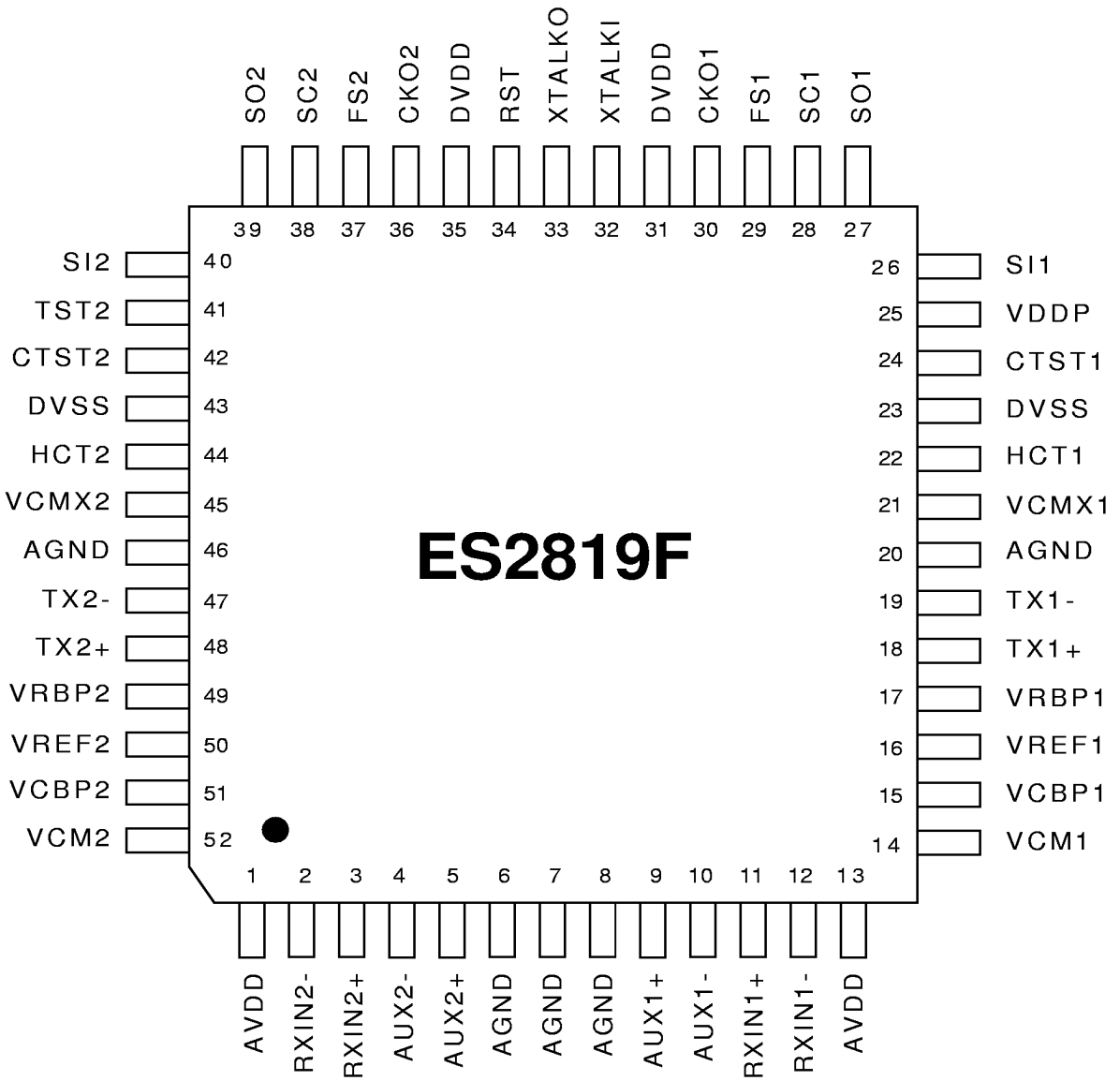

Figure 7 ES2819 Modem AFE Pinout

ES2819F PIN DESCRIPTION

Name	Number	I/O	Description
AVDD	1	I	Analog +5V power supply.
RXIN2-	2	I	CODEC 2 analog auxiliary differential negative input. The DC level is V_{cm} and the full scale ac input is either 2.2 V_{p-p} ± 5% or 1.1 V_{p-p} ± 5% depending on the gain setting.
RXIN2+-	3	I	CODEC 2 analog differential positive input. The DC level is V_{cm} and the full scale ac input is either 2.2 V_{p-p} ± 5% or 1.1 V_{p-p} ± 5% depending on the gain setting.
AUX2-	4	I	CODEC 1 analog auxiliary differential negative input. The DC level is V_{cm} and the full scale ac input is either 2.2 V_{p-p} ± 5% or 1.1 V_{p-p} ± 5% depending on the gain setting.
AUX2+	5	I	CODEC 1 analog auxiliary differential positive input. The DC level is V_{cm} and the full scale ac input is either 2.2 V_{p-p} ± 5% or 1.1 V_{p-p} ± 5% depending on the gain setting.
AGND	8:6	I	Analog ground.
AUX1+	9	I	CODEC 1 analog auxiliary differential positive input. The DC level is V_{cm} and the full scale ac input is either 2.2 V_{p-p} ± 5% or 1.1 V_{p-p} ± 5% depending on the gain setting.
AUX1-	10	I	CODEC 1 analog auxiliary differential negative input. The DC level is V_{cm} and the full scale ac input is either 2.2 V_{p-p} ± 5% or 1.1 V_{p-p} ± 5% depending on the gain setting.
RXIN1+	11	I	CODEC 1 analog auxiliary differential positive input. The DC level is V_{cm} and the full scale ac input is either 2.2 V_{p-p} ± 5% or 1.1 V_{p-p} ± 5% depending on the gain setting.
RXIN1-	12	I	CODEC 1 analog differential negative input. The DC level is V_{cm} and the full scale ac input is either 2.2 V_{p-p} ± 5% or 1.1 V_{p-p} ± 5% depending on the gain setting.
AVDD	13	I	Analog 5 V supply.
VCM1	14	O	Common mode voltage bypass 1. Has a range of 2.16 volt ± 5%. Bypass to VCBP1 with 0.1 µF ceramic chip capacitor parallel with 10 µF tantalum capacitor.
VCBP1	15	I	Ground pin for VCM1.
VREF1	16	O	Voltage reference bypass 1. Has a range of 1.235 volt ± 5%. Bypass to GND2 with 0.1 µF ceramic chip capacitor parallel with 10 µF tantalum capacitor.
VRBP1	17	I	Ground pin for VREF1.
TX1+	18	O	CODEC 1 positive analog output. The DC level is V_{cm} and the full scale ac output is either 2.8 V_{p-p} ± 5% or 1.4 V_{p-p} ± 5% depending on the gain setting. The maximum loading is 20kΩ in parallel with 100 pF for modem applications. For audio applications with low-impedance load, the maximum distortion-free (THD < -60 dB) current is 10 mA_{rms}.
TX1-	19	O	CODEC 1 negative analog output. The DC level is V_{cm} and the full scale ac output is either 2.8 V_{p-p} ± 5% or 1.4 V_{p-p} ± 5% depending on the gain setting. The maximum loading is 20kΩ in parallel with 100 pF for modem applications. For audio applications with low-impedance load, the maximum distortion-free (THD < -60 dB) current is 10 mA_{rms}.
AGND	20, 46	I	Analog ground.
VCMX1	21	O	CODEC 1 common mode reference voltage output pin. 2.16 ± 5% volt, maximum current ± 500 µA, maximum capacitive load 20 pF.
HCT1	22	I	CODEC 1 digital input mode control pin.
DVSS	23, 43		Digital ground.
CTST1	24	I	CODEC 1 Sigma Delta Modulator test port output enable.
VDDP	25	I	Reserved on ES2819. 3.3 V for clock output on ES2819A.
SI1	26	I	Serial port 1 input.
SO1	27	O	Serial port 1 output.

Name	Number	I/O	Description
SC1	28	O	Serial port 1 clock output.
FS1	29	O	Serial port 1 frame synchronize.
CKO1	30	O	Reserved on 2819. 18.816 MHz clock output on ES2819A.
DVDD	31.35	I	Digital 5 V power supply.
XTALKI	32	I	18.816 MHz crystal oscillator input.
XTALKO	33	O	Crystal oscillator output.
RST	34	I	Reset pin.
CKO2	36	O	CODEC 2 Sigma Delta Modulator clock. CKO2 can be used to clock TST2 data.
FS2	37	O	Serial port 2 frame synchronize.
SC2	38	O	Serial port 2 clock output.
SO2	39	O	Serial port 2 output.
SI2	40	I	Serial port 2 input.
TST2	41	o	CODEC 2 Sigma Dela Modulator test port.
CTST2	42	I	CODEC 2 Sigma Delta Modulator test port output enable.
HCT2	44	I	CODEC 2 digital input mode control pin.
VCMX2	45	O	CODEC 2 common mode reference voltage output pin.
TX2-	47	O	CODEC 2 negative analog output.
TX2+	48	O	CODEC 2 positive analog output.
VRBP2	49	I	Ground pin for VREF2.
VREF2	50	O	Voltage reference bypass 2.
VCBP2	51	I	Ground pin for VCM2.
VCM2	52	O	Common mode voltage bypass 2.

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Table 4 ES2890S Absolute Maximum Ratings

Parameter	Definition	Min	Max	Unit
V_{DD}	DC supply voltage	-0.3	7.0	V
V_{IN}	Input voltage	-0.3	V_{DD}+0.3	V
I_{IN}	Input current	-1	1	mA
I_{DO}	Digital output current	-20	20	mA
I_{AO}	Analog output current	-10	10	mA
T_O	Operating temperature	0	70	°C
T_{ST}	Storage temperature	-40	125	°C
P_{MAX}	Maximum power dissipation		200	mW

Table 5 ES2890S Electrical Characteristics

Parameter	Definition	Test Conditions	Min	Max	Unit
V_{DD}	Supply voltage		3.0	3.6	V
T_{AMB}	Ambient operating temperature		0	70	°C
V_{IH}	High-level input voltage	V_{DD} = max	2.0		V
V_{OH}	High-level output voltage	V_{DD} = min (I_{OH} = -0.5 mA)	2.4		V
V_{IL}	Low-level input voltage	V_{DD} = max		0.8	V
V_{OL}	Low-level output voltage	V_{DD} = min (I_{OL}= 2 mA)		0.4	V
V_{IHX}	High-level input XTAL_IN voltage	V_{DD} = max	2.2		V
I_{IH}	High-level input current	V_{DD} = 5.0V		TBD	µA
		V_{DD} = 3.3V		TBD	µA
I_{IL}	Low-level input current	V_{DD} = max		TBD	µA
I_{DDI}	Supply current (idle)	V_{DD} = max		16.5	mA
I_{DDD}	Supply current (dynamic) ES2890S	V_{DD} = max		90	mA
C_I	Input pin capacitance	V_{IN} = 2.5 V (F_{IN} = 1 MHz)		8	pF

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Table 6 ES2818F/ES2818P Absolute Maximum Ratings

Parameter	Definition	Min	Max	Unit
V_{DD}	DC supply voltage	-0.3	7.0	V
V_{IN}	Input voltage	-0.3	V_{DD}+0.3	V
I_{IN}	Input current	-1	1	mA
I_{DO}	Digital output current	-20	20	mA
I_{AO}	Analog output current	-10	10	mA
T_O	Operating temperature	0	70	°C
T_{ST}	Storage temperature	-40	125	°C
P_{MAX}	Maximum power dissipation		150	mW

Table 7 ES2818F/ES2818P DC Electrical Characteristics

Parameter	Definition	Min	Typ	Max	Unit
Single Digital/Analog Power Supply					
V_{DD}	Supply voltage	4.75	5.0	5.25	V
I_{DDA}	Analog supply current		16		mA
I_{DDD}	Digital supply current		17		mA
I_{DLP}	Low power mode supply current		10		µA
V_{CM}	Common mode output voltage		2.16		V
Separate Digital and Analog Power Supplies					
V_{DDD}	Digital supply voltage	4.75	5.0	5.25	V
V_{ADD}	Analog supply voltage	4.75	5.0	5.25	V
I_{DDA}	Analog supply current		18		mA
I_{DDD}	Digital supply current		22		mA
V_{CM}	Common mode output voltage		2.16		V
Digital Circuits (V_{DDD} = 3.3 V, T_A = 25 °C)					
V_{IH}	High-level input voltage	V_{DDD}-0.5			V
V_{OH}	High-level output voltage	V_{DDD}-0.5			V
V_{IL}	Low-level input voltage	-0.3		0.5	V
V_{OL}	Low-level output voltage			0.3	V
I_{IN}	Input current	-10	±1	10	µA
Digital Circuits (V_{DDD} = 3.3 V, T_A = 25 °C)					
V_{IH}	High level input voltage	V_{DDD}-0.5			V
V_{OH}	High level output voltage	V_{DDD}-0.5			V
V_{IL}	Low level input voltage	-0.3		0.5	V
V_{OL}	Low level output voltage			0.3	V
I_{IN}	Input current	-10	±1	10	µA
Analog Circuits					
V_{REF}	Differential reference output voltage		1.235		V
T_{CO}	Vref temperature coefficient		200		ppm/°C
V_{ICMO}	Input common mode offset voltage	-300		300	mV
V_{IDIF}	Differential input voltage		2 x V_{REF}		Vpp
V_{SEI}	Single-ended input voltage		V_{REF}		Vpp
V_{DIO}	Differential input DC offset voltage	-100		100	mV
V_{OCMO}	Output common mode offset voltage	-200		200	mV
V_{DIFO}	Differential output voltage		2 x V_{REF}		V
V_{DOO}	Differential output DC offset voltage	-100		100	mV
R_{IN}	Input resistance	100			kΩ
R_{OUT}	Output resistance			20	Ω
R_{LOAD}	Load resistance	10			kΩ
C_{LOAD}	Load capacitance			20	pF

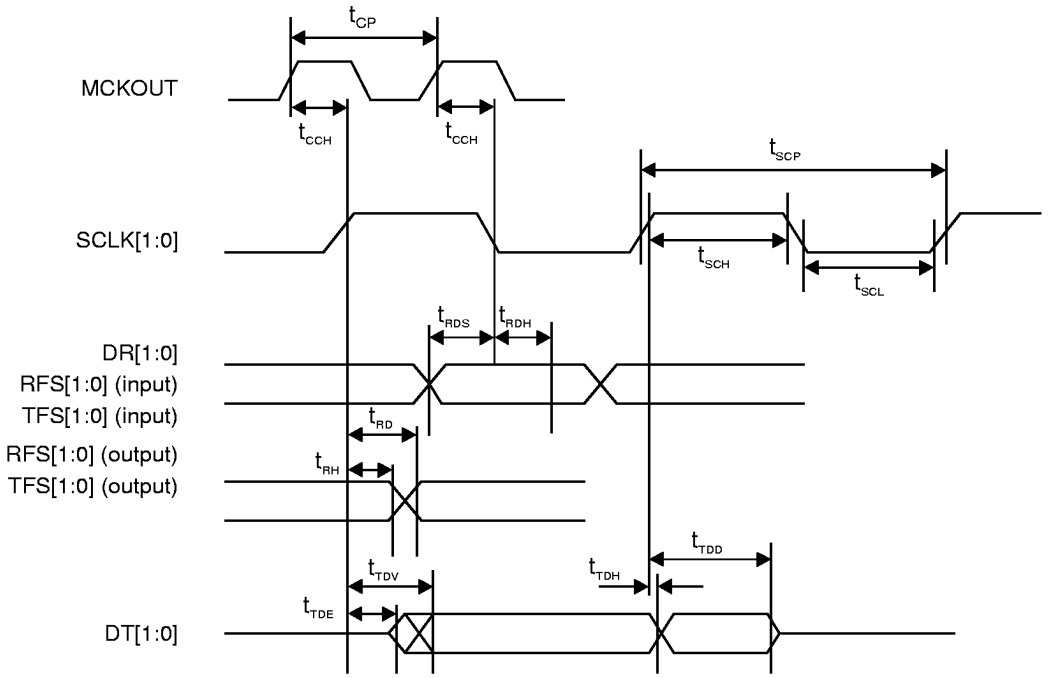
Table 8 ES2819F Absolute Maximum Ratings

Parameter	Definition	Min	Max	Unit
V_{DD}	DC supply voltage	-0.3	7.0	V
V_{IN}	Input voltage	-0.3	V_{DD}+0.3	V
I_{IN}	Input current	-1	1	mA
I_{DO}	Digital output current	-20	20	mA
I_{AO}	Analog output current	-10	10	mA
T_O	Operating temperature	0	70	°C
T_{ST}	Storage temperature	-40	125	°C
P_{MAX}	Maximum power dissipation		300	mW

Table 9 ES2819F DC Electrical Characteristics

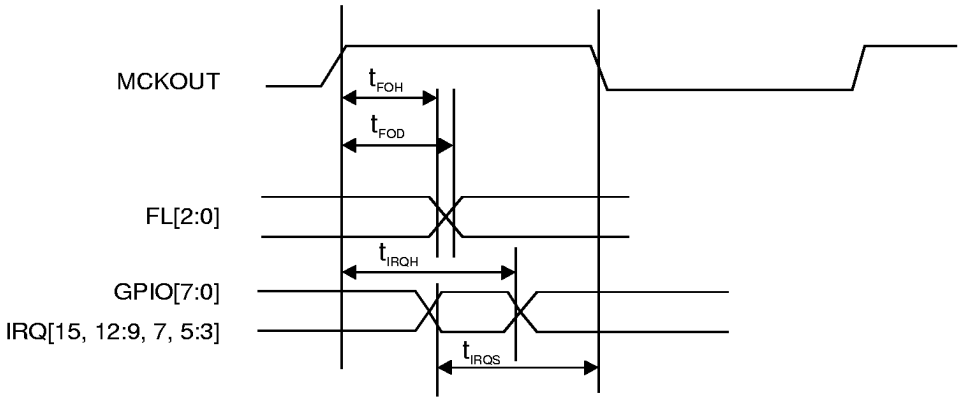
Parameter	Definition	Min	Typ	Max	Unit
Single Digital/Analog Power Supply					
V_{DD}	Supply voltage	4.75	5.0	5.25	V
I_{DDA}	Analog supply current		32		mA
I_{DDD}	Digital supply current		34		mA
I_{DLP}	Low power mode supply current		10		µA
V_{CM}	Common mode output voltage	$V_{DD}/2$ - 5%	$V_{DD}/2$	$V_{DD}/2$ + 5%	V
Separate Digital and Analog Power Supplies					
V_{DDD}	Digital supply voltage	4.75	5.0	5.25	V
V_{ADD}	Analog supply voltage	4.75	5.0	5.25	V
I_{DDA}	Analog supply current		36		mA
I_{DDD}	Digital supply current		44		mA
V_{CM}	Common mode output voltage	$V_{DD}/2$ - 5%	$V_{DD}/2$	$V_{DD}/2$ + 5%	V
Digital Circuits (V_{DDD} = 3.3 V, T_A = 25 °C)					
V_{IH}	High-level input voltage	V_{DDD} -0.5			V
V_{OH}	High-level output voltage	V_{DDD} -0.5			V
V_{IL}	Low-level input voltage	-0.3		0.5	V
V_{OL}	Low-level output voltage			0.3	V
I_{IN}	Input current	-10	±1	10	µA
Digital Circuits (V_{DDD} = 3.3 V, T_A = 25 °C)					
V_{IH}	High level input voltage	V_{DDD} -0.5			V
V_{OH}	High level output voltage	V_{DDD} -0.5			V
V_{IL}	Low level input voltage	-0.3		0.5	V
V_{OL}	Low level output voltage			0.3	V
I_{IN}	Input current	-10	±1	10	µA
Analog Circuits					
V_{REF}	Differential reference output voltage		1.235		V
T_{CO}	Vref temperature coefficient		200		ppm/°C
V_{ICMO}	Input common mode offset voltage	-300		300	mV
V_{IDIF}	Differential input voltage		2 x V_{REF}		Vpp
V_{SEI}	Single-ended input voltage		V_{REF}		Vpp
V_{DIO}	Differential input DC offset voltage	-100		100	mV
V_{OCMO}	Output common mode offset voltage	-200		200	mV
V_{DIFO}	Differential output voltage		2 x V_{REF}		V
V_{DOO}	Differential output DC offset voltage	-100		100	mV
R_{IN}	Input resistance	100			kΩ
R_{OUT}	Output resistance			20	Ω
R_{LOAD}	Load resistance	10			kΩ
C_{LOAD}	Load capacitance			20	pF

ES2890S TIMING DIAGRAMS/CHARACTERISTICS



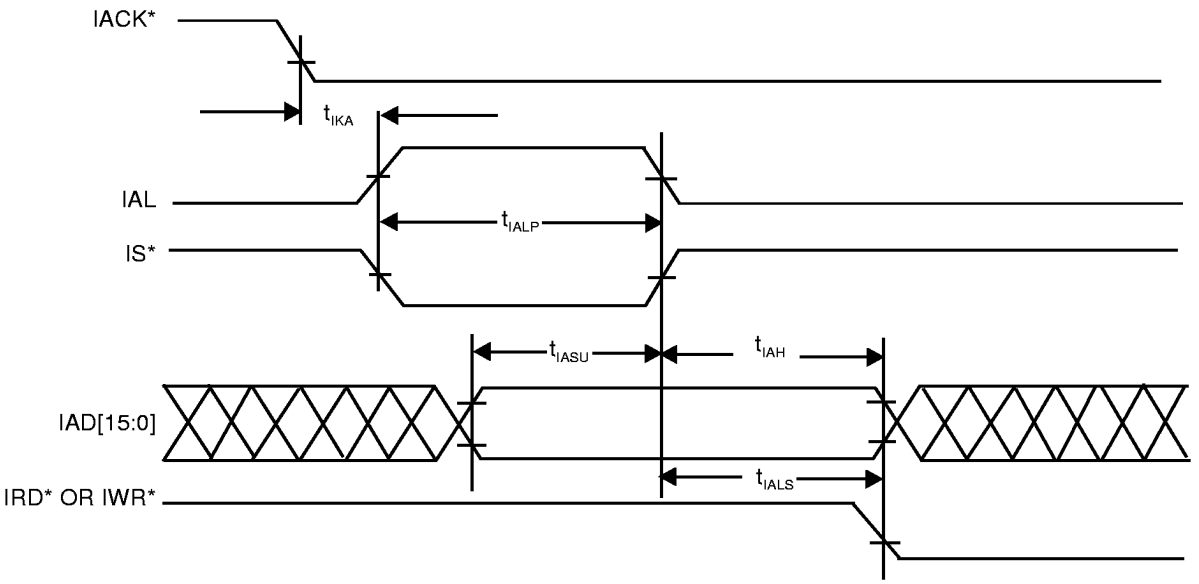
Symbol	Parameter	Min	Max	Units
t_{CCH}	XTALI high to SCLK high		15	ns
t_{CP}	XTALI clock period	55		ns
t_{SCH}	Serial clock high pulse width	20		ns
t_{SCL}	Serial clock low pulse width	20		ns
t_{SCP}	Serial clock cycle period	55		ns
t_{RD}	RFS[1:0]/TFS[1:0] delay time		13	ns
t_{RDH}	Receive data hold time	7		ns
t_{RDS}	Receive data setup time	2		ns
t_{RH}	RFS[1:0]/TFS[1:0] hold time	3		ns
t_{TDD}	Transmit data disable	3		ns
t_{TDE}	Transmit data enable		13	ns
t_{TDH}	Transmit data hold	3		ns
t_{TDV}	Transmit data valid		13	ns

Figure 8 Serial Port Timing Diagram



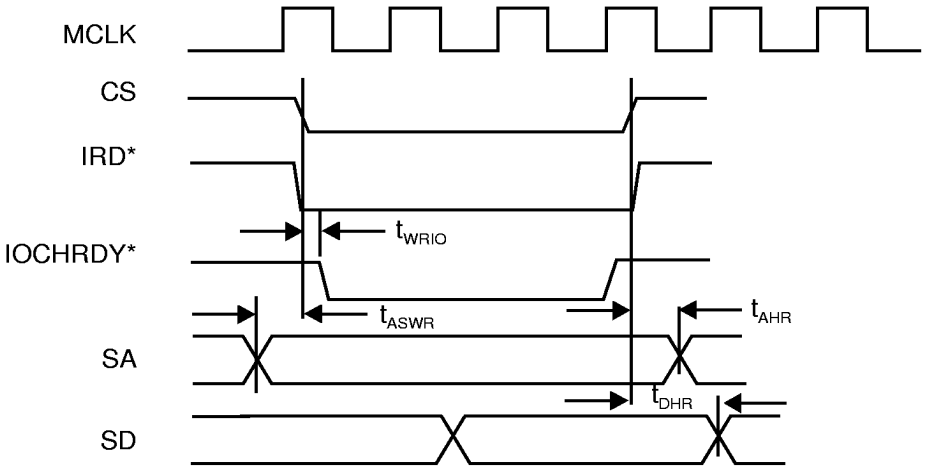
Symbol	Parameter	Min	Max	Units
t_{FOD}	Flag output data delay		15	ns
t_{FOH}	Flag output data hold time	3		ns
t_{IRQH}	IRQ hold time	3		ns
t_{IRQS}	IRQ setup time	5		ns

Figure 9 IRQ, Flag, and GPI/O Pin Timing Diagram



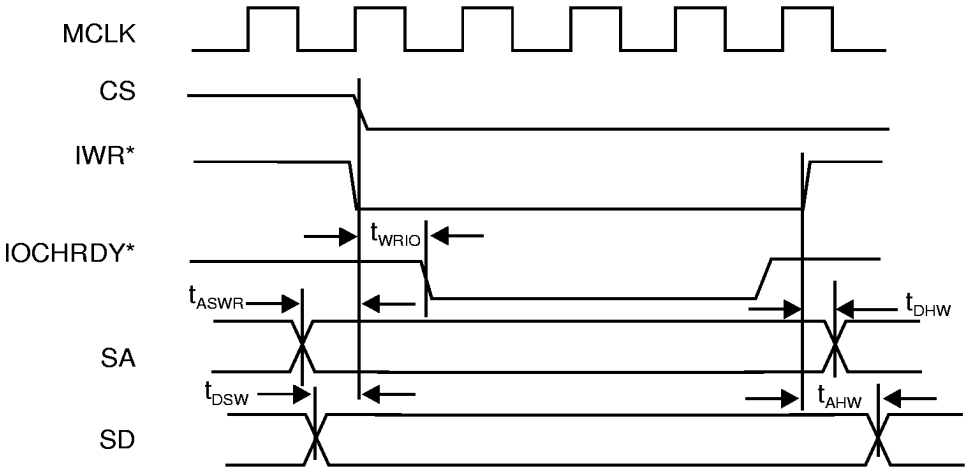
Symbol	Parameter	Min	Max	Units
t_{IALP}	Duration of Address Latch	10		ns
t_{IASU}	IAD15-0 Address Setup before Address Latch End	5		ns
t_{IAH}	IAD15-0 Address Hold after Address Latch End	3		ns
t_{IKA}	IACK* low before start of Address Latch	5		ns
t_{IALS}	Start of Write or Read after Address Latch End	5		ns

Figure 10 IDMA Address Latch



Symbol	Parameter	Min	Typ	Max	Units
t_{WRIO}	IWR*, IRD* to IOCHRDY*			8	ns
t_{ASWR}	Address setup to IWR*, IRD*	4			ns
t_{AHR}	Address hold from rising edge of IRD* (minimum read cycle = 4.5 x (int DSP CLK) + 1 MCLK)	0			ns
t_{DHR}	Data hold from rising edge of IRD* (minimum read cycle = 4.5 x (int DSP CLK) + 1 MCLK)	2			ns

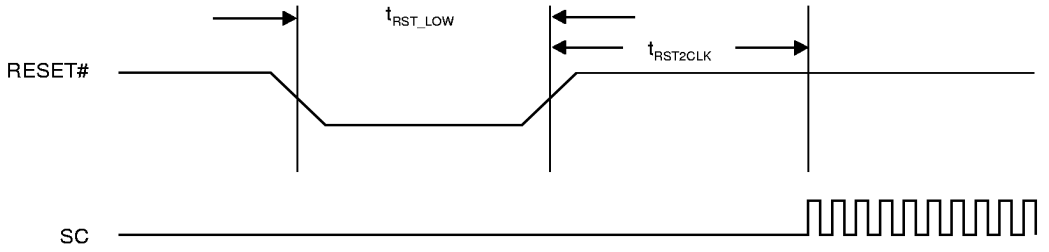
Figure 11 ISA Bus Read Cycle



Symbol	Parameter	Min	Typ	Max	Units
t_{WRIO}	IWR*, IRD* to IOCHRDY*			8	ns
t_{ASWR}	Address setup to IWR*, IRD*	4			ns
t_{DSW}	Data setup to IWR*	0			ns
t_{AHW}	Address hold from rising edge of IWR* (minimum write cycle = 2.5 x (int DSP CLK) + 1 MCLK)	2			ns
t_{DHW}	Data hold from rising edge of IWR* (minimum write cycle = 2.5 x (int DSP CLK) + 1 MCLK)	2			ns

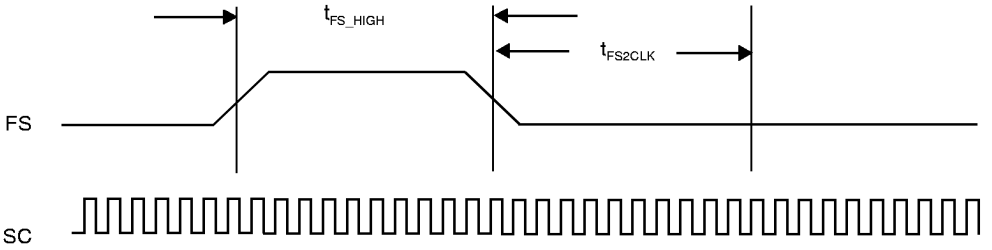
Figure 12 ISA Bus Write Cycle

ES2818/ES2819 AFE AC TIMING DIAGRAMS/CHARACTERISTICS



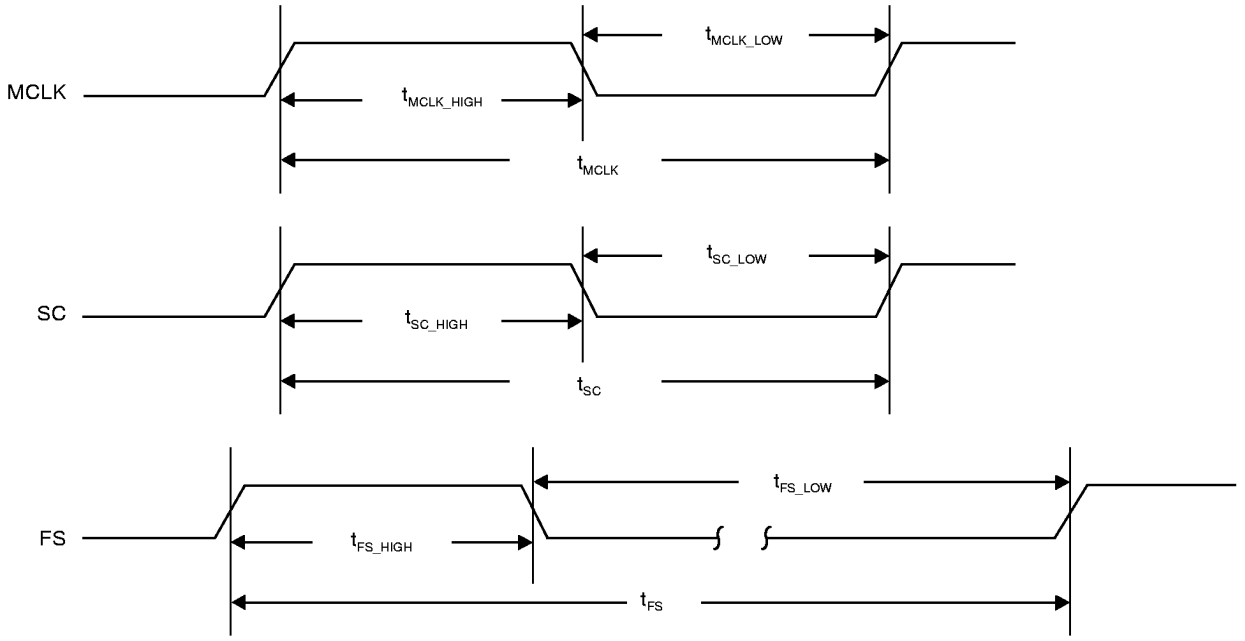
Symbol	Parameter	Min	Typ	Max	Units
t_{RST_LOW}	RESET# active-low pulse width	0.5			µs
$t_{RST2CLK}$	RESET# inactive to SC start-up delay	2.0			µs

Figure 13 Cold Reset



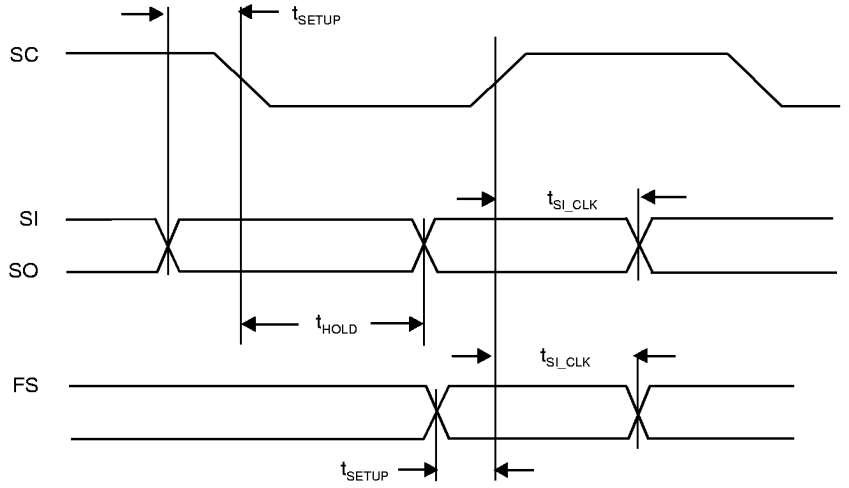
Symbol	Parameter	Min	Typ	Max	Units
t_{FS_HIGH}	FS active-high pulse width		1.3		µS
t_{FS2CLK}	FS inactive to SC start-up delay	162.8			nS

Figure 14 Warm Reset



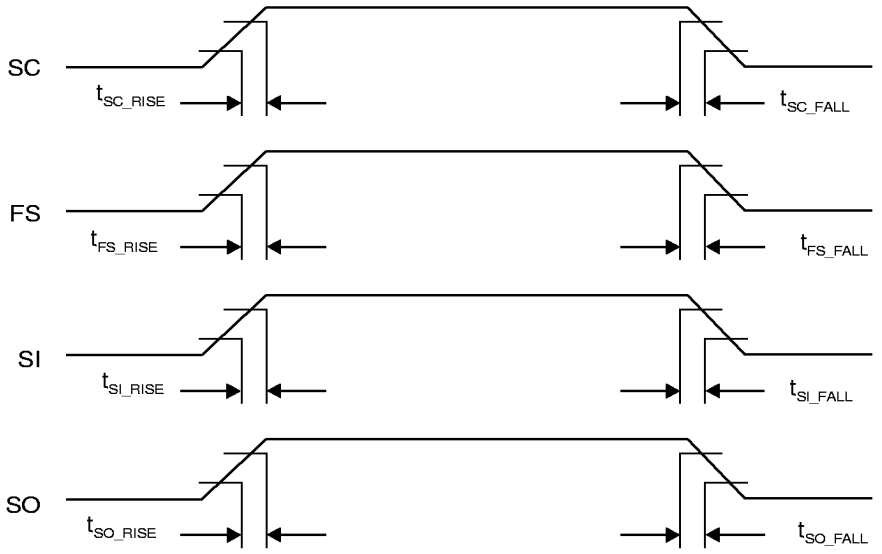
Symbol	Parameter	Min	Typ	Max	Units
	MCLK frequency		56.488		MHz
t_{MCLK}	MCLK period		17.7		ns
t_{MCLK_HIGH}	MCLK high pulse width		8.5		ns
t_{MCLK_LOW}	MCLK low pulse width		8.4		ns
	SC frequency	1.008			MHz
t_{SC}	SCLK period			992	ns
t_{SC_HIGH}	SC high pulse width			490	ns
t_{SC_LOW}	SC low pulse width			490	ns
	FS frequency	7.2			KHz
t_{FS}	FS period	62.5		139	ms
t_{FS_HIGH}	FS high pulse width			0.99	ms
t_{FS_LOW}	FS low pulse width			138	ms

Figure 15 Clocks



Symbol	Parameter	Min	Typ	Max	Units
t_{SETUP}	Setup to falling edge of SC	1.3			ns
t_{HOLD}	Hold from falling edge of SC	3.0			ns
t_{SI_CLK}	Valid delay from FS to SC rising edge	4		8	ns
t_{SI_CLK}	Valid delay from SI to SC rising edge	4		8	ns

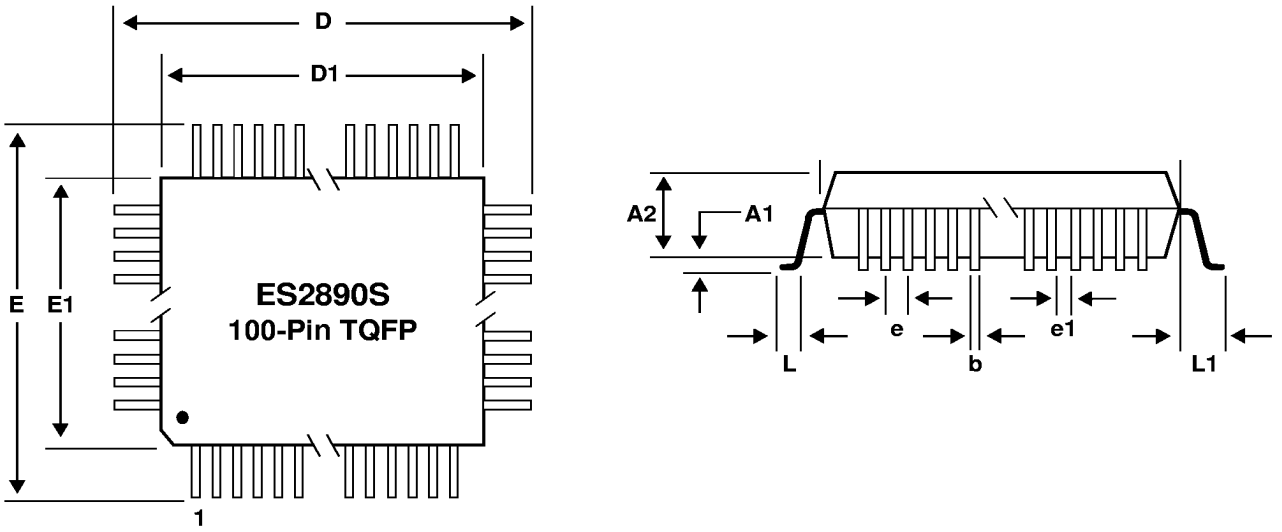
Figure 16 Data Setup and Hold



Symbol	Parameter	Min	Typ	Max	Units
t_{SC_RISE}	SC rise time	2		6	ns
t_{SC_FALL}	SC fall time	2		6	ns
t_{FS_RISE}	FS rise time	2		6	ns
t_{FS_FALL}	FS fall time	2		6	ns
t_{SI_RISE}	SI rise time	2		6	ns
t_{SI_FALL}	SI fall time	2		6	ns
t_{SO_RISE}	SO rise time	2		6	ns
t_{SO_FALL}	SO fall time	2		6	ns

Figure 17 Signal Rise and Fall Times

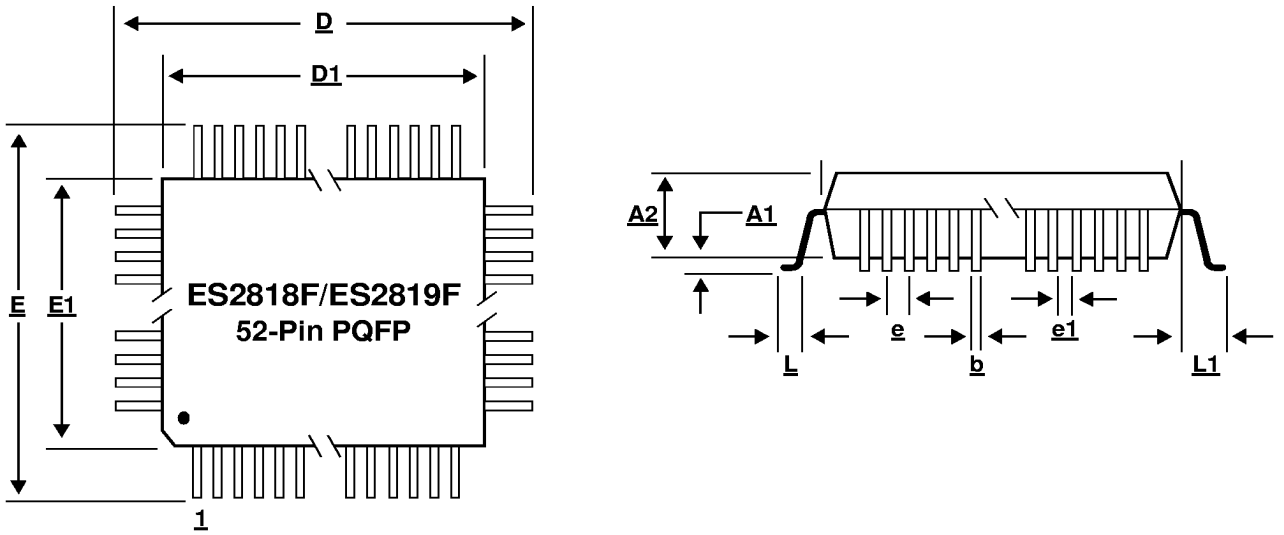
ES2890S MECHANICAL DIMENSIONS



Symbol	Description	Millimeters		
		Min	Nom	Max
D	Lead to lead, X-axis	15.75	16.00	16.25
D1	Package's outside, X-axis	13.90	14.00	14.10
E	Lead to lead, Y-axis	15.75	16.00	16.25
E1	Package's outside, Y-axis	13.90	14.00	14.10
A1	Board standoff	0.05	0.10	0.15
A2	Package thickness	1.35	1.40	1.45
b	Lead width	0.17	0.22	0.27
e	Lead pitch	-	0.50	-
e1	Lead gap	0.24	-	-
L	Foot length	0.45	0.60	0.75
L1	Lead length	0.93	1.00	1.07
-	Foot angle	0°		7°
-	Coplanarity	-	-	0.102
-	Leads in X-axis	-	25	-
-	Leads in Y-axis	-	25	-
-	Total leads	-	100	-
-	Package type	-	TQFP	-

Figure 18 ES2890S DSP Mechanical Dimensions

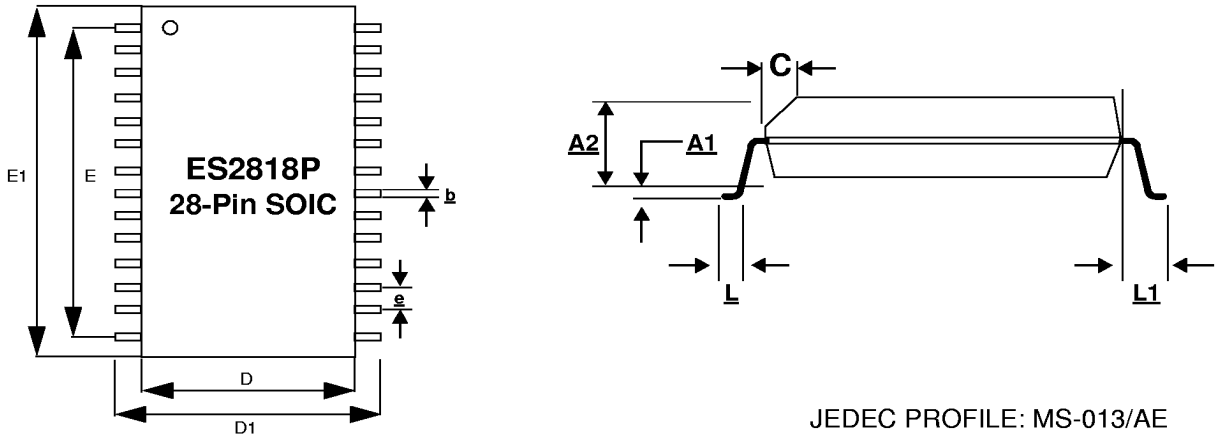
ES2818F/ES2819F MECHANICAL DIMENSIONS / 52-PIN PQFP



Symbol	Description	Millimeters		
		Min	Nom	Max
D	Lead to lead, X-axis	12.95	13.20	13.45
D1	Package's outside, X-axis	9.90	10.00	10.10
E	Lead to lead, Y-axis	12.95	13.20	13.45
E1	Package's outside, Y-axis	9.90	10.00	10.10
A1	Board standoff	0.10	0.25	0.35
A2	Package thickness	1.90	2.00	2.20
b	Lead width	0.20	0.30	0.40
e	Lead pitch	-	0.65	-
e1	Lead gap	0.24	-	-
L	Foot length	0.65	0.80	0.95
L1	Lead length	1.52	1.60	1.68
-	Foot angle	0°		7°
-	Coplanarity	-	-	0.102
-	Leads in X-axis	-	13	-
-	Leads in Y-axis	-	13	-
-	Total leads	-	52	-
-	Package type	-	PQFP	-

Figure 19 ES2818F/ES2819F Modem AFE Mechanical Dimensions / 52-pin PQFP

ES2818P MECHANICAL DIMENSIONS / 28-PIN SOIC



JEDEC PROFILE: MS-013/AE

Symbol	Description	Millimeters		
		Min	Nom	Max
D	Lead to lead, X-axis	7.08	7.44	7.82
D1	Package's outside, X-axis	10.24	10.36	10.48
E	Lead to lead, Y-axis	16.85	16.91	16.97
E1	Package's outside, Y-axis	17.45	17.83	18.21
A1	Board standoff	0.10	0.25	0.35
A2	Package thickness	-	2.34	-
b	Lead width	0.30	0.40	0.50
e	Lead pitch	-	1.27	-
L	Foot length		0.76	
L1	Lead length	2.87	2.92	2.97
-	Foot angle	-	5°	-
-	Chamfer angle		45°	
C	Chamfer distance		0.635	
-	Leads per single Y-axis	-	14	-
-	Total leads	-	28	-
-	Package type	-	SOIC	-

Figure 20 ES2818P Modem AFE Mechanical Dimensions / 28-pin SOIC

APPENDIX A: SCHEMATIC EXAMPLES

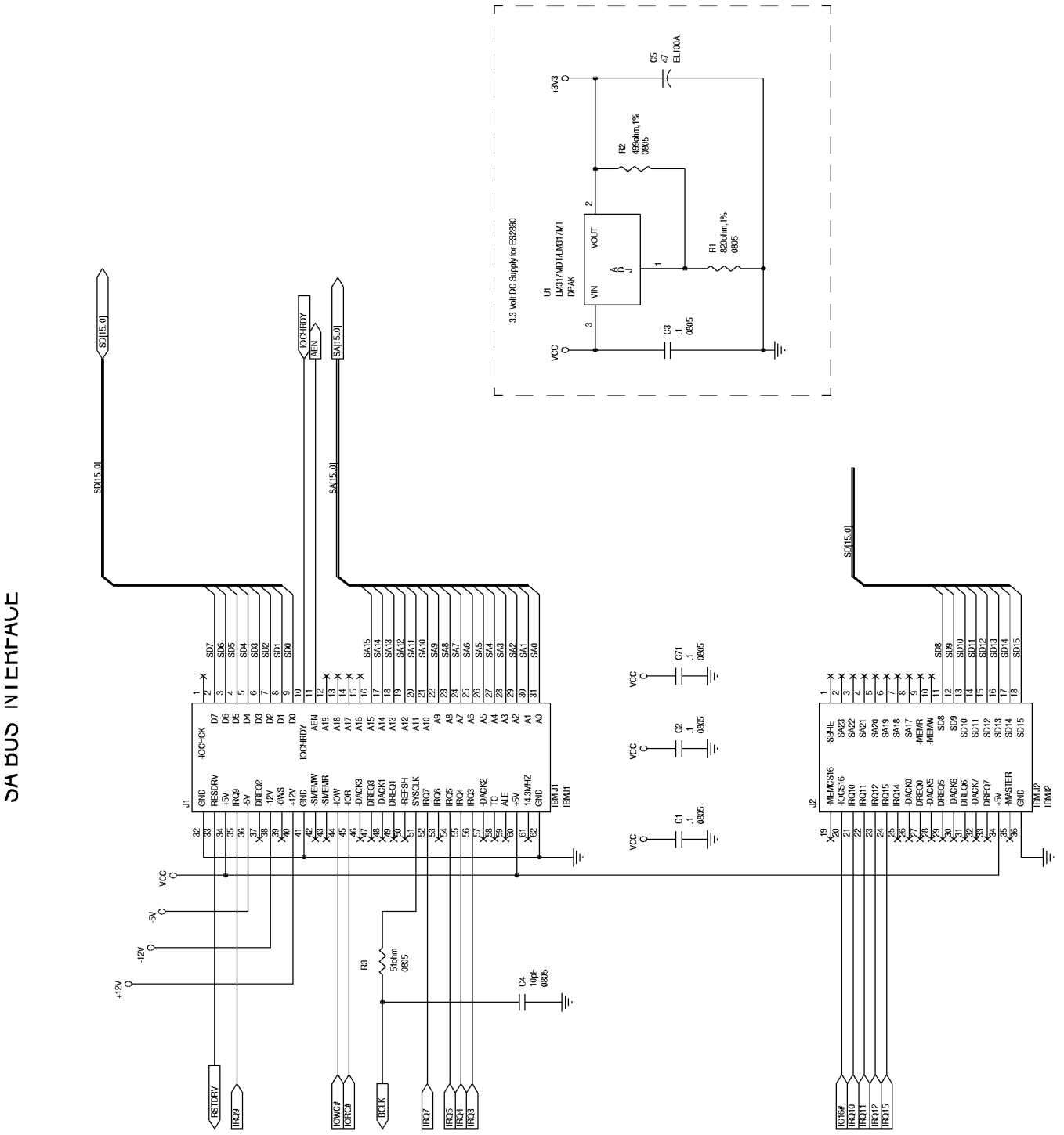


Figure 21 ISA Bus Interface Schematic

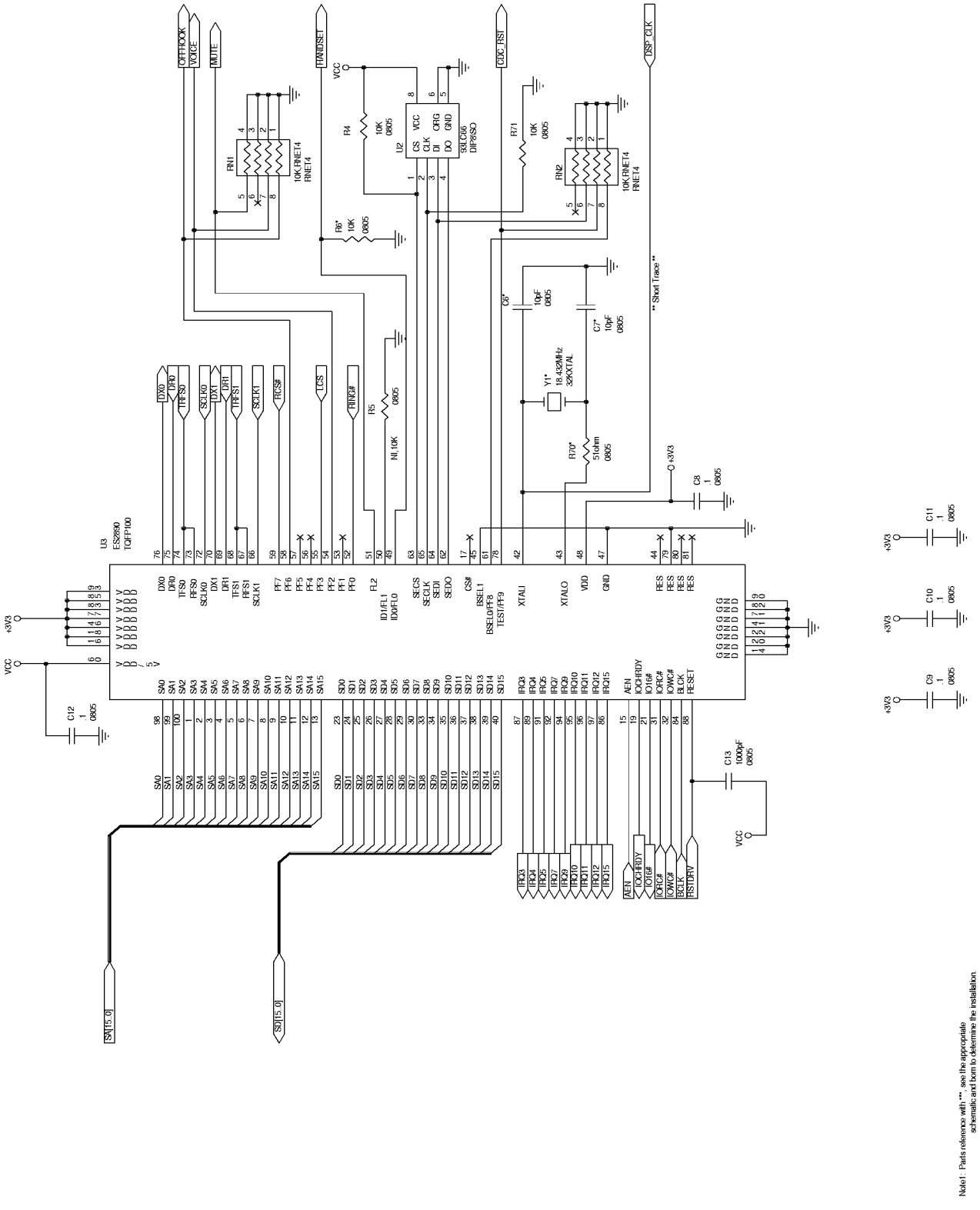


Figure 22 ES2890S Modem DSP Interface

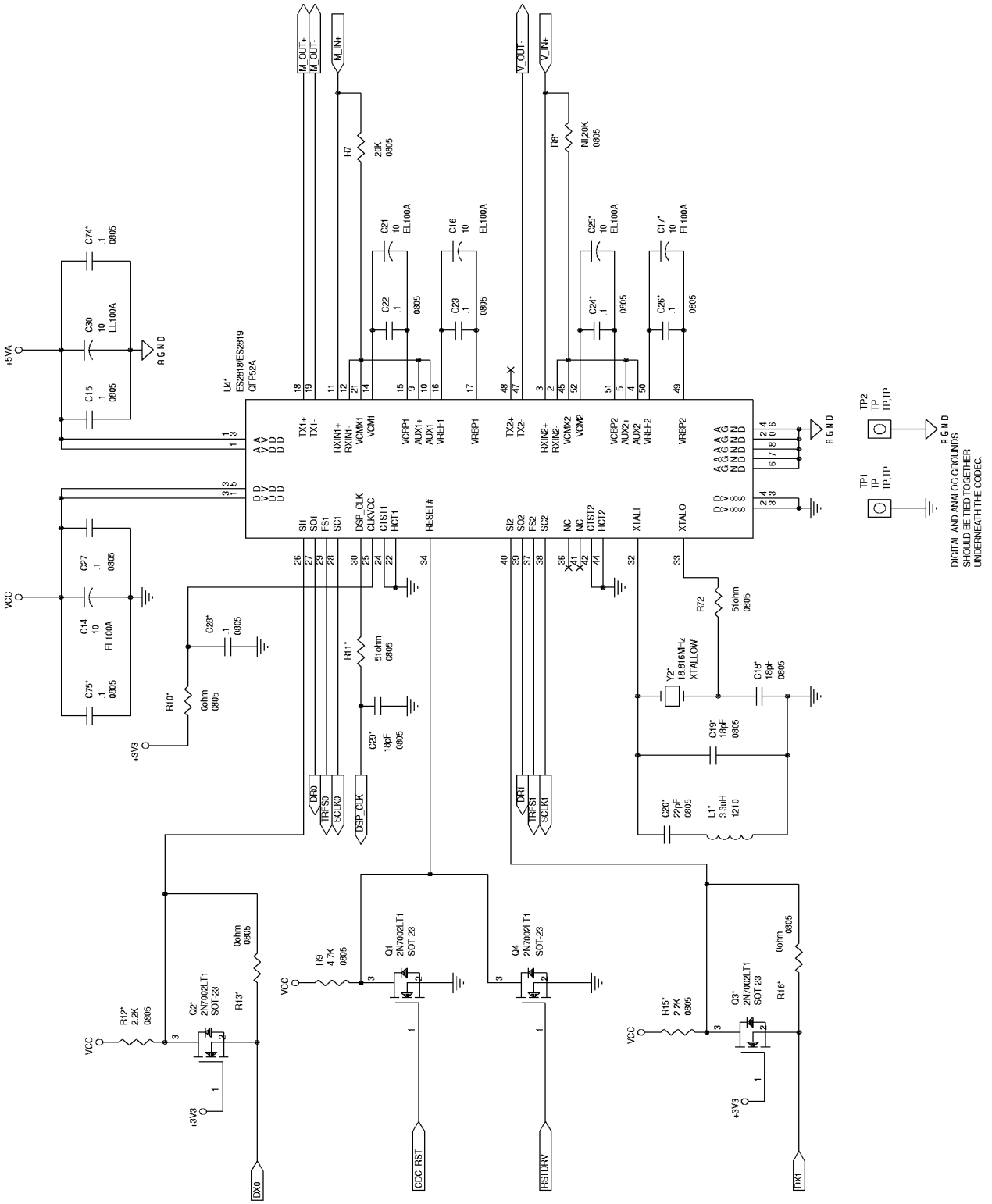


Figure 23 Modem AFE Interface

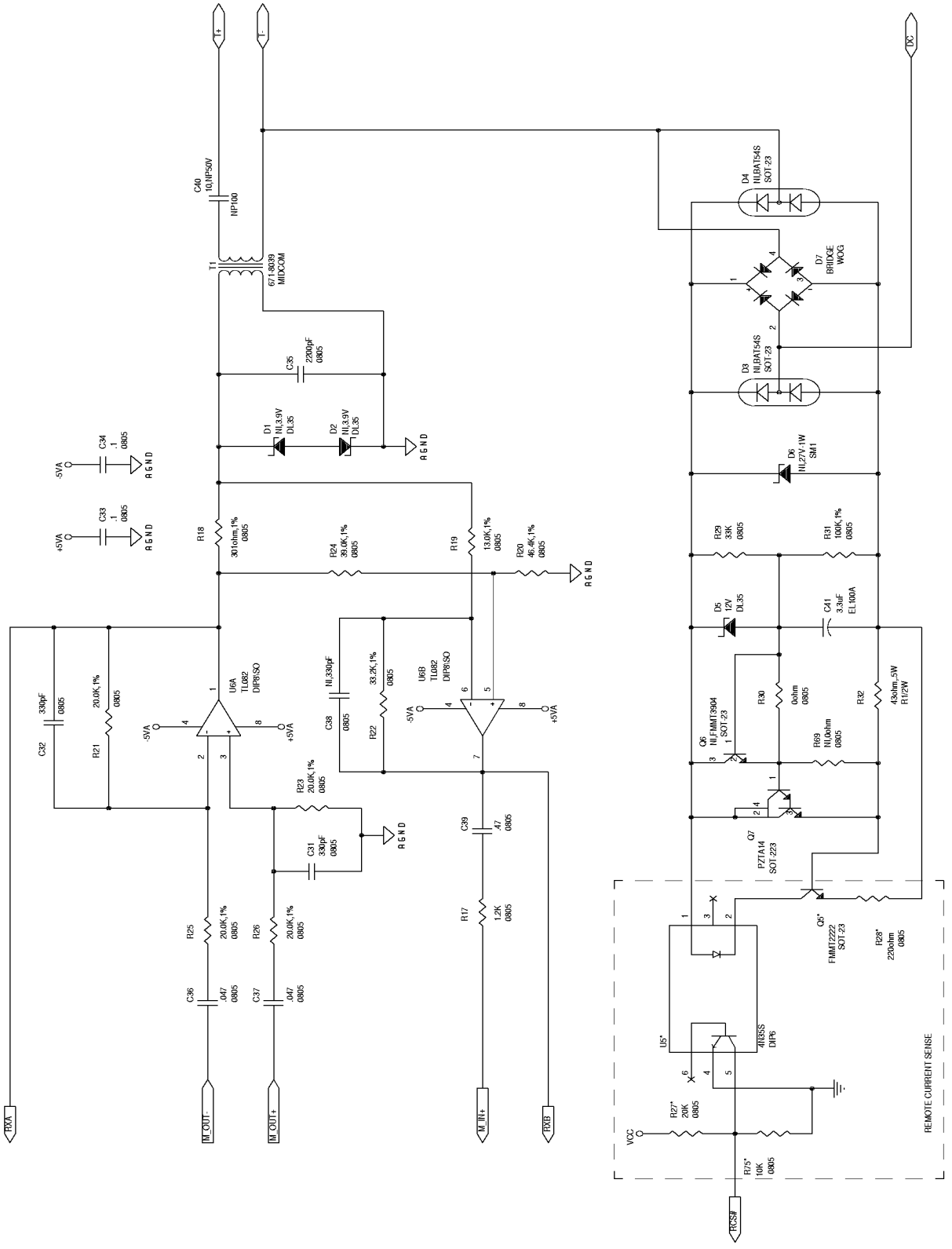


Figure 24 Modem Transhybrid/Coil Holder Section

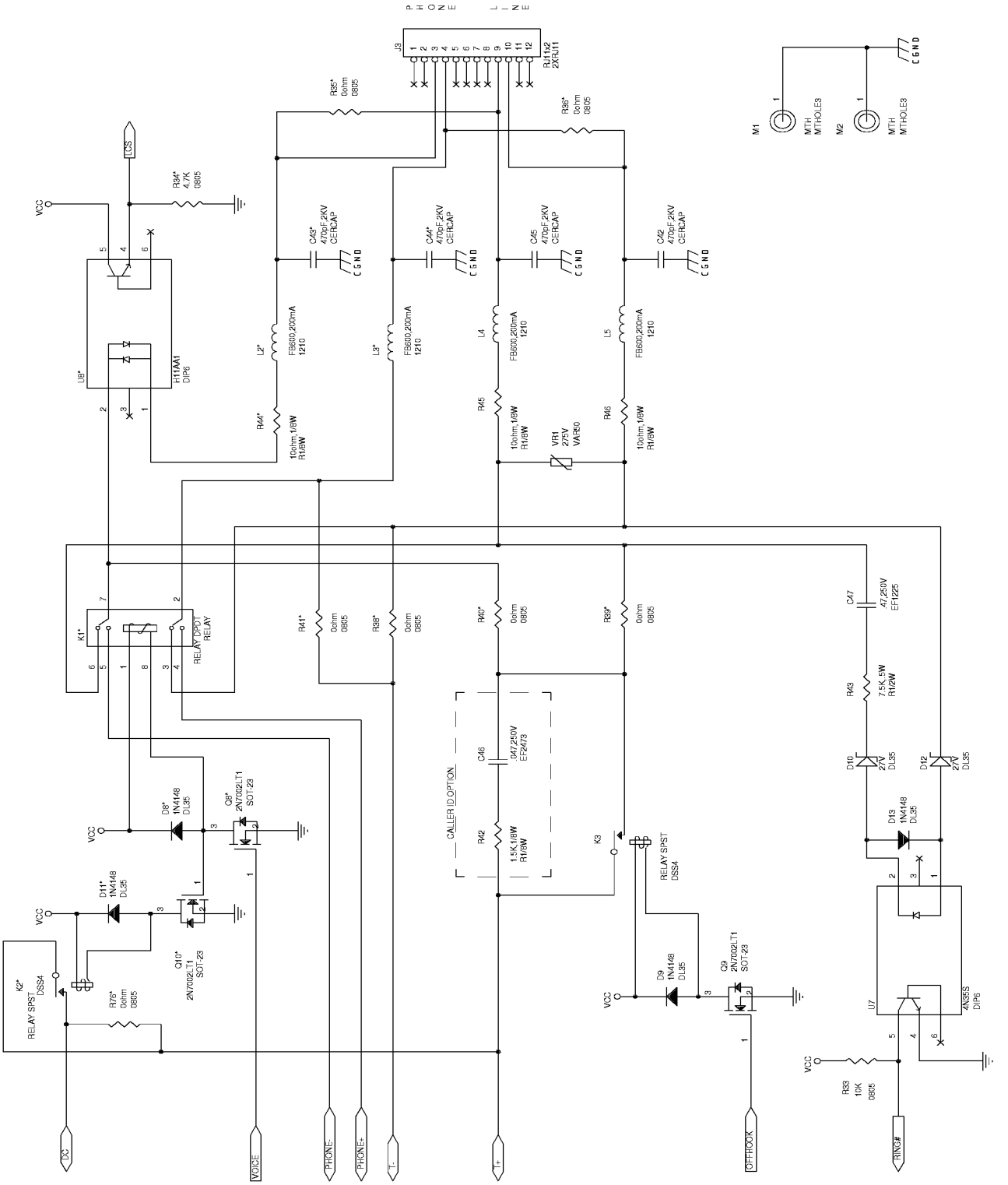


Figure 25 DAA/Phone Line Interface

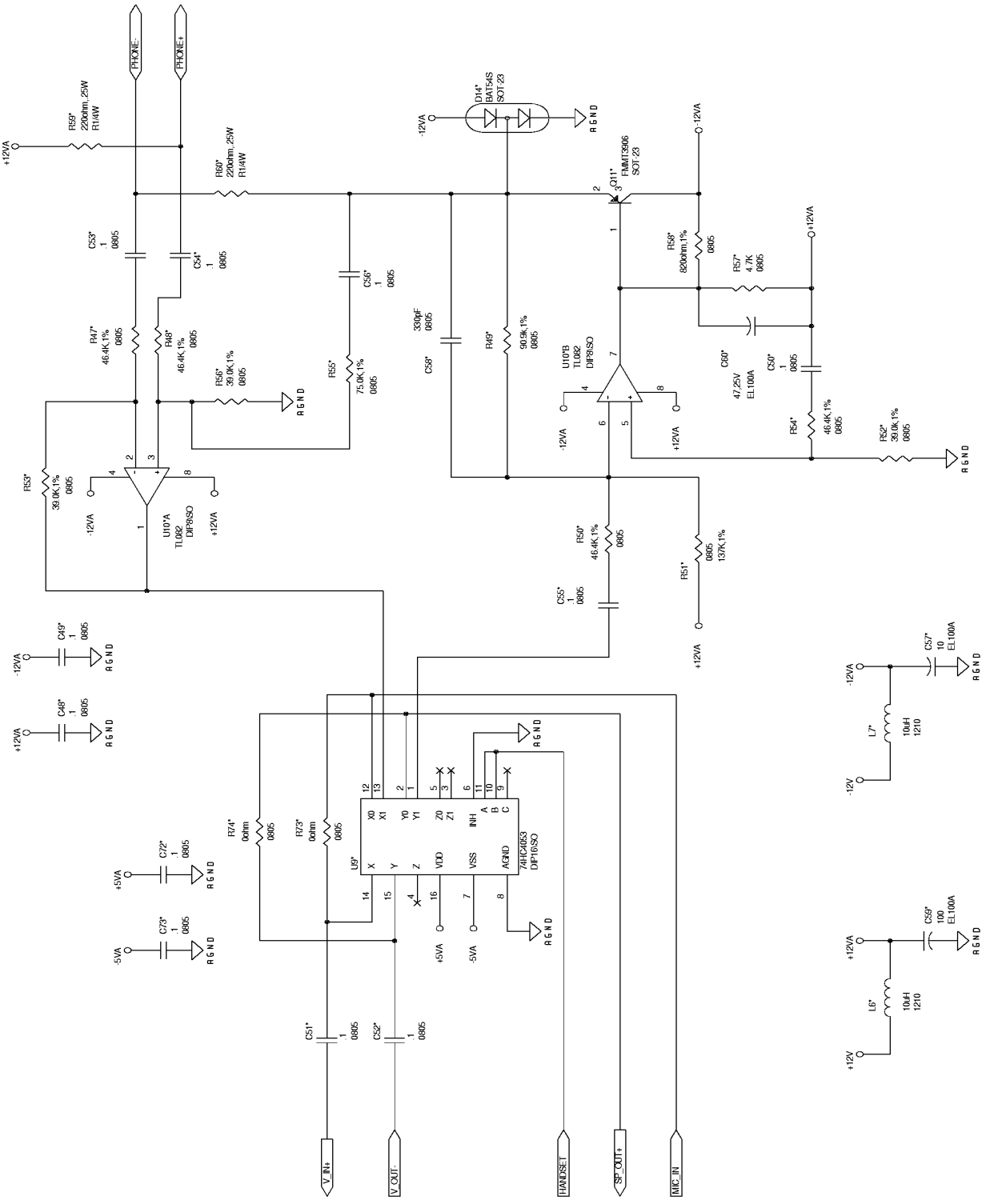


Figure 26 Telephone Answering Machine Schematic

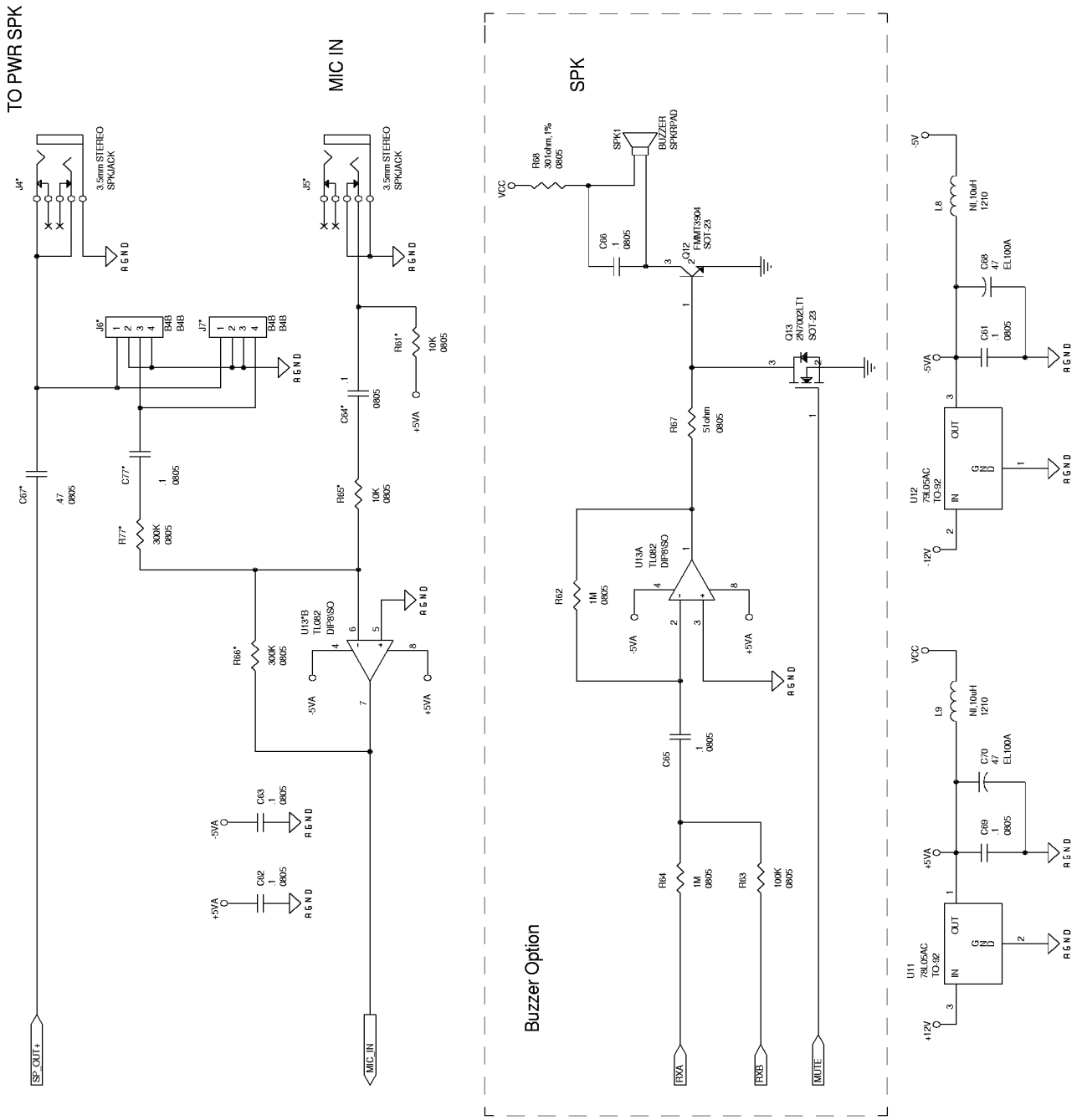


Figure 27 Full Duplex Speakerphone Schematic

APPENDIX B: BILL OF MATERIALS

ES56-I DATA/FAX BOM

Item	Quantity	Reference	Part	Description
1	1	C4	10pF	Cap,10pF,5%,50V,NPO,0805
2	3	C18,C19,C29	18pF	Cap,18pF,5%,50V,NPO,0805
3	2	C31,C32	330pF	Cap,330pF,10%,50V,Ceramic,0805
4	1	C13	1000pF	Cap,1000pF,10%,50V,Ceramic,0805
5	1	C35	2200pF	Cap,2200pF,10%,50V,Ceramic,0805
6	2	C36,C37	0.047	Cap,0.047uF,10%,50V,Ceramic,0805
7	22	C1,C2,C3,C8,C9, C10,C11, C12,C15,C22,C23,C27,C28, C33,C34,C61,C62,C63,C65, C66,C69,C71	0.1	Cap,0.1uF,-20/+80%,50V,Ceramic,0805
8	1	C39	0.47	Cap,0.47uF,-20/+80%,50V,Ceramic,0805
9	1	C46	.047,250V	Cap,Mploy,0.047uF,20%,250V,Ra-0.3sp
10	1	C47	.47,250V	Cap,Mploy,0.47uF,20%,250V,Ra-0.6sp
11	1	C41	3.3uF	Cap,Elec,3.3uF,20%,50V,Ra-0.1sp
12	1	C40	10,NP50V	Cap,NP Elec,10uF,20%,50V,Ra-0.1sp
13	4	C14,C16,C21,C30	10	Cap,Elec,10uF,20%,16V,Ra-0.1sp
14	3	C5,C68,C70	47	Cap,Elec,47uF,20%,16V,Ra-0.1sp
15	2	C42,C45	470pF,2KV	Cap,Cer,470pF,20%,2000V,Ra-0.2sp
16	1	D5	12V	Diode,Zener,12V,5%,SOD-80
17	2	D10,D12	27V	Diode,Zener,27V,5%,SOD-80
18	2	D9,D13	1N4148	Diode,Signal,100V,SOD-80
19	1	D7	BRIDGE	Diode Rectifier Bridge,1A,GI-W04G
20	1	SPK1	BUZZER	Speaker,buzzer,.25 sp,MG Elec.,SBT1606,T/H
21	1	J3	RJ11x2	Dual RJ-11 phone Jack,Millennium,AJ-026-16-2-C-3
22	1	K3	RELAY SPST	Relay,SPST,Form 1A,Z660-ND,PC Clare,DSS41A05
23	2	L4,L5	FB600,200mA	Ferrite Bead,SM,200mA,1206,EXC-ELSA35,Pan
24	1	Q12	FMMT3904	Transistor,NPN,FMMT3904,SOT-23
25	1	Q7	PZTA14	Transistor,NPN Darlington,PZTA14,SOT-223
26	4	Q1,Q4,Q9,Q13	2N7002LT1	FET,N-Channel 2N7002LT1,SOT-23
27	8	R10,R13,R30,R35,R36,R38, R39,R76	0ohm	Resistor,SM,0 Ohm,1/10W,0805
28	4	R3,R11,R67,R72	51ohm	Resistor,SM,51 Ohm,5%,1/10W,0805
29	1	R17	1.2K	Resistor,SM,1.2K,5%,1/10W,0805
30	1	R9	4.7K	Resistor,SM,4.7K,5%,1/10W,0805
31	4	R4,R33,R71,R75	10K	Resistor,SM,10K,5%,1/10W,0805
32	1	R7	20K	Resistor,SM,20K,5%,1/10W,0805
33	1	R29	33K	Resistor,SM,33K,5%,1/10W,0805
34	1	R63	100K	Resistor,SM,100K,5%,1/10W,0805
35	2	R62,R64	1M	Resistor,SM,1M,5%,1/10W,0805
36	2	R18,R68	301ohm,1%	Resistor,SM,301 Ohm,1%,1/10W,0805
37	1	R2	499ohm,1%	Resistor,SM,499 Ohm,1%,1/10W,0805
38	1	R1	820ohm,1%	Resistor,SM,820 Ohm,1%,1/10W,0805
39	1	R19	13.0K,1%	Resistor,SM,13.0K,1%,1/10W,0805
40	4	R21,R23,R25,R26	20.0K,1%	Resistor,SM,20.0K,1%,1/10W,0805

Item	Quantity	Reference	Part	Description
41	1	R22	33.2K,1%	Resistor,SM,33.2K,1%,1/10W,0805
42	1	R24	39.0K,1%	Resistor,SM,39.0K,1%,1/10W,0805
43	1	R20	46.4K,1%	Resistor,SM,46.4K,1%,1/10W,0805
44	1	R31	100K,1%	Resistor,SM,100K,1%,1/10W,0805
45	1	R42	1.5K,1/8W	Resistor,SM,1.5K,5%,1/8W,1206
46	2	R45,R46	10ohm,1/8W	Resistor,SM,10 Ohm,5%,1/8W,1206
47	1	R32	43ohm,.5W	Resistor,Axial,43 Ohm,5%,1/2W
48	1	R43	7.5K,.5W	Resistor,Axial,7.5K, 5%,1/2W
49	2	RN1,RN2	10K,RNET4	Resistor Nerwork,SM,4-pack,10K,5%,1/16W
50	1	T1	671-8039	Transformer,Modem,1:1,600ohm,Midcom 671-8039
51	1	U1	LM317MDT/LM317MT	IC,Regulator,LM317MDT/MT,DPAK/TO-220
52	1	U12	79L05AC	IC,-5 Volt Regulator,79L05AC,TO-92
53	1	U11	78L05AC	IC,+5 Volt Regulator,78L05AC,TO-92
54	2	U6,U13	TL082	IC,SM,Dual JFET OP Amp., TL082, SOP-8
55	1	U2	93LC66	IC,SM,EEPROM,Microchip,93LC66,Atmel,93C66-10SC-2.7,SO-8
56	1	U3	ES2890	IC,SM,ESS EDSP ES2890,TQFP-100
57	1	U4	ES2818	IC,SM,ESS AFE CODECs,ES2818,TQFP-52
58	1	U7	4N35S	IC,Optocoupler,4N35,DIP-6
59	1	VR1	275V	Varistor, 275V 5mm,Harris V275LA4
60	1	Y2	18.816MHz	Crystal,18.816MHz,Fundamental,HC-49S
61	1	BKT	Bractet	Reat Panel, Purcell Bracket, Inc., PE02-ESS2, Rev.2
62	2	SCR	Screw	Bracket Screw 4-40,.3/16"

ES56T-I DATA/FAX/TAM BOM

Item	Quantity	Reference	Part	Description
1	1	C4	10pF	Cap,10pF,5%,50V,NPO,0805
2	3	C18,C19,C29	18pF	Cap,18pF,5%,50V,NPO,0805
3	2	C31,C32	330pF	Cap,330pF,10%,50V,X7R,0805
4	1	C13	1000pF	Cap,1000pF,10%,50V,Creamic,0805
5	1	C35	2200pF	Cap,2200pF,10%,50V,Ceramic,0805
6	2	C36,C37	0.047	Cap,0.047uF,10%,50V,Ceramic,0805
7	22	C1,C2,C3,C8,C9,C10,C11, C12,C15,C22,C23,C27,C28, C33,C34,C61,C62,C63,C65, C66,C69,C71	0.1	Cap,0.1uF,-20/+80%,50V,Ceramic,0805
8	1	C39	0.47	Cap,0.47uF,-20/+80%,50V,Ceramic,0805
9	1	C46	.047,250V	Cap,Mploy,0.047uF,20%,250V,Ra-0.3sp
10	1	C47	.47,250V	Cap,Mploy,0.47uF,20%,250V,Ra-0.6sp
11	1	C41	3.3uF	Cap,Elec,3.3uF,20%,50V,Ra-0.1sp
12	1	C40	10,NP50V	Cap,NP Elec,10uF,20%,50V,Ra-0.1sp
13	4	C14,C16,C21,C30	10	Cap,Elec,10uF,20%,16V,Ra-0.1sp
14	3	C5,C68,C70	47	Cap,Elec,47uF,20%,16V,Ra-0.1sp
15	1	C60	47,25V	Cap,Elec,47uF,20%,25V,Ra-0.1sp
16	4	C42,C43,C44,C45	470pF,2KV	Cap,Cer,470pF,20%,2000V,Ra-0.2sp
17	1	D5	12V	Diode,Zener,12V,5%,SOD-80
18	2	D10,D12	27V	Diode,Zener,27V,5%,SOD-80
19	1	D14	BAT54S	Diode,Dual Rectifier,200mA,SOT-23
20	4	D8,D9,D11,D13	1N4148	Diode,Signal,100V,SOD-80
21	1	D7	BRIDGE	Diode Rectifier Bridge,1A,GI-W04G
22	1	SPK1	BUZZER	Speaker,buzzer,.25 sp,MG Elec.,SBT1606,T/H
23	1	J3	RJ11x2	Dual RJ-11 phone Jack,Millennium,AJ-026-16-2-C-3
24	1	K1	RELAY DPDT	Relay,DPDT,Form 2C,Omron,G5V-2-DC5
25	2	K3,K2	RELAY SPST	Relay,SPST,Form 1A,Z660-ND,PC Clare,DSS41A05
26	4	L2,L3,L4,L5	FB600,200mA	Ferrite Bead,SM,200mA,1206,EXC-ELSA35,Pan
27	2	L6,L7	10uH	Inductor,10uH,SM,1210,667-210,Mini-reel+G38
28	1	Q12	FMMT3904	Transistor,NPN,FMMT3904,SOT-23
29	1	Q11	FMMT3906	Transistor,PNP,FMMT3906,SOT-23
30	1	Q7	PZTA14	Transistor,NPN Darlington,PZTA14,SOT-223
31	6	Q1,Q4,Q8,Q9,Q10,Q13	2N7002LT1	FET,N-Channel 2N7002LT1,SOT-23
32	5	R10,R13,R30,R40,R41	0ohm	Resistor,SM,0 Ohm,1/10W,0805
33	4	R3,R11,R67,R72	51ohm	Resistor,SM,51 Ohm,5%,1/10W,0805
34	1	R17	1.2K	Resistor,SM,1.2K,5%,1/10W,0805
35	3	R9,R34,R57	4.7K	Resistor,SM,4.7K,5%,1/10W,0805
36	4	R4,R33,R71,R75	10K	Resistor,SM,10K,5%,1/10W,0805
37	1	R7	20K	Resistor,SM,20K,5%,1/10W,0805
38	1	R29	33K	Resistor,SM,33K,5%,1/10W,0805
39	1	R63	100K	Resistor,SM,100K,5%,1/10W,0805
40	2	R62,R64	1M	Resistor,SM,1M,5%,1/10W,0805
41	2	R18,R68	301ohm,1%	Resistor,SM,301 Ohm,1%,1/10W,0805
42	1	R2	499ohm,1%	Resistor,SM,499 Ohm,1%,1/10W,0805
43	2	R1,R58	820ohm,1%	Resistor,SM,820 Ohm,1%,1/10W,0805
44	1	R19	13.0K,1%	Resistor,SM,13.0K,1%,1/10W,0805
45	4	R21,R23,R25,R26	20.0K,1%	Resistor,SM,20.0K,1%,1/10W,0805

Item	Quantity	Reference	Part	Description
46	1	R22	33.2K,1%	Resistor,SM,33.2K,1%,1/10W,0805
47	1	R24	39.0K,1%	Resistor,SM,39.0K,1%,1/10W,0805
48	1	R20	46.4K,1%	Resistor,SM,46.4K,1%,1/10W,0805
49	1	R31	100K,1%	Resistor,SM,100K,1%,1/10W,0805
50	1	R42	1.5K,1/8W	Resistor,SM,1.5K,5%,1/8W,1206
51	3	R44,R45,R46	10ohm,1/8W	Resistor,SM,10 Ohm,5%,1/8W,1206
52	2	R59,R60	220ohm,.25W	Resistor,Axial,220 Ohm,5%,1/4W
53	1	R32	43ohm,.5W	Resistor,Axial,43 Ohm,5%,1/2W
54	1	R43	7.5K,.5W	Resistor,Axial,7.5K, 5%,1/2W
55	2	RN1,RN2	10K,RNET4	Resistor Nerwork,SM,4-pack,10K,5%,1/16W,CA Elec.,TSMB08-103J
56	1	T1	671-8039	Transformer,Modem,1:1,600ohm,Midcom 671-8039
57	1	U1	LM317MDT/ LM317MT	IC,Regulator,LM317MDT/MT,DPAK/TO-220
58	1	U12	79L05AC	IC,-5 Volt Regulator,79L05AC,TO-92
59	1	U11	78L05AC	IC,+5 Volt Regulator,78L05AC,TO-92
60	2	U6,U13	TL082	IC,SM,Dual JFET OP Amp., TL082, SOP-8
61	1	U2	93LC66	IC,SM,EEPROM,Microchip,93LC66,Atmel,93C66-10SC-2.7,SO-8
62	1	U3	ES2890	IC,SM,ESS EDSP ES2890,TQFP-100
63	1	U4	ES2818	IC,SM,ESS AFE CODECs,ES2818,TQFP-52
64	1	U7	4N35S	IC,Optocoupler,4N35,DIP-6
65	1	U8	H11AA1	IC,AC-input Solid State Current Sensor,H11AA1,DIP-6
66	1	VR1	275V	Varistor, 275V 5mm,Harris V275LA4
67	1	Y2	18.816MHz	Crystal,18.816MHz,Fundamental,HC-49S
68	1	BKT	Bracket	Reat Panel, Purcell Bracket, Inc., PE02-ESS2, Rev.2
69	2	SCR	Screw	Bracket Screw 4-40,.3/16"

ES56V-I DATA/FAX/SPEAKERPHONE BOM

Item	Quantity	Reference	Part	Description
1	5	C4,C6,C7,C18, C19	10pF	Cap,10pF,5%,50V,NPO,0805
2	1	C20	22pF	Cap,22pF,5%,50V,NPO,0805
3	3	C31,C32,C58	330pF	Cap,330pF,10%,50V,X7R,0805
4	1	C13	1000pF	Cap,1000pF,10%,50V,Ceramic,0805
5	1	C35	2200pF	Cap,2200pF,10%,50V,Ceramic,0805
6	2	C36,C37	0.047	Cap,0.047uF,10%,50V,Ceramic,0805
7	38	C1,C2,C3,C8,C9, C10,C11,C12, C15,C22,C23, C24,C26,C27, C33,C34,C48, C49,C50,C51, C52,C53,C54, C55,C56,C61, C62,C63,C64, C65,C66,C69, C71,C72,C73, C74,C75, C77	0.1	Cap,0.1uF,-20/+80%,50V,Ceramic,0805
8	2	C67,C39	0.47	Cap,0.47uF,-20/+80%,50V,Creamic,0805
9	1	C46	.047,250V	Cap,Mploy,0.047uF,20%,250V,Ra-0.3sp
10	1	C47	.47,250V	Cap,Mploy,0.47uF,20%,250V,Ra-0.6sp
11	1	C41	3.3uF	Cap,Elec,3.3uF,20%,50V,Ra-0.1sp
12	1	C40	10,NP50V	Cap,NP Elec,10uF,20%,50V,Ra-0.1sp
13	7	C14,C16,C17,C21,C25,C30, C57	10	Cap,Elec,10uF,20%,16V,Ra-0.1sp
14	3	C5,C68,C70	47	Cap,Elec,47uF,20%,16V,Ra-0.1sp
15	1	C59	100	Cap,Elec,100uF,20%,16V,Ra-0.1sp
16	4	C42,C43,C44,C45	470pF,2KV	Cap,Cer,470pF,20%,2000V,Ra-0.2sp
17	1	D5	12V	Diode,Zener,12V,5%,SOD-80
18	2	D10,D12	27V	Diode,Zener,27V,5%,SOD-80
19	1	D14	BAT54S	Diode,Dual Rectifier,200mA,SOT-23
20	3	D8,D9,D13	1N4148	Diode,Signal,100V,SOD-80
21	1	D7	BRIDGE	Diode Rectifier Bridge,1A,GI-W04G
22	2	J6,J7	B4B	Conn,B4B-PH-K,J.S.T. Mfg. Co. Ltd.
23	2	J4,J5	3.5mm STEREO	Conn,3..5mm Stereo Jack,Flat,Mouser,161-3504
24	1	SPK1	BUZZER	Speaker,buzzer,.25 sp,MG Elec.,SBT1606,T/H
25	1	J3	RJ11x2	Dual RJ-11 phone Jack,Millennium,AJ-026-16-2-C-3
26	1	K1	RELAY DPDT	Relay,DPDT,Form 2C,Omron,G5V-2-DC5
27	1	K3	RELAY SPST	Relay,SPST,Form 1A,Z660-ND,PC Clare,DSS41A05
28	4	L2,L3,L4,L5	FB600,200mA	Ferrite Bead,SM,200mA,1206,EXC-ELSA35,Pan
29	1	L1	3.3uH	Inductor,3.3uH,SM,1210,667/467-133,Mini-reel
30	2	L6,L7	10uH	Inductor,10uH,SM,1210,667-210,Mini-reel
31	1	Q5	FMMT2222	Transistor,NPN,FMMT2222,SOT-23
32	1	Q12	FMMT3904	Transistor,NPN,FMMT3904,SOT-23
33	1	Q11	FMMT3906	Transistor,PNP,FMMT3906,SOT-23
34	1	Q7	PZTA14	Transistor,NPN Darlington,PZTA14,SOT-223
35	7	Q1,Q2,Q3,Q4,Q8,Q9,Q13	2N7002LT1	FET,N-Channel 2N7002LT1,SOT-23

36	4	R30,R38,R39,R76	0ohm	Resistor,SM,0 Ohm,1/10W,0805
37	4	R3,R67,R70,R72	51ohm	Resistor,SM,51 Ohm,5%,1/10W,0805
38	1	R28	220ohm	Resistor,SM,220,5%,1/10W,0805
39	1	R17	1.2K	Resistor,SM,1.2K,5%,1/10W,0805
40	2	R12,R15	2.2K	Resistor,SM,2.2K,5%,1/10W,0805
41	2	R34,R9	4.7K	Resistor,SM,4.7K,5%,1/10W,0805
42	6	R4,R6,R33,R61, R65,R71	10K	Resistor,SM,10K,5%,1/10W,0805
43	3	R7,R8,R27	20K	Resistor,SM,20K,5%,1/10W,0805
44	1	R29	33K	Resistor,SM,33K,5%,1/10W,0805
45	1	R63	100K	Resistor,SM,100K,5%,1/10W,0805
46	2	R66,R77	300K	Resistor,SM,300K,5%,1/10W,0805
47	2	R62,R64	1M	Resistor,SM,1M,5%,1/10W,0805
48	2	R18,R68	301ohm,1%	Resistor,SM,301 Ohm,1%,1/10W,0805
49	1	R2	499ohm,1%	Resistor,SM,499 Ohm,1%,1/10W,0805
50	1	R1	820ohm,1%	Resistor,SM,820 Ohm,1%,1/10W,0805
51	1	R19	13.0K,1%	Resistor,SM,13.0K,1%,1/10W,0805
52	4	R21,R23,R25, R26	20.0K,1%	Resistor,SM,20.0K,1%,1/10W,0805
53	1	R22	33.2K,1%	Resistor,SM,33.2K,1%,1/10W,0805
54	4	R24,R52,R53, R56	39.0K,1%	Resistor,SM,39.0K,1%,1/10W,0805
55	5	R20,R47,R48, R50,R54	46.4K,1%	Resistor,SM,46.4K,1%,1/10W,0805
56	1	R55	75.0K,1%	Resistor,SM,75.0K,1%,1/10W,0805
57	1	R49	90.9k,1%	Resistor,SM,90.9K,1%,1/10W,0805
58	1	R31	100K,1%	Resistor,SM,100K,1%,1/10W,0805
59	1	R51	137K,1%	Resistor,SM,137K,1%,1/10W,0805
60	1	R42	1.5K,1/8W	Resistor,SM,1.5K,5%,1/8W,1206
61	3	R44,R45,R46	10ohm,1/8W	Resistor,SM,10 Ohm,5%,1/8W,1206
62	2	R59,R60	220ohm,.25W	Resistor,Axial,220 Ohm,5%,1/4W
63	1	R32	43ohm,.5W	Resistor,Axial,43 Ohm,5%,1/2W
64	1	R43	7.5K,.5W	Resistor,Axial,7.5K, 5%,1/2W
65	2	RN1,RN2	10K,RNET4	Resistor Nerwork,SM,4-pack,10K,5%,1/16W,CA Elec.,TSMB08-103J
66	1	T1	671-8039	Transformer,Modem,1:1,600ohm,Midcom 671-8039
67	1	U1	LM317MDT/LM317MT	IC,Regulator,LM317MDT/MT,DPAK/TO-220
68	1	U12	79L05AC	IC,-5 Volt Regulator,79L05AC,TO-92
69	1	U11	78L05AC	IC,+5 Volt Regulator,78L05AC,TO-92
70	1	U9	74HC4053	IC,SM,2-channel analog Mux,SOP-16
71	3	U6,U10,U13	TL082	IC,SM,Dual JFET OP Amp., TL082, SOP-8
72	1	U2	93LC66	IC,SM,EEPROM,Microchip,93LC66,Atmel,93C66-10SC-2.7,SO-8
73	1	U3	ES2890	IC,SM,ESS EDSP ES2890,TQFP-100
74	1	U4	ES2819	IC,SM,ESS Dual AFE CODECs,ES2819,TQFP-52
75	2	U5,U7	4N35S	IC,Optocoupler,4N35,DIP-6
76	1	U8	H11AA1	IC,AC-input Solid State Current Sensor,H11AA1,DIP-6
77	1	VR1	275V	Varistor, 275V 5mm,Harris V275LA4
78	1	Y1	18.432MHz	Crystal,18.432MHz,Fundamental
79	1	Y2	56.448MHz	Crystal,56.448MHz,3rd overtone,HC-49S
80	1	BKT	Bracket	Reat Panel, Purcell Bracket, Inc., PE02-ESS1, Rev.1
81	2	SCR	Screw	Bracket Screw 4-40,.3/16"

ORDERING INFORMATION

To order a complete modem solution, it is necessary to order the correct chipset.

Chipset P/N	Driver	IC	Code Description	Available
V.90 ISA				
ES56-IF	ES9I---DI	2890S, 2818F	data/fax V.90	4/30
ES56-IS	ES9I---DI	2890S, 2818P	data/fax V.90	4/30
ES56T-IF	ES9I-T-DI	2890S, 2818F	data/fax/tam V.90	4/30
ES56T-IS	ES9I-T-DI	2890S, 2818P	data/fax/tam V.90	4/30
ES56V-IF	ES9I-V-DI	2890S, 2819F	data/fax/voice V.90	4/30

Chipset part numbering scheme:

ESxx	C	V	P	X	S
Modem	Configuration	Telephony	Bus	Modem Code	AFE Package
336 – V.34	C – Combo	V – Voice	P - PCI	X – x2	S – ES2818P (SOIC)
56 – x2/V.90	- Modem	T – TAM	- ISA	I – V.90	F - ES2818F (PQFP)
		- Data/Fax		- V.34	and ES2819F (PQFP)

Driver numbering scheme:

ES9	X	C	V	I	D	M
Software	Current Code	Configuration	Telephony	New Code	Type	Bus
	336 – V.34	C – Combo	V - Voice	X – x2	D – DSP	I - ISA
	X – x2	– Modem	T – TAM	I – V.90	H – HSP	P - PCI
	I – V.90		– data/fax	-No new code		