



Monolithic N-Channel JFET Dual

PRODUCT SUMMARY

$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	g_{fs} Min (mS)	I_G Max (pA)	$ V_{GS1} - V_{GS2} $ Max (mV)
-1.0 to -4.5	-50	1	-50	25

FEATURES

- Monolithic Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 5 pA
- Low Noise: 9 nV/√Hz
- High CMRR: 100 dB

BENEFITS

- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

APPLICATIONS

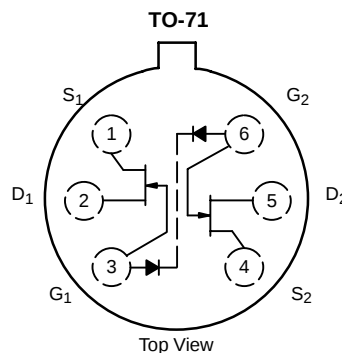
- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High Speed Comparators
- Impedance Converters

DESCRIPTION

The low cost 2N3958 JFET dual is designed for high-performance differential amplification for a wide range of precision test instrumentation applications. This series features tightly matched specs, low gate leakage for accuracy, and wide dynamic range with I_G guaranteed at $V_{DG} = 20$ V.

The hermetically-sealed TO-71 package is available with full military processing (see Military Information and the 2N5545/5546/5547JANTX/JANTXV data sheet).

For similar products see 2N5196/5197/5198/5199, the low-noise U/SST401 series, the high-gain 2N5911/5912, and the low-leakage U421/423 data sheets.



ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage -50 V
Gate Current 50 mA
Lead Temperature ($1/16$ " from case for 10 sec.) 300 °C
Storage Temperature -65 to 200 °C
Operating Junction Temperature -55 to 150 °C

Power Dissipation : Per Side^a 250 mW
Total^b 500 mW

Notes

- Derate 2 mW/°C above 85 °C
- Derate 4 mW/°C above 85 °C

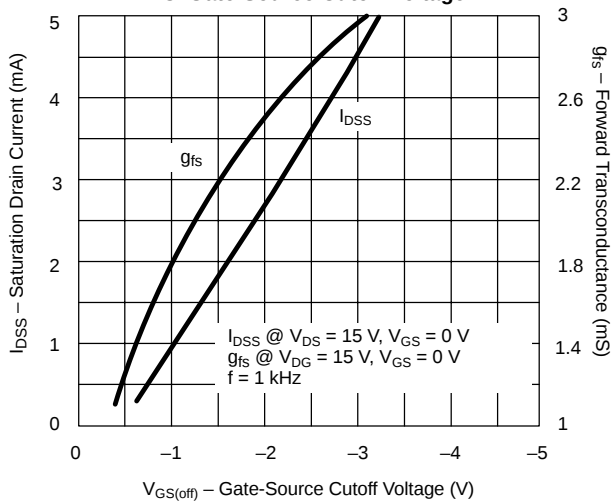
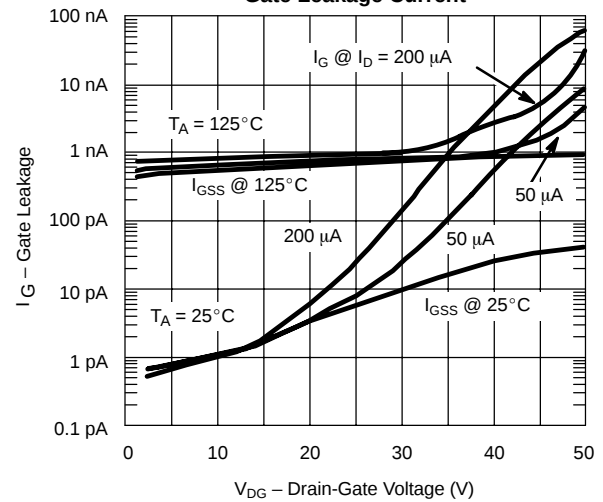
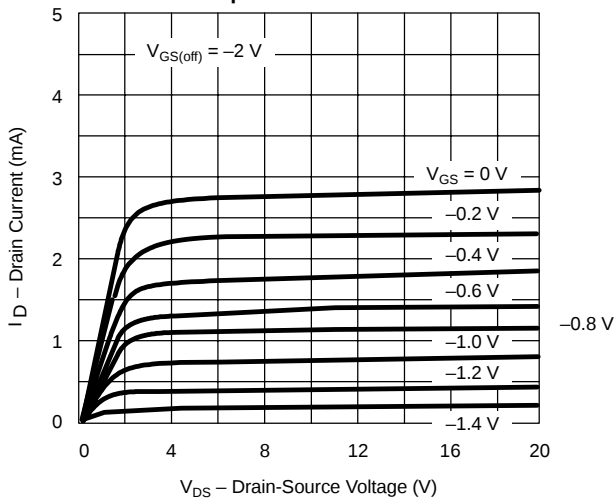
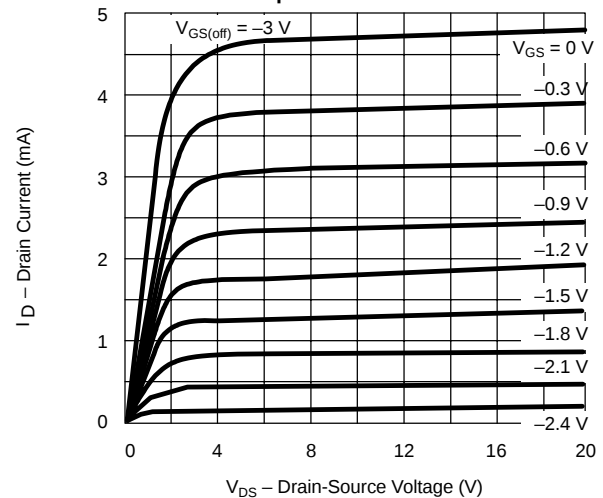
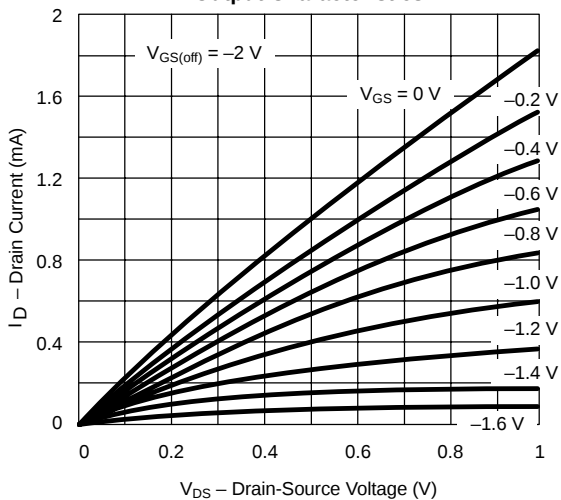
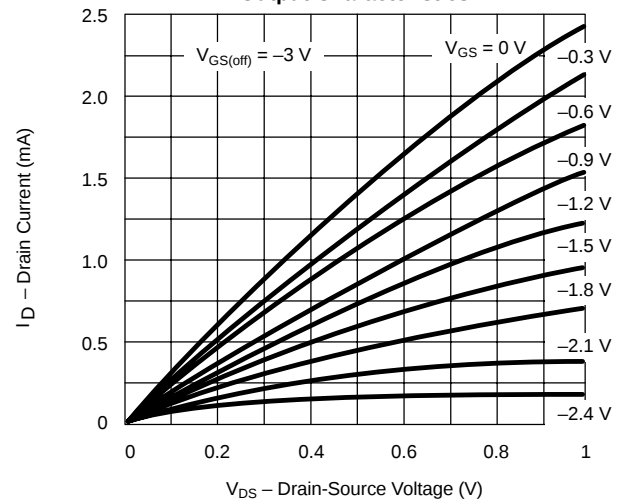
**SPECIFICATIONS (T_A = 25 °C UNLESS OTHERWISE NOTED)**

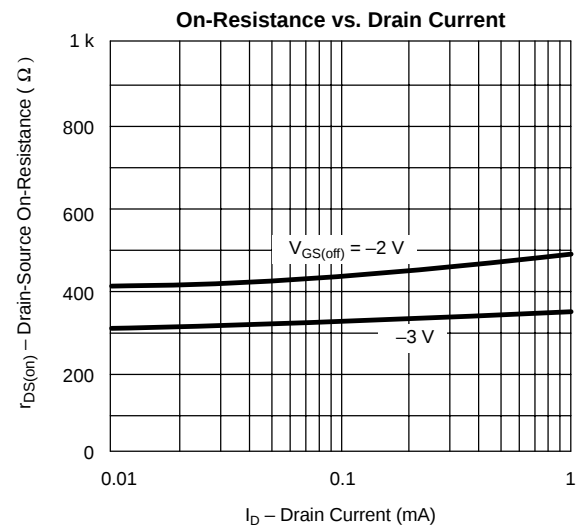
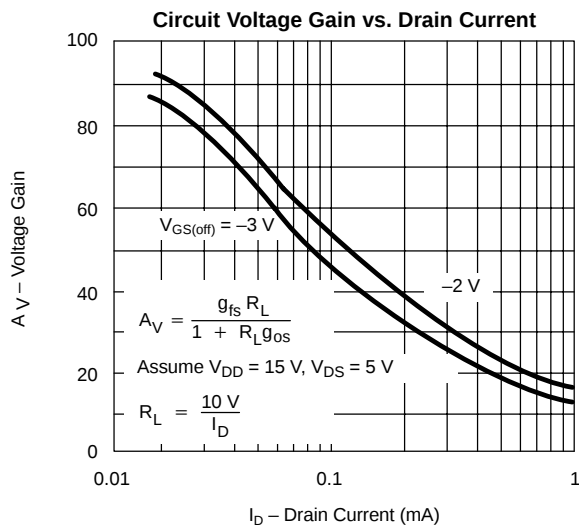
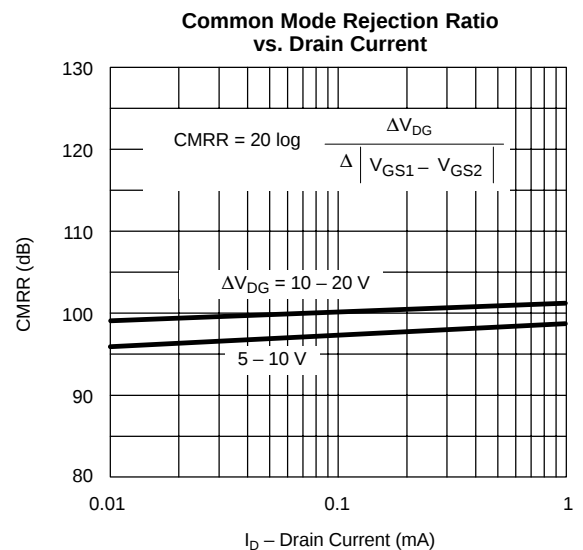
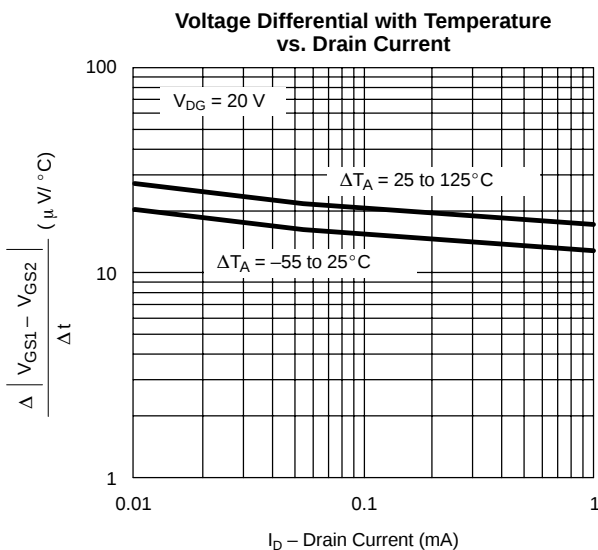
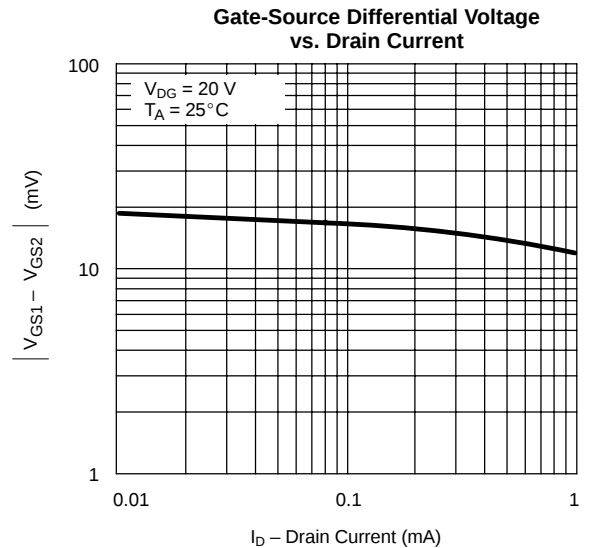
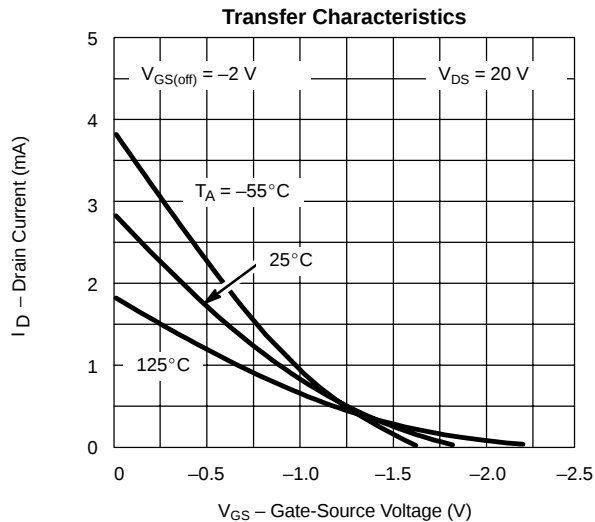
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ ^a	Max	
Static						
Gate-Source Breakdown Voltage	V _{(BR)GSS}	I _G = −1 μA, V _{DS} = 0 V	−50	−57		V
Gate-Source Cutoff Voltage	V _{GS(off)}	V _{DS} = 20 V, I _D = 1 nA	−1.0	−2	−4.5	
Saturation Drain Current ^b	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	0.5	3	5	mA
Gate Reverse Current	I _{GSS}	V _{GS} = −30 V, V _{DS} = 0 V		−10	−100	pA
		T _A = 150 °C		−20	−500	nA
Gate Operating Current	I _G	V _{DG} = 20 V, I _D = 200 μA		−5	−50	pA
		T _A =125 °C		−0.8	−250	nA
Gate-Source Voltage	V _{GS}	V _{DG} = 20 V, I _D = 200 μA	−0.5	−1.5	−4	V
		I _D = 50 μA			−4.2	
Gate-Source Forward Voltage	V _{GS(F)}	I _G = 1 mA, V _{DS} = 0 V			2	
Dynamic						
Common-Source Forward Transconductance	g _{fs}	V _{DS} = 20 V, V _{GS} = 0 V f = 1 kHz	1	2.5	3	mS
Common-Source Output Conductance	g _{os}			2	35	μS
Common-Source Input Capacitance	C _{iss}	V _{DS} = 20 V, V _{GS} = 0 V f = 1 MHz		3	4	pF
Common-Source Reverse Transfer Capacitance	C _{rss}			1	1.2	
Drain-Gate Capacitance	C _{dg}	V _{DG} = 10 V, I _S = 0 , f = 1 MHz			1.5	
Equivalent Input Noise Voltage	$\bar{e}_n$	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 kHz		9		nV/ √Hz
Noise Figure	NF	V _{DS} = 20 V, V _{GS} = 0 V f = 100 Hz, R _G = 10 MΩ			0.5	dB
Matching						
Differential Gate-Source Voltage	V _{GS1} −V _{GS2}	V _{DG} = 20 V, I _D = 200 μA		15	25	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1}-V_{GS2} }{\Delta T}$	V _{DG} = 20 V, I _D = 200 μA T _A = −55 to 125 °C		20	100	μV/°C
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V _{DS} = 20 V, V _{GS} = 0 V	0.85	0.97	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V _{DS} = 20 V, I _D = 200 μA f = 1 kHz	0.85	0.97	1	
Differential Output Conductance	g _{os1} −g _{os2}			0.1		μS
Differential Gate Current	I _{G1} −I _{G2}	V _{DG} = 20 V, I _D = 200 μA T _A = 125 °C		0.1	10	nA
Common Mode Rejection Ratio ^c	CMRR	V _{DG} = 10 to 20 V, I _D = 200 μA		100		dB

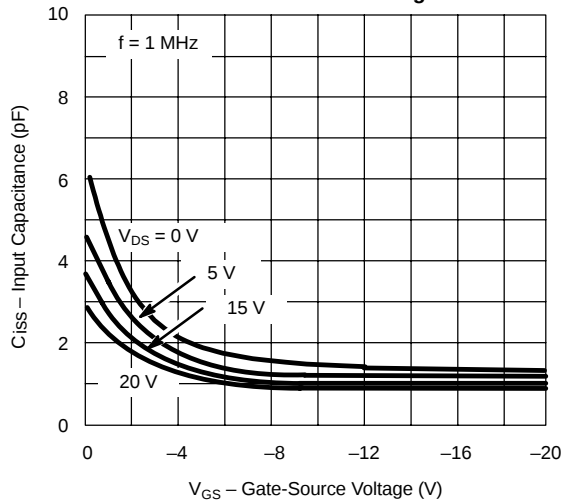
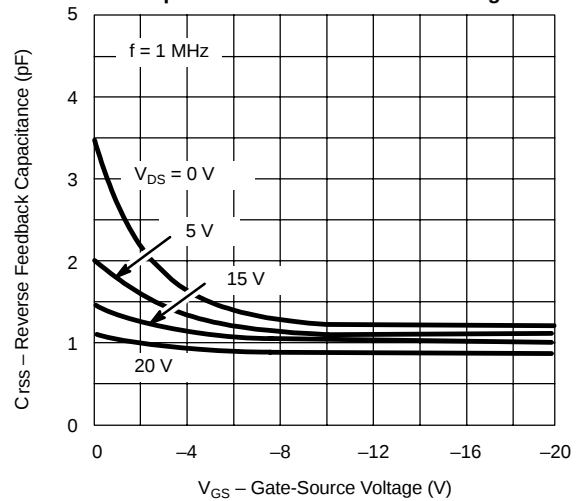
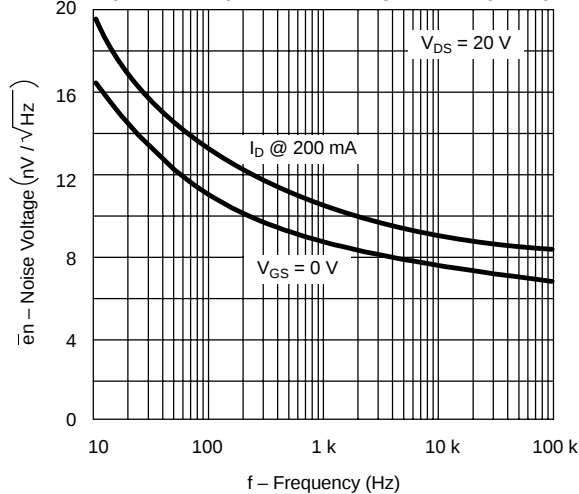
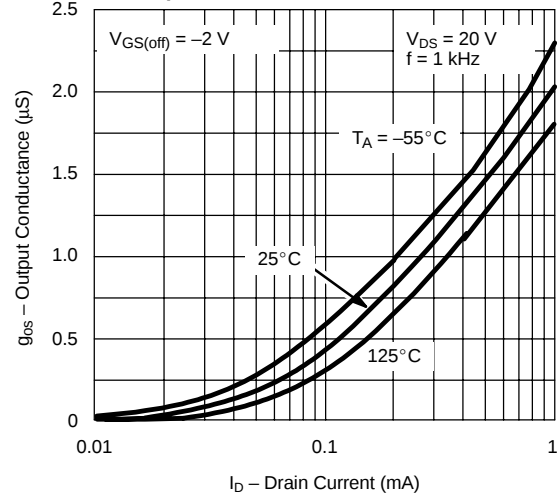
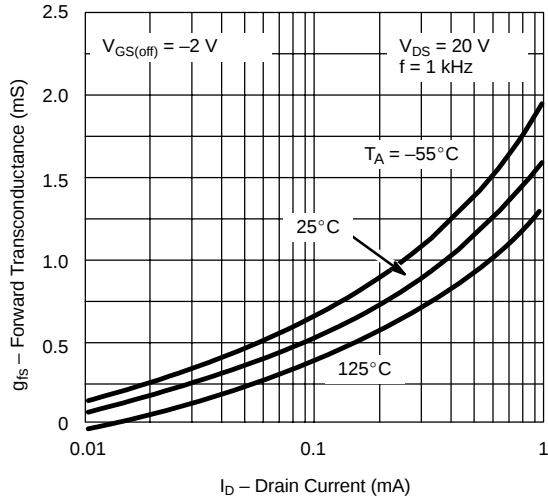
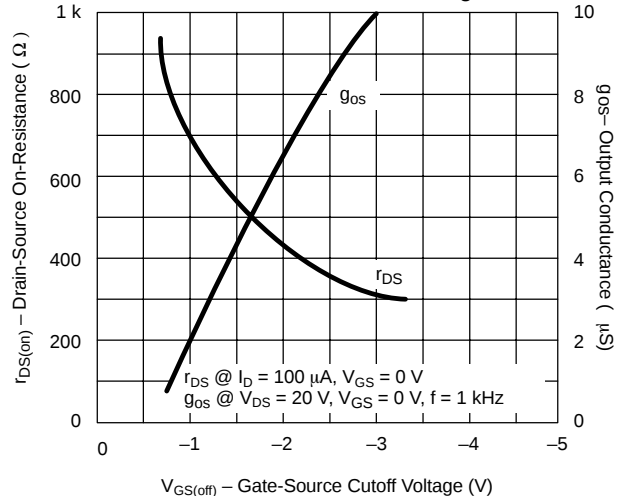
Notes

- a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.
c. This parameter not registered with JEDEC.

NQP

**TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)****Drain Current and Transconductance
vs. Gate-Source Cutoff Voltage****Gate Leakage Current****Output Characteristics****Output Characteristics****Output Characteristics****Output Characteristics**

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)


**TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)****Common-Source Input Capacitance
vs. Gate-Source Voltage****Common-Source Reverse Feedback
Capacitance vs. Gate-Source Voltage****Equivalent Input Noise Voltage vs. Frequency****Output Conductance vs. Drain Current****Common-Source Forward Transconductance
vs. Drain Current****On-Resistance and Output Conductance
vs. Gate-Source Cutoff Voltage**



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