ECL programmable array logic — 10H20EV8/10020EV8

DESCRIPTION

The 10H20EV8/10020EV8 is an ultra high-speed universal ECL PAL® device. Combining versatile output macrocells with a standard AND/OR single programmable array, this device is ideal in implementing a user's custom logic. The use of Philips Semiconductors state-of-the-art bipolar oxide isolation process enables the 10H20EV8/10020EV8 to achieve optimum speed in any design. The SNAP design software package from Philips Semiconductors simplifies design entry based upon Boolean or state equations.

The 10H20EV8/10020EV8 is a two-level logic element comprised of 11 fixed inputs, an input pin that can either be used as a clock or 12th input, 90 AND gates, and 8 Output Logic Macrocells. Each Output Macrocell can be individually configured as a dedicated input, dedicated output with polarity control, a bidirectional I/O, or as a registered output that has both output polarity control and feedback to the AND array. This gives the part the capability of having up to 20 inputs and eight outputs.

The 10H20EV8/10020EV8 has a variable number of product terms that can be OR'd per output. Four of the outputs have 12 AND terms available and the other four have 8 terms per output. This allows the designer the extra flexibility to implement those functions that he couldn't in a standard PAL device. Asynchronous Preset and Reset product terms are also included for system design ease. Each output has a separate output enable product term. Another feature added for the system designer is a power-up Reset on all registered outputs.

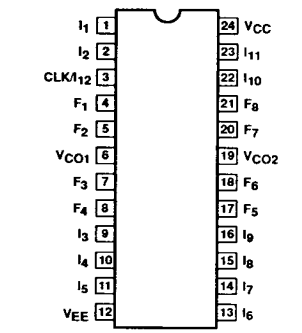
The 10H20EV8/10020EV8 also features the ability to Preload the registers to any desired state during testing. The Preload is not affected by the pattern within the device, so can be performed at any step in the testing sequence. This permits full logical verification even after the device has been patterned.

FEATURES

- Ultra high speed ECL device
  - t_{PD} = 4.5ns (max)
  - t_{IS} = 2.6ns (max)
  - t_{CKO} = 2.3ns (max)
  - f_{MAX} = 208MHz
- Universal ECL Programmable Array Logic
  - 8 user programmable output macrocells
  - Up to 20 inputs and 8 outputs
  - Individual user programmable output polarity
- Variable product term distribution allows increased design capability
- Asynchronous Preset and Reset capability
- 10KH and 100K options
- Power-up Reset and Preload function to enhance state machine design and testing
- Design support provided via SNAP and other CAD tools
- Security fuse for preventing design duplication
- Available in 24-Pin 300mil-wide DIP and 28-Pin PLCC.

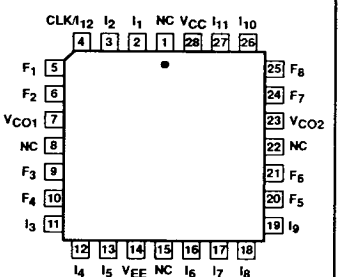
PIN CONFIGURATIONS

F Package



F = Ceramic DIP (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
24-Pin Ceramic Dual In-Line (300mil-wide)	10H20EV8–4F 10020EV8–4F	0586B
28-Pin Plastic Leaded Chip Carrier	10H20EV8–4A 10020EV8–4A	0401F

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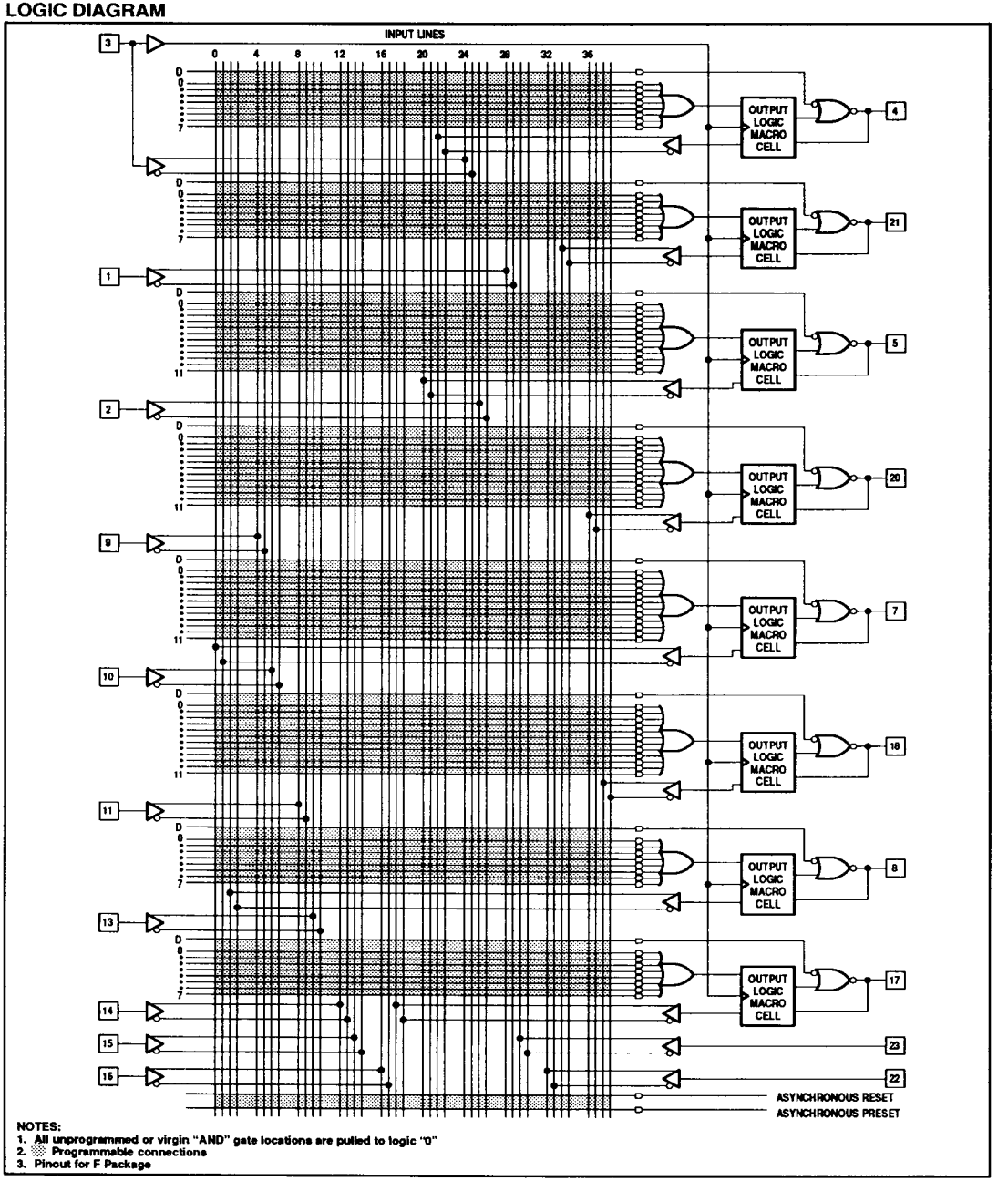
LOGIC DIAGRAM



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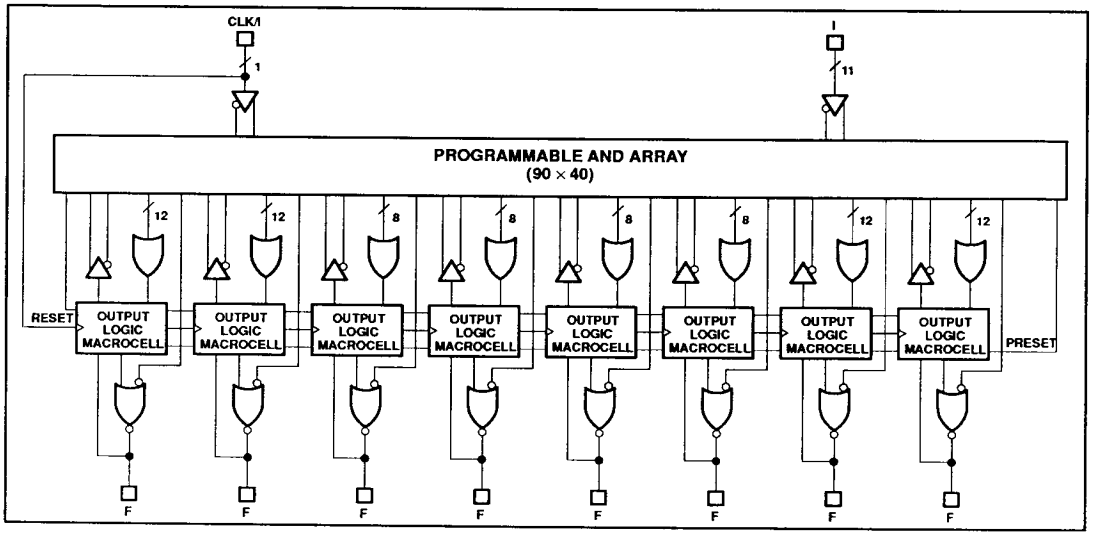
FUNCTIONAL DIAGRAM



FUNCTIONAL DESCRIPTION

The 10H20EV8/10020EV8 is an ultra high-speed universal ECL PAL-type device. Combining versatile Output Macrocells with a standard AND/OR single programmable array, this device is ideal in implementing a user's custom logic.

As can be seen in the Logic Diagram, the device is a two-level logic element with a programmable AND array. The 20EV8 can have up to 20 inputs and 8 outputs. Each output has a versatile Macrocell whereby the output can either be configured as a dedicated input, a dedicated combinatorial output with polarity control, a bidirectional I/O, or as a registered output that has both output polarity control and feedback into the AND array.

The device also features 90 product terms. Two of the product terms can be used for a global asynchronous preset and/or reset. Eight of the product terms can be used for individual output enable control of each Macrocell. The other 80 product terms are distributed among the outputs. Four of the outputs have eight product terms, while the other four have 12. This arrangement allows the utmost in flexibility when implementing user patterns.

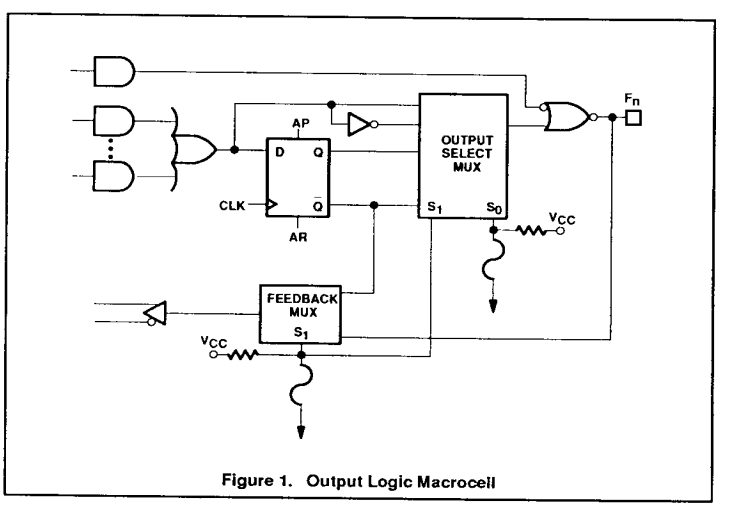


Figure 1. Output Logic Macrocell

Output Logic Macrocell

The 10H20EV8/10020EV8 incorporates an extremely versatile Output Logic Macrocell that allows the user complete flexibility when configuring outputs.

As seen in Figure 1, the 10H20EV8/10020EV8 Output Logic Macrocell consists of an edge-triggered D-type flip-flop, an output select MUX, and a feedback select MUX. Fuses S_0 and S_1 allow the user to select between the various cells. S_1 controls whether the output will be either registered with internal feedback or combinatorial I/O. S_0 controls the polarity of the output (Active-HIGH or Active-LOW). This allows the user to achieve the following configurations: Registered Active-HIGH output, Registered Active-LOW output, Combinatorial Active-HIGH output, and Combinatorial Active-LOW output. With the output enable product term, this list can be extended by adding the configurations of a Combinatorial I/O with Polarity or another input.

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER		RATING	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current		–50	mA
T_S	Operating Temperature range		–55 to +150	°C
T_J	Storage Temperature range	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

DC OPERATING CONDITIONS 10H20EV8

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS NOM	LIMITS MAX	UNIT
V_{CC}, V_{CO1}, V_{CO2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_{amb} = 0°C	–1170		–840	mV
		T_{amb} = +25°C	–1130		–810	mV
		T_{amb} = +75°C	–1070		–735	mV
V_{IL}	Low level input voltage	T_{amb} = 0°C	–1950		–1480	mV
		T_{amb} = +25°C	–1950		–1480	mV
		T_{amb} = +75°C	–1980		–1450	mV
T_{amb}	Operating ambient temperature range		0	+25	+75	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC OPERATING CONDITIONS 10020EV8

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS NOM	LIMITS MAX	UNIT
V_{CC}, V_{CO1}, V_{CO2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when opetating with the 10K or 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_{amb}	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC Electrical Characteristics will vary slightly from their specified values.

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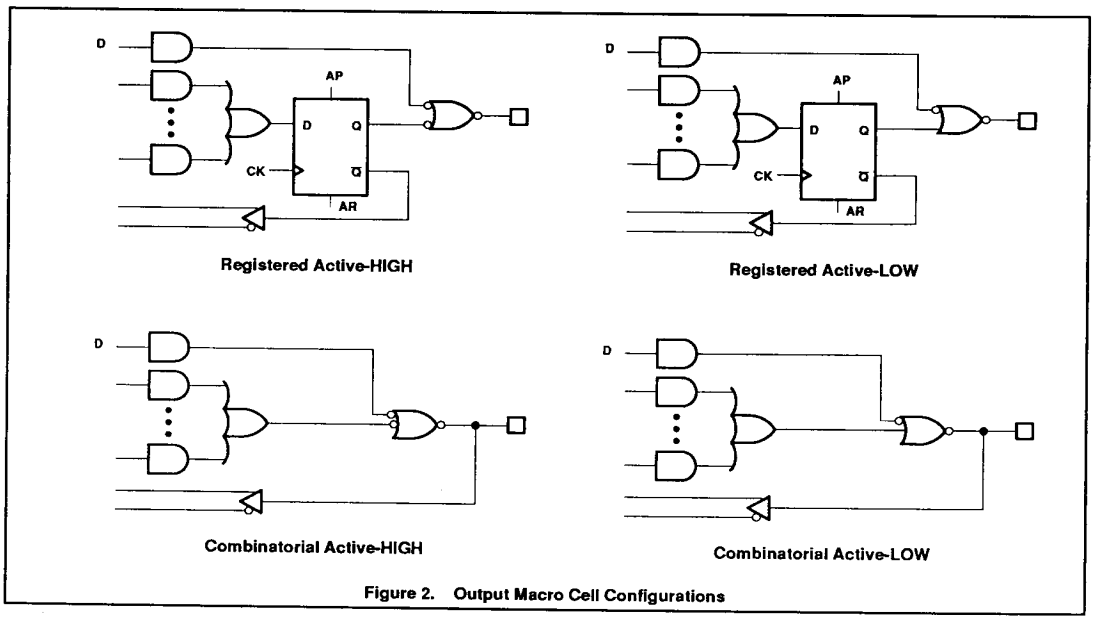

Figure 2. Output Macro Cell Configurations

OUTPUT MACRO CELL CONFIGURATION

Shown in Figure 2 are the four possible configurations of the output macrocell using fuses S_0 and S_1. As seen, the output can either be registered Active-HIGH/LOW with feedback or combinatorial Active-HIGH/LOW with feedback. If the registered mode is chosen, the feedback from the $\overline{Q}$ output to the AND array enables one to make state machines or shift registers without having to tie the output to one of the inputs. If a combinatorial output is chosen, the feedback gate is enabled from the pin and allows one to create permanent outputs, permanent inputs, or I/O pins through the use of the output enable (D) product term.

OUTPUT ENABLE

Each output on the 10H20EV8/10020EV8 has its own individual product term for output enable. The use of the D product term (direction control) allows the user three possible configurations of the outputs. They are: always enabled, always disabled, and controlled by a programmed pattern. A HIGH on the D term enables the output, while a LOW performs the disable function. Output enable control can be achieved by programming a pattern on the D term.

The output enable control can also be used to expand a designer's possibilities once a combinatorial output has been chosen. If the D term is always HIGH, the pin becomes a permanent Active-HIGH/LOW output. If the D term is always LOW (all fuses left intact), the pin now becomes an extra input.

PRESET AND RESET

The 10H20EV8/10020EV8 also includes a separate product term for asynchronous Preset and asynchronous Reset. These lines are common for all registers and are asserted when the specific product term goes HIGH. Being asynchronous, they are independent of the clock. It should be noted that the actual state of the output is dependent on how the polarity of the particular output has been chosen. If the outputs are a mix of Active-HIGH and Active-LOW, a Preset signal will force the Active-HIGH outputs HIGH while the Active-LOW outputs would go LOW, even though the Q output of all flip-flops would go HIGH. A Reset signal would force the opposite conditions.

PRELOAD

To simplify testing, the 10H20EV8/10020EV8 has also included PRELOAD circuitry. This allows a user to load any particular data desired into the registers regardless of the programmed pattern. This means that the PRELOAD can be done on a blank part and after that same part has been programmed to facilitate any post-fuse testing desired.

It can also be used by a designer to help debug a circuit. This could be important if a state machine was implemented in the 10H20EV8/ 10020EV8. The PRELOAD would allow the entry of any state in the sequence desired and start clocking from that particular point. Any or all transitions could be verified.

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DC ELECTRICAL CHARACTERISTICS 10H20EV8

$0°C \le T_{amb} \le +75°C$, $V_{EE} = -5.2V \pm 5\%$, $V_{CC} = V_{CO1} = V_{CO2} = GND$

SYMBOL	PARAMETER[1]	TEST CONDITIONS[2]	T_{amb}	LIMITS[4] MIN	LIMITS[4] MAX	UNITS
V_{OH}	High level output voltage	$V_{IN} = V_{IH}$ MIN or V_{IL} MAX	0°C +25°C +75°C	−1020 −980 −920	−840 −810 −735	mV
V_{OL}	Low level output voltage	$V_{IN} = V_{IH}$ MIN or V_{IL} MAX	0°C +25°C +75°C	−1950 −1950 −1950	−1630 −1630 −1600	mV
I_{IH}	High level input current	$V_{IN} = V_{IH}$ MAX	0°C +75°C		220	µA
I_{IL}	Low level input current	$V_{IN} = V_{IL}$ MIN Except I/O Pins	0°C +75°C	0.3		µA
$-I_{EE}$	Supply current	V_{EE} = MAX All inputs = V_{IH} MAX	0°C to +75°C		250	mA

DC ELECTRICAL CHARACTERISTICS 10020EV8

$0°C \le T_{amb} \le +85°C$, $-4.8V \le V_{EE} \le -4.2V$, $V_{CC} = V_{CO1} = V_{CO2} = GND$

SYMBOL	PARAMETER[1]	TEST CONDITIONS[2]			LIMITS[4] MIN	LIMITS[4] TYP	LIMITS[4] MAX	UNITS
V_{OH}	High level output voltage	Outputs Loaded with 50Ω to −2.0V ±0.010V	$V_{IN} = V_{IH}$ MAX or V_{IL} MIN	$V_{EE} = -4.2V$	−1020		−870	mV
				$V_{EE} = -4.5V$	−1025	−955	−880	mV
				$V_{EE} = -4.8V$	−1035		−880	mV
V_{OHT}	High level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inuts at V_{IHMAX} or V_{ILMIN}.	$V_{EE} = -4.2V$	−1030			mV
				$V_{EE} = -4.5V$	−1035			mV
				$V_{EE} = -4.8V$	−1045			mV
V_{OLT}	Low level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inuts at V_{IHMAX} or V_{ILMIN}.	$V_{EE} = -4.2V$			−1595	mV
				$V_{EE} = -4.5V$			−1610	mV
				$V_{EE} = -4.8V$			−1610	mV
V_{OL}	Low level output voltage		Inuts at V_{IHMAX} or V_{ILMIN}.	$V_{EE} = -4.2V$	−1810		−1605	mV
				$V_{EE} = -4.5V$	−1810	−1705	−1620	mV
				$V_{EE} = -4.8V$	−1830		−1620	mV
I_{IH}	High level input current	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					220	µA
I_{IL}	Low level input current	One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current	All inputs at V_{IHMAX}.					230	mA

NOTES:

1. All voltage measurements are referenced to the ground terminal.
2. Each ECL 10KH/100K series device has been designed to meet the DC specification after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min.) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3, of the *Philips Semiconductors 10/100K ECL Data Handbook*.
3. Terminals not specifically referenced can be left electrically open. Open inputs assume a logic LOW state. Any unused pins can be terminated to −2V. If tied to V_{EE}, it must be through a resistor > 10K. It is recommended that pins that have been programmed as RESET, PRESET, or CLOCK inputs not be left open due to the possibility of false triggering from internally and externally generated switching transients.
4. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.

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AC ELECTRICAL CHARACTERISTICS (for Ceramic Dual In-Line Package)

10H20EV8: $0°C \le T_{amb} \le +75°C$, $V_{EE} = -5.2V \pm 5\%$, $V_{CC} = V_{CO1} = V_{CO2} = GND$
10020EV8: $0°C \le T_{amb} \le +85°C$, $-4.8V \le V_{EE} \le -4.2V$, $V_{CC} = V_{CO1} = V_{CO2} = GND$

SYMBOL	PARAMETER	FROM	TO	LIMITS[1]									UNIT
				0°C			+25°C			+75°C/+85°C			
				MIN[2]	TYP[3]	MAX[2]	MIN[2]	TYP[3]	MAX[2]	MIN[2]	TYP[3]	MAX[2]	
Pulse Width													
t_{CKH}	Clock High	CLK +	CLK –	2.0	0.6		2.0	0.6		2.0	0.6		ns
t_{CKL}	Clock Low	CLK –	CLK +	2.0	0.9		2.0	0.9		2.0	0.9		ns
t_{CKP}	Clock Period	CLK +	CLK +	4.0			4.0			4.0			ns
t_{PRH}	Preset/Reset Pulse	(I, I/O) ±	(I, I/O) ±	4.5	—		4.5	—		4.5	—		ns
Setup and Hold Time													
t_{IS}	Input	(I, I/O) ±	CLK +	2.6	1.0		2.6	1.1		2.7	1.4		ns
t_{IH}	Input	CLK +	(I, I/O) ±	0.1	< 0		0.1	< 0		0.1	< 0		ns
t_{PRS}	Clock Resume after Preset/Reset	(I, I/O) ±	CLK +	4.6	1.0		4.6	0.9		4.6	0.8		ns
Propagation Delay													
t_{PD}	Input	(I, I/O) ±	I/O ±		2.85	4.7		2.95	4.7		3.35	4.7	ns
t_{CKO}	Clock	CLK +	I/O ±		1.65	2.4		1.7	2.4		2.0	2.5	ns
t_{OE}	Output Enable	(I, I/O) ±	I/O		2.0	4.2		2.1	4.2		2.2	4.2	ns
t_{OD}	Output Disable	(I, I/O) ±	I/O		2.0	4.2		2.1	4.2		2.2	4.2	ns
t_{PRO}	Preset/Reset	(I, I/O) ±	I/O ±		2.8	4.7		3.0	4.7		3.5	4.7	ns
t_{PPR}	Power-on Reset	V_{EE}	I/O		—	10		—	10		—	10	ns
f_{MAX}				212	377		212	357		204	294		MHz

NOTES:
1. Refer to AC Test Circuit and Voltage Wafeforms diagrams.
2. Maximum loading conditions: 89 fuses intact per row.
3. Typical loading conditions: 15 fuses intact per row. (All "inactive" fuses, except those necessary for correct functionality, are removed.)

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AC ELECTRICAL CHARACTERISTICS (for Plastic Leaded Chip Carrier)

10H20EV8: $0°C \le T_{amb} \le +75°C$, $V_{EE} = -5.2V \pm 5\%$, $V_{CC} = V_{CO1} = V_{CO2} = GND$
10020EV8: $0°C \le T_{amb} \le +85°C$, $-4.8V \le V_{EE} \le -4.2V$, $V_{CC} = V_{CO1} = V_{CO2} = GND$

SYMBOL	PARAMETER	FROM	TO	LIMITS[1]									UNIT
				0°C			+25°C			+75°C/+85°C			
				MIN	TYP[3]	MAX[2]	MIN	TYP[3]	MAX[2]	MIN	TYP[3]	MAX[2]	
Pulse Width													
t_{CKH}	Clock High	CLK +	CLK –	2.0	0.6		2.0	0.6		2.0	0.6		ns
t_{CKL}	Clock Low	CLK –	CLK +	2.0	0.9		2.0	0.9		2.0	0.9		ns
t_{CKP}	Clock Period	CLK +	CLK +	4.0			4.0			4.0			ns
t_{PRH}	Preset/Reset Pulse	(I, I/O) ±	(I, I/O) ±	4.5	—		4.5	—		4.5	—		ns
Setup and Hold Time													
t_{IS}	Input	(I, I/O) ±	CLK +	2.5	1.0		2.5	1.1		2.6	1.4		ns
t_{IH}	Input	CLK +	(I, I/O) ±	0	< 0		0	< 0		0	< 0		ns
t_{PRS}	Clock Resume after Preset/Reset	(I, I/O) ±	CLK +	4.5	1.0		4.5	0.9		4.5	0.8		ns
Propagation Delay													
t_{PD}	Input	(I, I/O) ±	I/O ±		2.85	4.5		2.95	4.5		3.35	4.5	ns
t_{CKO}	Clock	CLK +	I/O ±		1.65	2.2		1.7	2.2		2.0	2.3	ns
t_{OE}	Output Enable	(I, I/O) ±	I/O		2.0	4.0		2.1	4.0		2.2	4.0	ns
t_{OD}	Output Disable	(I, I/O) ±	I/O		2.0	4.0		2.1	4.0		2.2	4.0	ns
t_{PRO}	Preset/Reset	(I, I/O) ±	I/O ±		2.8	4.5		3.0	4.5		3.5	4.5	ns
t_{PPR}	Power-on Reset	V_{EE}	I/O		—	10		—	10		—	10	ns
f_{MAX}				212	377		212	357		204	294		MHz

NOTES:
1. Refer to AC Test Circuit and Voltage Wafeforms diagrams.
2. Maximum loading conditions: 89 fuses intact per row.
3. Typical loading conditions: 15 fuses intact per row. (All "inactive" fuses, except those necessary for correct functionality, are removed.)

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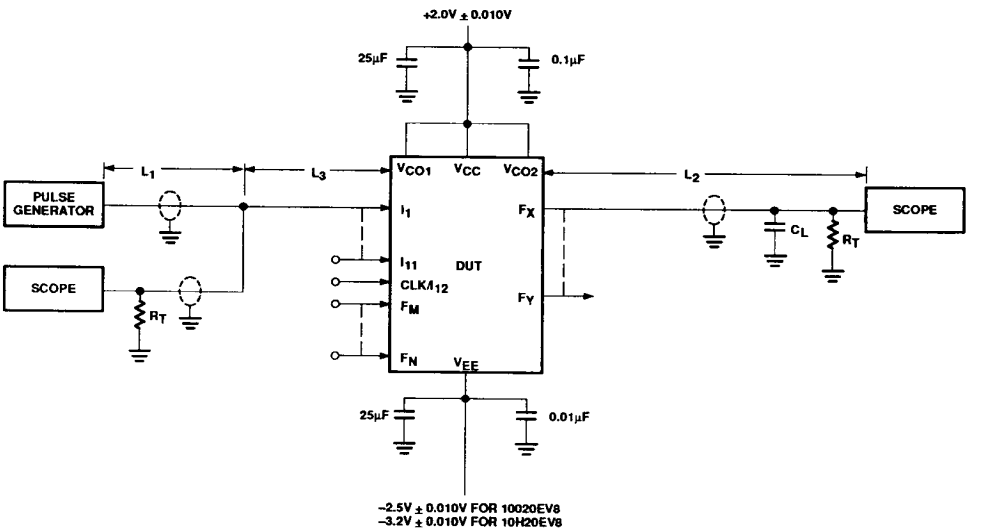
AC TEST CIRCUIT



NOTES:

1. Use decoupling capacitors of 0.1µF and 25µF from GND to V_{CC}, and 0.01µF and 25µF from GND to V_{EE} (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than $^1/_4$ inch (6mm).
2. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
3. All unused outputs are loaded with 50Ω to GND.
4. L_1 and L_2 are equal length 50Ω impedance lines. L_3, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed $^1/_4$ inch (6mm).
5. R_T = 50Ω terminator internal to Scope.
6. The unmatched wire stub between coaxial cable and pins under test must be less than $^1/_4$ inch (6mm) long for proper test.
7. C_L = Fixture and stray capacitance ≤ 3pF.
8. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed $^1/_4$ inch (6mm) in length (refer to section on AC setup procedure).
9. All 50Ω resistors should have tolerance of ± 1% or better.
10. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.

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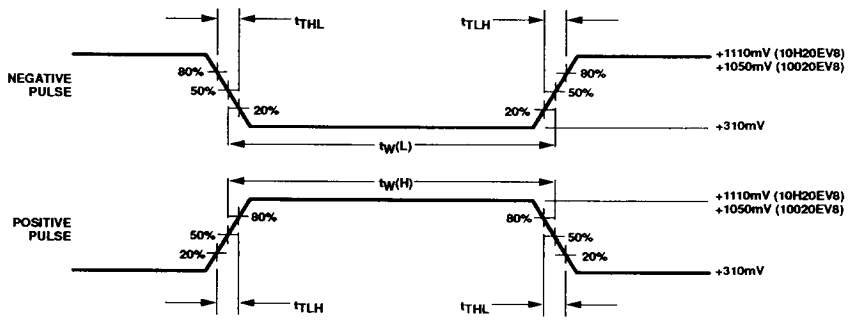
VOLTAGE WAVEFORMS



INPUT PULSE REQUIREMENTS $V_{CC} = V_{CO1} = V_{CO2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, V_T = GND (0V)					
FAMILY	AMPLITUDE	REP RATE	PULSE WIDTH	t_{TLH}	t_{THL}
10KH ECL	$800mV_{P-P}$	1MHz	500ns	$1.3 \pm 0.2ns$	$1.3 \pm 0.2ns$
INPUT PULSE REQUIREMENTS $V_{CC} = V_{CO1} = V_{CO2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, V_T = GND (0V)					
FAMILY	AMPLITUDE	REP RATE	PULSE WIDTH	t_{TLH}	t_{THL}
100K ECL	$740mV_{P-P}$	1MHz	500ns	$0.7 \pm 0.1ns$	$0.7 \pm 0.1ns$

Input Pulse Definition

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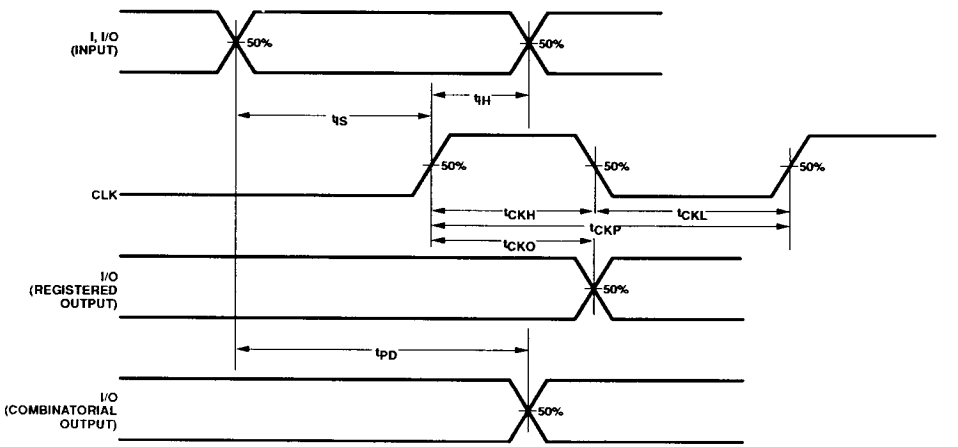
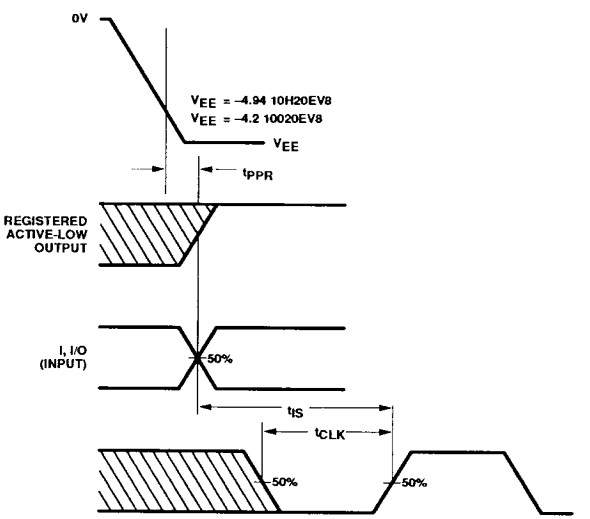
TIMING DIAGRAMS



Flip-Flop and Gate Outputs



Power-On Reset

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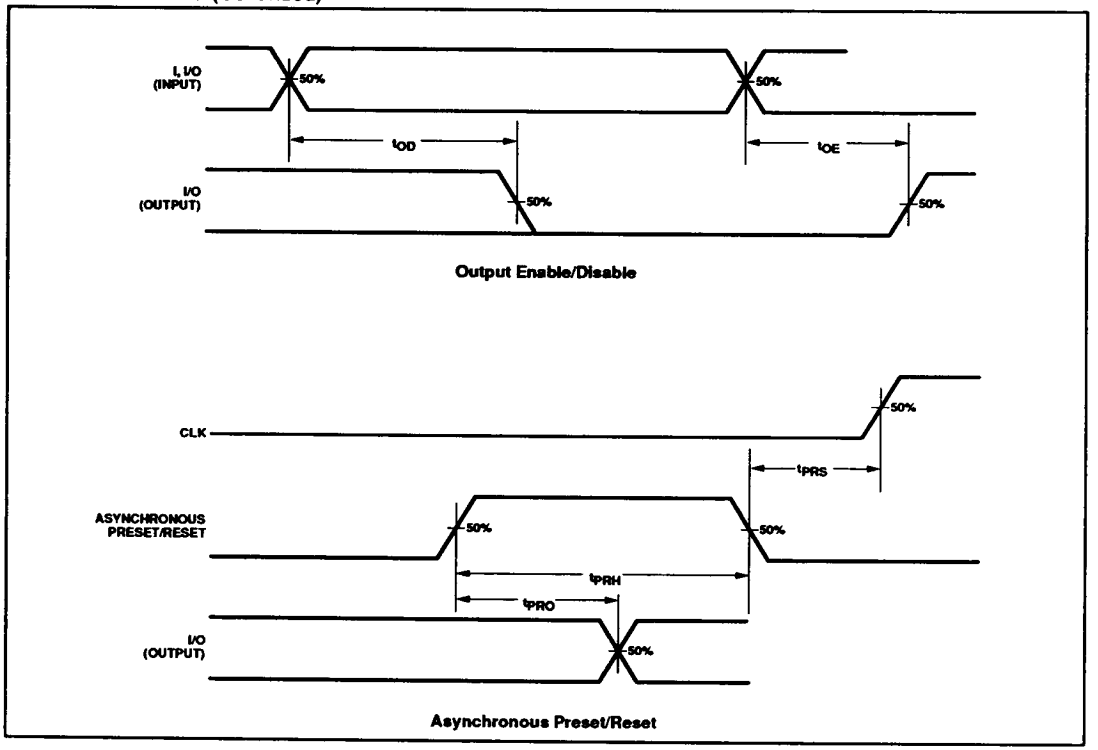
TIMING DIAGRAMS (Continued)



Output Enable/Disable

Asynchronous Preset/Reset

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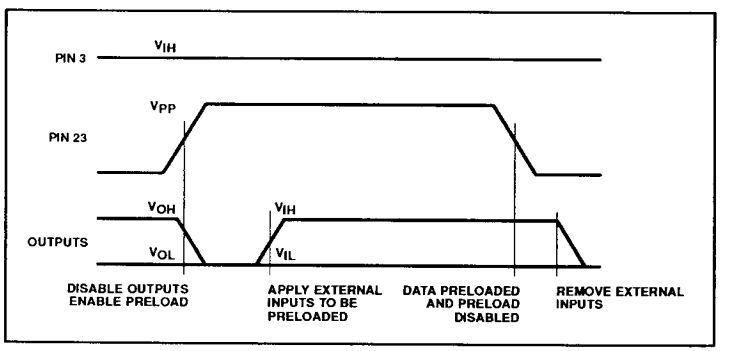
REGISTER PRELOAD

The 10H20EV8/10020EV8 has included circuitry that allows a user to load data into the output registers. Register PRELOAD can be done at any time and is not dependent on any particular pattern programmed into the device. This simplifies the ability to fully verify logic states and sequences even after the device has been patterned.

The pin levels and sequence necessary to perform the register PRELOAD are shown below.



SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP	MAX	
V_{IH}	Input HIGH level during PRELOAD and Verify	–1.1	–0.9	–0.7	V
V_{IL}	Input LOW level during PRELOAD and Verify	–1.85	–1.65	–1.45	V
V_{PP}	PRELOAD enable voltage applied to I_{11}	1.45	1.6	1.75	V

NOTE:

1. Unused inputs should be handled as follows:
   - Set at V_{IH} or V_{IL}
   - Terminated to –2V
   - Tied to V_{EE} through a resistor > 10K
   - Open

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LOGIC PROGRAMMING

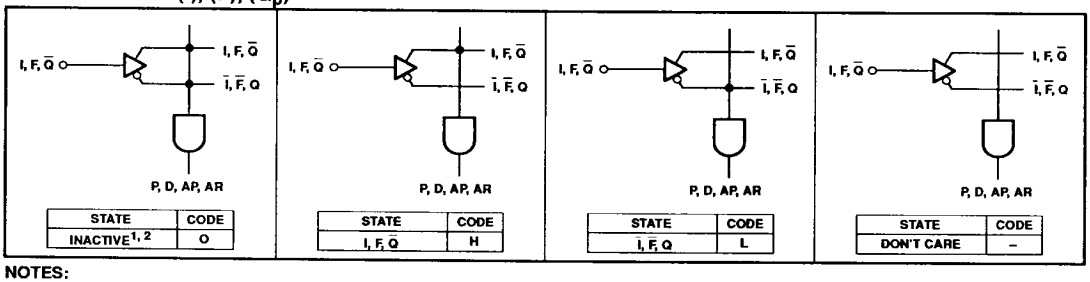
The 10H20EV8/10020EV8 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors SNAP design software package. ABEL™ and CUPL™ design software packages also support the 10H20EV8/10020EV8.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

10H20EV8/10020EV8 logic designs can also be generated using the program table entry format detailed on the following page. This program table entry format is supported by SNAP only.

To implement the desired logic functions, the state of each logic variable from logic equations (I, F, Q, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

"AND" ARRAY – (I), (F), ($\overline{Q}_p$)



NOTES:
1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates.
2. Any gate (P, D, AP, AR) will be unconditionally inhibited if any one of the I, F or Q link pairs is left intact.

OUTPUT MACROCELL CONFIGURATIONS

OUTPUT MACROCELL CONFIGURATION	CONTROL WORD FUSE	POLARITY FUSE
Registered Output, Active-HIGH	D	H
Registered Output, Active-LOW	D[1]	L[1]
Combinatorial I/O, Active-HIGH	B	H
Combinatorial I/O, Acitve-LOW	B	L

NOTE:
1. This is the initial (unprogrammed) state of the device.

PROGRAMMING AND SOFTWARE SUPPORT

Refer to Section 9 *(Development Software)* and Section 10 *(Third-party Programmer/ Software Support)* of the 1992 PLD Data Handbook for additional information.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

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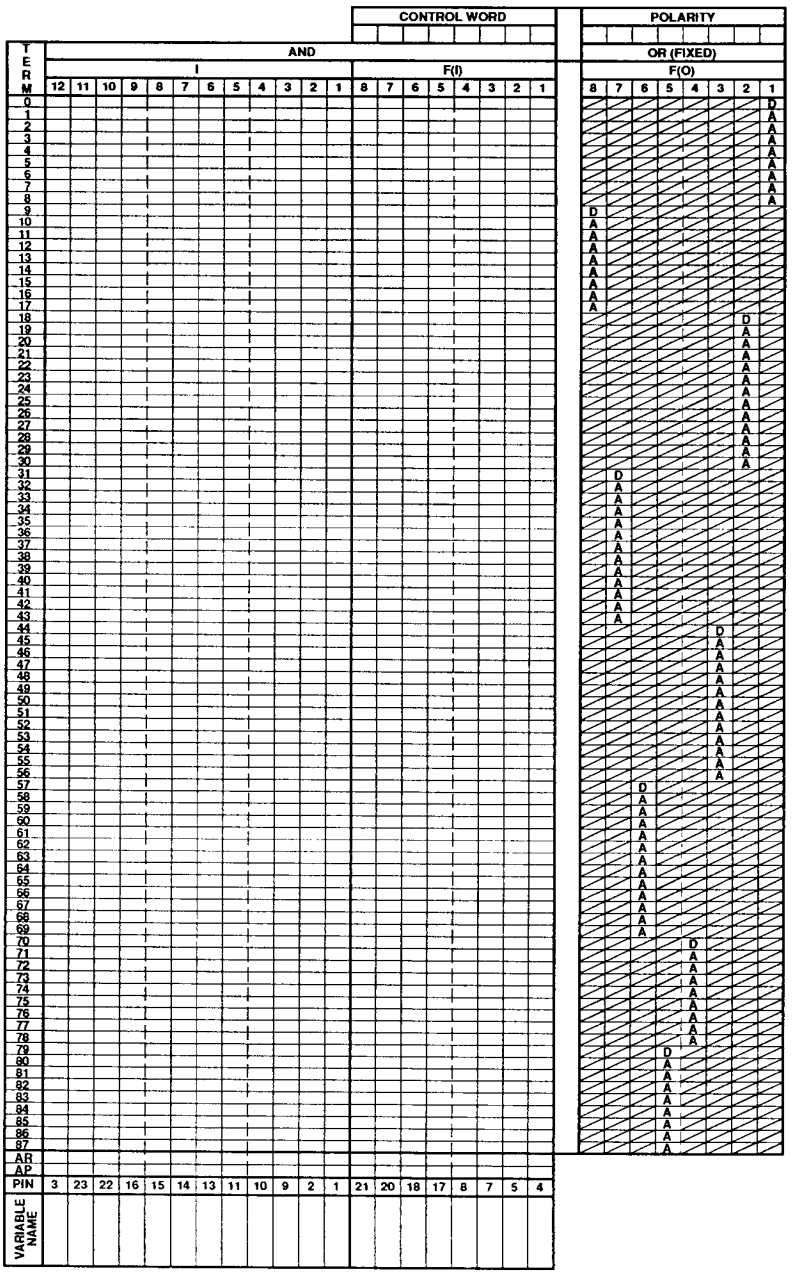
PROGRAM TABLE



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SNAP

Features

- Schematic entry using DASH™ 4.0 or above or OrCAD™ SDT III
- State Equation Entry
- Boolean Equation Entry
- Allows design entry in any combination of above formats
- Simulator
  - Logic and fault simulation
  - Timing model generation for device timing simulation
  - Synthetic logic analyzer format
- Macro library for standard TTL and user defined functions
- Device independent netlist generation
- JEDEC fuse map generated from netlist

SNAP (Synthesis, Netlist, Analysis and Program) is a versatile development tool that speeds the design and testing of PML. SNAP combines a user-friendly environment and powerful modules that make designing with PML simple. The SNAP environment gives the user the freedom to design independent of the device architecture.

The flexibility in the variations of design entry methodologies allows design entry in the most appropriate terms. SNAP merges the inputs, regardless of the type, into a high-level netlist for simulation or compilation into a JEDEC fuse map. The JEDEC fuse map can then be transferred from the host computer to the device programer.

SNAP's simulator uses a synthetic logic analyzer format to display and set the nodes of the design. The SNAP simulator provides complete timing information, setup and hold-time checking, plus toggle and fault grading analysis.

SNAP operates on an IBM® PC/XT, PC/AT, PS/2, or any compatible system with DOS 2.1 or higher. A minimum of 640K bytes of RAM is required together with a hard disk.

DESIGN SECURITY

The 10H20EV8/10020EV8 has a programmable security fuse that controls the access to the data programmed in the device. By using this programmable feature, proprietary designs implemented in the device cannot be copied or retrieved.

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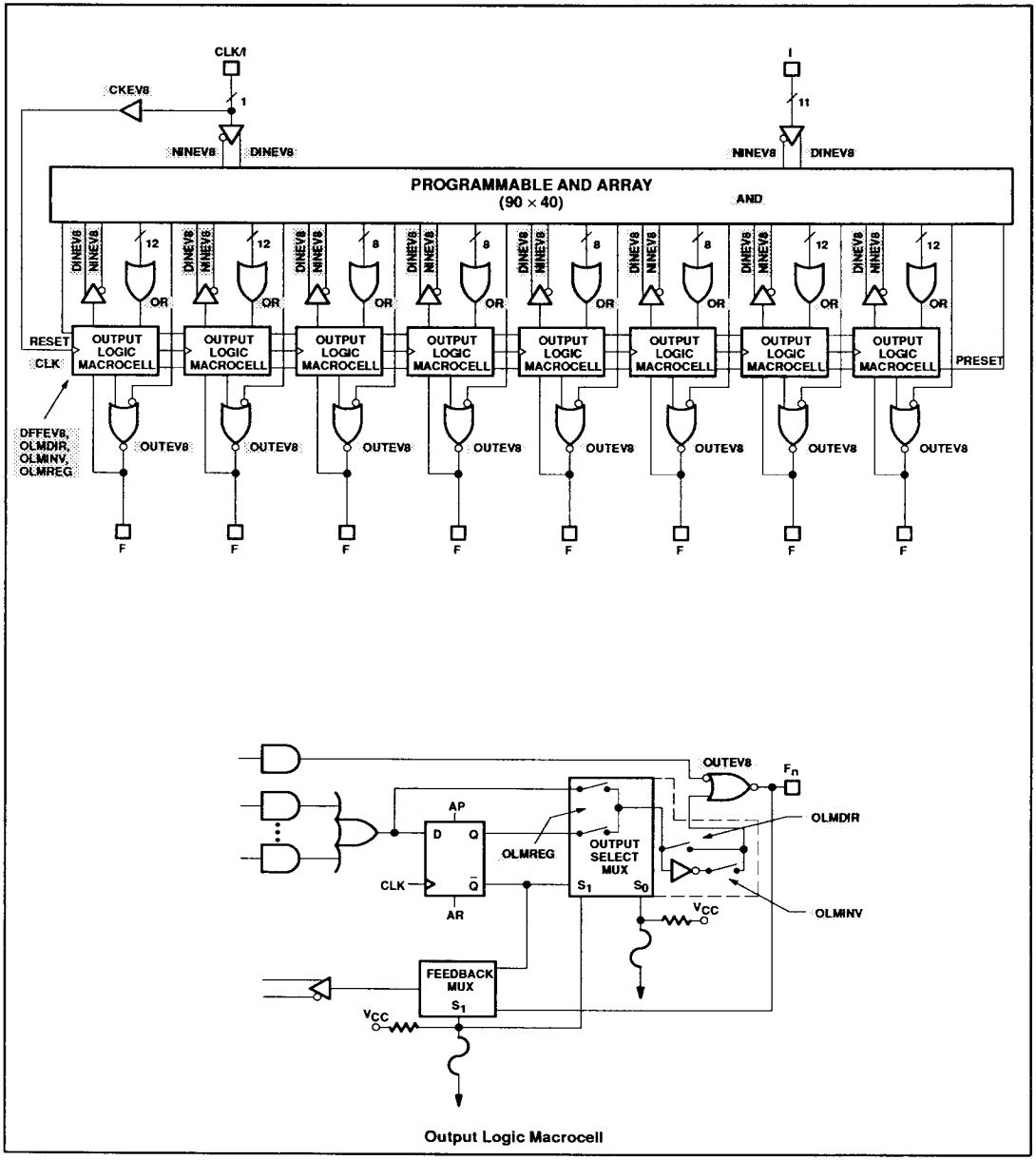
SNAP RESOURCE SUMMARY DESIGNATIONS



Output Logic Macrocell

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