Quad D-type flip–flop (3-State) 74F173

FEATURES

- Edge–triggered D–type register
- Gated clock enable for hold "do nothing" mode
- 3–state output buffers
- Gated output enable control
- Speed upgrade of N8T10 and current sink upgrade
- Controlled output edges to minimize ground bounces
- 48mA sinking capability

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F173	125MHz	23mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
16–pin plastic DIP	N74F173N
16–pin plastic SO	N74F173D

DESCRIPTION

The 74F173 is a high speed 4–bit parallel load registor with clock enable control, 3–state buffered outputs, and master reset (MR). When the two clock enable ($\overline{E}0$ and $\overline{E}1$) inputs are low, the data on the D inputs is loaded into the register simultaneously with low–to–high clock (CP) transition. When one or both enable inputs are high one setup time before the low–to–high clock transition, the register retains the previous data.

Data inputs and clock enable inputs are fully edge–triggered and must be stable only one setup time before the low–to–high clock transition.

The master reset (MR) is an active–high asynchronous input. When the MR is high, all four flip–flops are reset (cleared) independently of any other input condition.

The 3–state output buffers are controlled by a 2–input NOR gate. When both output enable ($\overline{OE}0$ and $\overline{OE}1$) inputs are low, the data in the register is presented at the Q output.

When one or both $\overline{OE}$ inputs are high, the outputs are forced to a high impedance "off" state.

The 3–state output buffers are completely independent of the register operation; the $\overline{OE}$ transition does not affect the clock and reset operations.

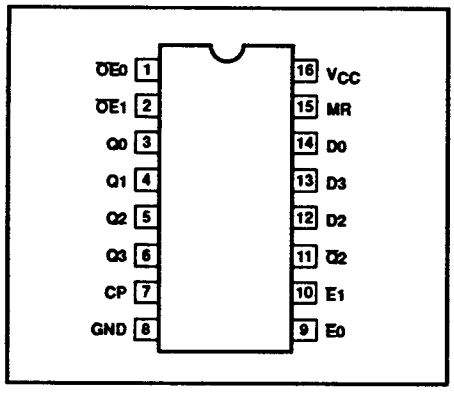
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	1.0/1.0	20µA/0.6mA
CP	Clock input	1.0/1.0	20µA/0.6mA
$\overline{E}0$, $\overline{E}1$	Clock enable inputs	1.0/1.0	20µA/0.6mA
MR	Master reset input	1.0/1.0	20µA/0.6mA
$\overline{OE}0$, $\overline{OE}1$	Output enable inputs	1.0/1.0	20µA/0.6mA
Q0 – Q3	Data outputs	750/80	15mA/48mA

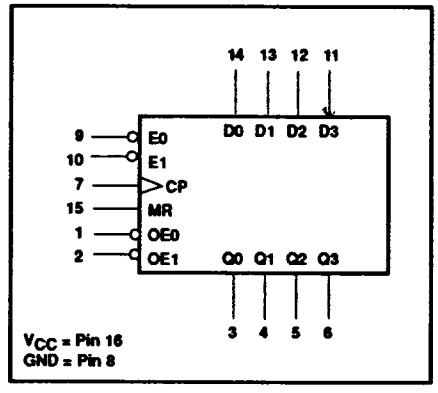
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

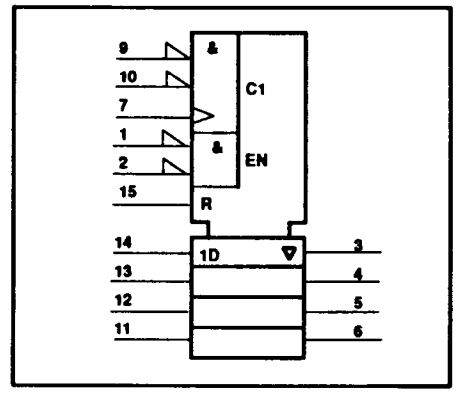
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



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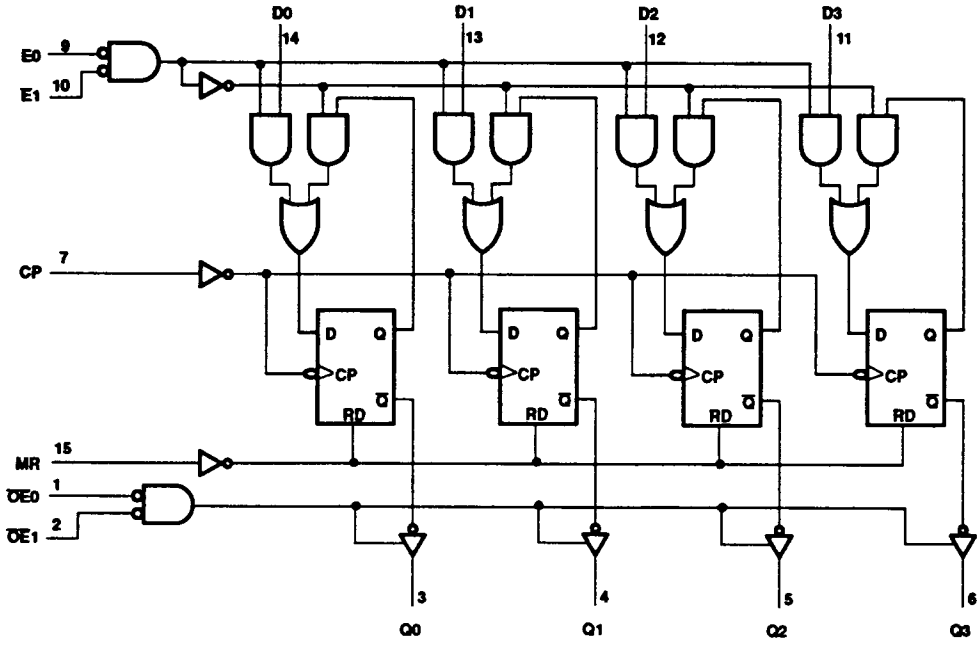
LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS	OUTPUTS
MR	CP	$\overline{E0}$	$\overline{E1}$	Dn	Qn (register)	
H	X	X	X	X	L	Reset (clear)
L	↑	l	l	l	L	Parallel load
L	↑	l	l	h	H	
L	X	h	X	X	qn	Hold (do nothing)
L	X	X	h	X	qn	

Notes to function table
1. H = High–voltage level
2. h = High state one setup time before the low–to–high clock transition
3. L = Low–voltage level
4. l = Low state one setup time before the low–to–high clock transition
5. qn = Lower case letters indicate the state of the referenced input (or output) on setup time prior to the low–to–high clock transition
6. X = Don't care
7. ↑ = Low–to–high clock transition

FUNCTION TABLE

INPUTS			OUTPUTS	OUTPUTS
Qn (register)	$\overline{OE0}$	$\overline{OE1}$	Qn	
L	L	L	L	Read
H	L	L	H	
X	H	X	Z	Disabled
X	X	H	Z	

Notes to function table
1. H = High–voltage level
2. L = Low–voltage level
3. X = Don't care
4. Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	96	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–15	mA
I_{OL}	Low–level output current			48	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
			V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.0			V
			V_{IH} = MIN, I_{OH} = –15mA	±5%V_{CC}	2.0	3.1		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OZH}	Off–state output current, high–level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off–state output current, low–level voltage applied		V_{CC} = MAX, V_O = 0.5V				–50	µA
I_{OS}	Short–circuit output current3		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			19	26	mA
		I_{CCL}				27	37	mA
		I_{CCZ}				23	32	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

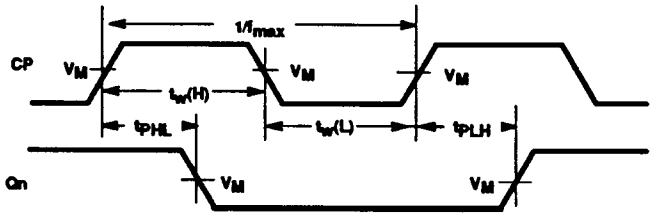
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	100	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	Waveform 1	4.5 6.0	6.5 8.0	9.0 10.5	4.0 5.5	10.0 11.5	ns
t_{PHL}	Propagation delay MR to Qn	Waveform 2	6.5	8.5	11.5	6.0	12.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low level	Waveform 4 Waveform 5	3.5 5.5	5.0 7.0	8.0 10.0	2.5 4.5	8.5 11.0	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level	Waveform 4 Waveform 5	1.5 3.0	3.5 5.0	7.0 8.5	1.0 2.5	8.0 9.0	ns
t_{THL} t_{TLH}	Transition time 10% to 90%, 90% to 10%	Waveform 5 Waveform 4	2.0 4.0	5.0 7.5	8.0 10.0	2.0 4.0	8.5 11.0	ns

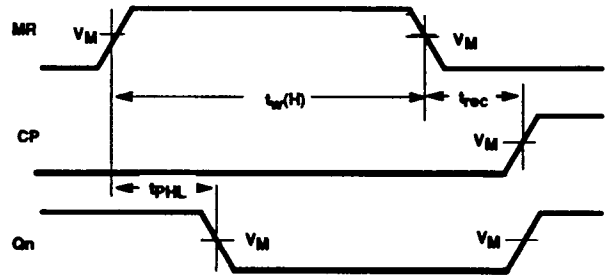
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low level Dn to CP	Waveform 3	2.5 2.5			3.0 4.0		ns
t_h (H) t_h (L)	Hold time, high or low level Dn to CP	Waveform 3	0 0			0 0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low level $\overline{E}$ to CP	Waveform 3	4.5 7.5			5.0 8.5		ns
t_h (H) t_h (L)	Hold time, high or low level $\overline{E}$ to CP	Waveform 3	0 0			0 0		ns
t_w (H) t_w (L)	CP Pulse width, high or low	Waveform 1	3.0 6.0			3.0 6.0		ns
t_w (H)	MR Pulse width, high	Waveform 2	3.5			3.5		ns
t_{rec}	Recovery time, MR to CP	Waveform 2	4.5			5.5		ns

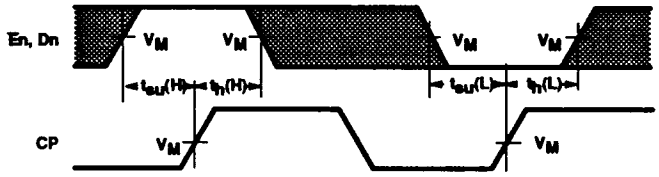
AC WAVEFORMS



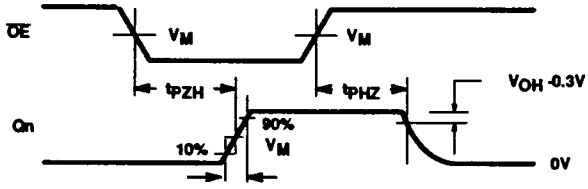
Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency



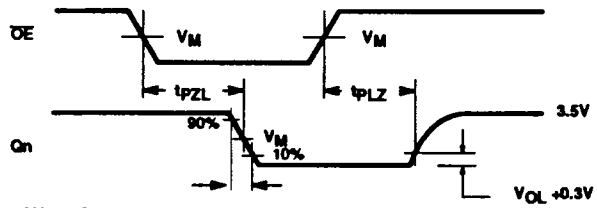
Waveform 2. Master reset pulse width, master reset to output delay and master resetf to clock recovery time



Waveform 3. Data and enable setup time and hold times



Waveform 4. 3-state output enable time to high level, output disable time from high level and transition time to high level



Waveform 5. 3-state output enable time to low level, output disable time from low level and transition time to low level

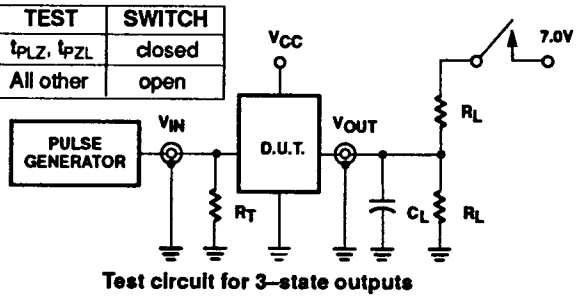
Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



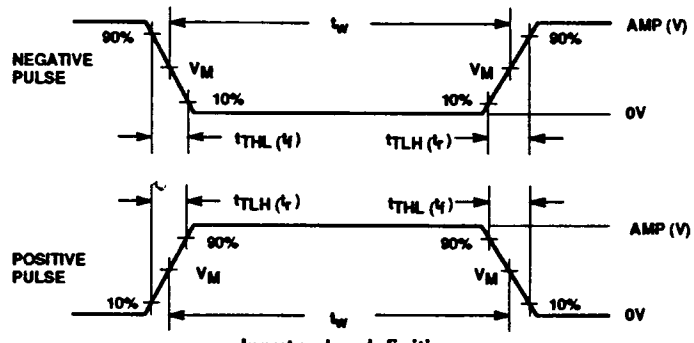
Test circuit for 3–state outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns