DALLAS SEMICONDUCTOR

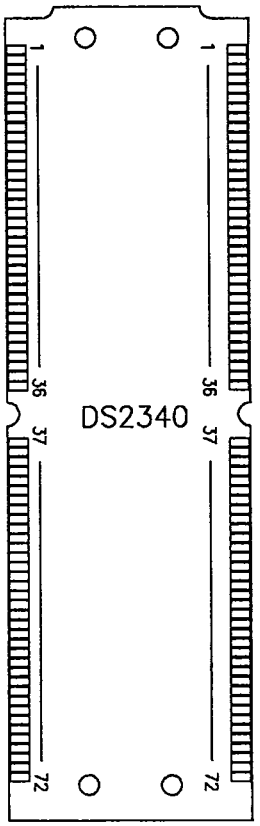
DS2340
Soft V40 Flip Stik

T-49-19-07

FEATURES

- V40-based embedded control system adapts to task-at-hand:
  - -Up to 256K bytes of lithium-backed NV SRAM for program/data storage
  - -Serial bootstrap loading of software
  - -Code can be changed in end use
- Incorporates V40 family processor:
  - -Executes industry-standard 8086 instruction set
  - -On-chip timers, serial I/O, DMA, and interrupt control
  - -Allows code development in native instruction set of IBM PC
- Crashproof operation during transient conditions
- Provides 3 enhanced 8-bit parallel I/O ports
- DS2340T provides DS1283 Watchdog Timekeeper Chip
- Dual 72-pin SIMM connection scheme supports single-board or expanded operation

PACKAGE OUTLINE



72-Pin SIMM Double-edge Connector

DESCRIPTION

The DS2340 and DS2340T Soft V40 Flip Stiks are complete, 8086-compatible microcontroller systems that provide the benefits of adaptability, crashproof operation, and powerful I/O capabilities for embedded control applications in an extremely small form factor. These unique features are made possible by the incorporation of the DS5340 V40 Softener Chip. In addition, the DS2340 and DS2340T execute the native instruction set of the IBM PC, so that the PC can serve as a development platform for the Soft V40 Flip Stiks. As a result, a wide variety of high-level language compilers, assemblers, and debugging tools are available to support system designs based on the DS2340.

The DS2340 offers two SIMM card-edges to support single-board and expanded operations. This scheme allows the Flip Stik to be installed into a 72-pin SIMM connector in one of two ways to support the selected operation. Connector A supports single-board operation. This card edge provides a total of three 8-bit parallel I/O ports. One of these ports allows each pin to serve as an interrupt input. The other two ports can be configured as a high-speed interface to allow the DS2340 to act as a peripheral controller to a host microprocessor system. For expanded operation, connector B supports all of the address lines as well as DMA handshake and bus control lines.

The DS2340T incorporates a DS1283 Watchdog Timekeeper Chip as a permanently-powered clock/calendar function that keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years. The clock is parallel-accessed by the V40 processor and is powered by the onboard lithium cell for greater than 10 years of timekeeping in the absence of V_{cc}.

NOTE: Throughout this data sheet, when features are discussed that are generic to both the time and non-time versions of the DS2340, the device is referred to as the DS2340(T).

PIN DESCRIPTION

Tables 1 and 2 document the pin assignments for sides A and B, respectively, for the DS2340(T). Table 3 is a summary of the pin functions that are common for both sides A and B. Finally, Tables 4 and 5 summarize pin functions unique to sides A and B, respectively.

DS2340(T) SIDE A PIN ASSIGNMENT Table 1

1 - AD0	25 - PB.3	49 - TOUT2
2 - AD1	26 - PB.4	50 - TCLT2
3 - AD2	27 - PB.5	51 - TCLK
4 - AD3	28 - PB.6	52 - A16
5 - AD4	29 - PB.7	53 - A15
6 - AD5	30 - IBR\	54 - A14
7 - AD6	31 - PCE2\	55 - A13
8 - AD7	32 - CE4\	56 - A12
9 - INTP1	33 - CE3\	57 - A11
10 - INTP2	34 - CE2\	58 - A10
11 - INTP3	35 - V_{cc}	59 - A9
12 - INTP4	36 - GND	60 - A8
13 - INTP6	37 - GND	61 - INTAK\/TOUT1/SRDY\
14 - TXD	38 - V_{cc}	62 - ASTB
15 - RXD	39 - X1	63 - PA.7
16 - IOWR\	40 - X2	64 - PA.6
17 - MWR\	41 - PC.7	65 - PA.5
18 - IORD\	42 - PC.6	66 - PA.4
19 - MRD\	43 - PC.5	67 - PA.3
20 - RST\	44 - PC.4	68 - PA.2
21 - INTP\	45 - PC.3	69 - PA.1
22 - PB.0	46 - PC.2	70 - PA.0
23 - PB.1	47 - PC.1	71 - RL\
24 - PB.2	48 - PC.0	72 - NMI

(\Denotes Condition Low)

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DS2340(T) SIDE B PIN ASSIGNMENT Table 2

1 - AD0	25 - BUFR/W\	49 - A19
2 - AD1	26 - REFRQ\	50 - A18
3 - AD2	27 - DMARQ0	51 - A17
4 - AD3	28 - DMAAK0\	52 - A16
5 - AD4	29 - DMARQ1	53 - A15
6 - AD5	30 - DMAAK1	54 - A14
7 - AD6	31 - PCE2\	55 - A13
8 - AD7	32 - CE4\	56 - A12
9 - INTP1	33 - CE3\	57 - A11
10 - INTP2	34 - CE2\	58 - A10
11 - INTP3	35 - V_{cc}	59 - A9
12 - INTP4	36 - GND	60 - A8
13 - INTP6	37 - GND	61 - A7
14 - TXD	38 - V_{cc}	62 - A6
15 - RXD	39 - X1	63 - A5
16 - IOWR\	40 - X2	64 - A4
17 - MWR\	41 - END/TC\	65 - A3
18 - IORD\	42 - BUSLOCK\	66 - A2
19 - MRD\	43 - PA.3	67 - A1
20 - RST\	44 - PA.2	68 - A0
21 - INTP\	45 - TOUT2	69 - PA.1
22 - RSTOUT\	46 - TCTL2	70 - PA.0
23 - CLKOUT	47 - TCLK	71 - RL\
24 - BUFEN\	48 - INTAK\/TOUT1/	

DS2340(T) PIN DESCRIPTION - COMMON FOR SIDE A OR B Table 3

NAME	DESCRIPTION	NAME	DESCRIPTION
V_{cc}	+5V Power Supply Input	NMI	Non-Maskable Interrupt
GND	Ground		Input to V40
X1	Crystal Oscillator Input	INTP1	Interrupt Input 1 to V40
X2	Crystal Oscillator Output	INTP2	Interrupt Input 2 to V40
A16-A8	V40 Address Bus Outputs	INTP3	Interrupt Input 3 to V40
AD7-AD0	V40 Mux. Address/Data	INTP4	Interrupt Input 4 to V40
	Bus; Bidirectional	INTP6	Interrupt Input 6 to V40
MRD\	V40 Memory Read Output	PA.3-0	DS5340 Port A Bits 1 and 0;
MWR\	V40 Memory Write Output		Bidirectional
IOR\	V40 I/O Read Output	RL\	DS5340 Reload Input
IOWR\	V40 I/O Write Output	INTP\	DS1283 INTP\ Output;
CE2\-CE4\	DS5340 Chip Enable Outputs		Open-Drain
PCE2\	DS5340 Peripheral Chip	TCLK	V40 Timer Clock Input
	Enable Output	TCTL2	V40 Timer/Counter 2
RST\	System Reset Input		Control Input
TXD	V40 Transmit Data Output	TOUT2	V40 Timer/Counter 2 Output
RXD	V40 Receive Data Input	INTAK\	V40 Interrupt Acknowledge
		/ TOUT1	/ Timer 1 Output
		/SRDY\	/ Serial Ready

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DS2340(T) PIN DESCRIPTION - UNIQUE TO SIDE A Table 4

NAME	DESCRIPTION
ASTB	V40 Address Strobe
PA7-PA4	DS5340 Port A bits 7-2; Bidirectional
PB7-PB0	DS5340 Port B; Bidirectional
PC7-PC0	DS5340 Port C; Bidirectional
IBR\	Interrupt Buffer Ready status output

DS2340(T) PIN DESCRIPTION - UNIQUE TO SIDE B Table 5

NAME	DESCRIPTION
A19-A17	Demultiplexed V40 AddressOutput Lines
A7-A0	Demultiplexed V40 Address Output Lines
RSTOUT\	V40 Reset Output
CLKOUT	V40 Clock Output
BUFEN\	V40 Buffer Enable Output
BUFR\W	V40 Buffer Read/Write Output
REFRQ\	V40 Refresh Request Output
DMARQ0,1	V40 DMA Request Inputs
DMAAK0,1	V40 DMA Acknowledge Outputs
ENDVTC\	V40 End Input/Terminal Count Output
BUSLOCK\	V40 Bus Lock Output

BLOCK DIAGRAM

Figure 1 depicts the DS2340(T). A standard NEC V40 is used as the microprocessor. This component provides the 8086-compatible CPU along with basic I/O functions. The Dallas Semiconductor DS5340 V40 Softener Chip provides nonvolatile control, bootstrap loading capability, and program/data partitioning for the Stik's SRAM. In addition, it provides a clock oscillator, extended function parallel I/O ports, and a watchdog timer.

The DS1283 Watchdog Timekeeper Chip is a self-contained clock/calendar, alarm, and interval timer in a 28-pin SOIC surface mount package. This device is parallel accessed from the V40 and is powered from the V40 Softener's primary V_{cco} output pin.

MICROPROCESSOR

The NEC V40 is a low-power CMOS microprocessor. It is instruction set-compatible with the industry standard 8086. As a result, software for the DS2340(T) is written in the native instruction set of the IBM PC, and the PC can serve as a platform for software development. In addition to the CPU functions, the V40 provides serial I/O, timer/counters, and interrupt inputs. The NEC data sheet for this device should be consulted for full operational details.

DS5340 V40 SOFTENER CHIP

The DS5340 makes possible NV SRAM management, serial bootstrap loading, crashproof operation, and watchdog timer features of the DS2340(T). For complete operational information on this device, the user should consult the DS53xx Micro Softener Chips data sheet and the DS5340 V40 Softener Chip data sheet. The features of the DS5340 that relate to the Flip Stik are described on the following pages.

DS2340(T) BLOCK DIAGRAM Figure 1

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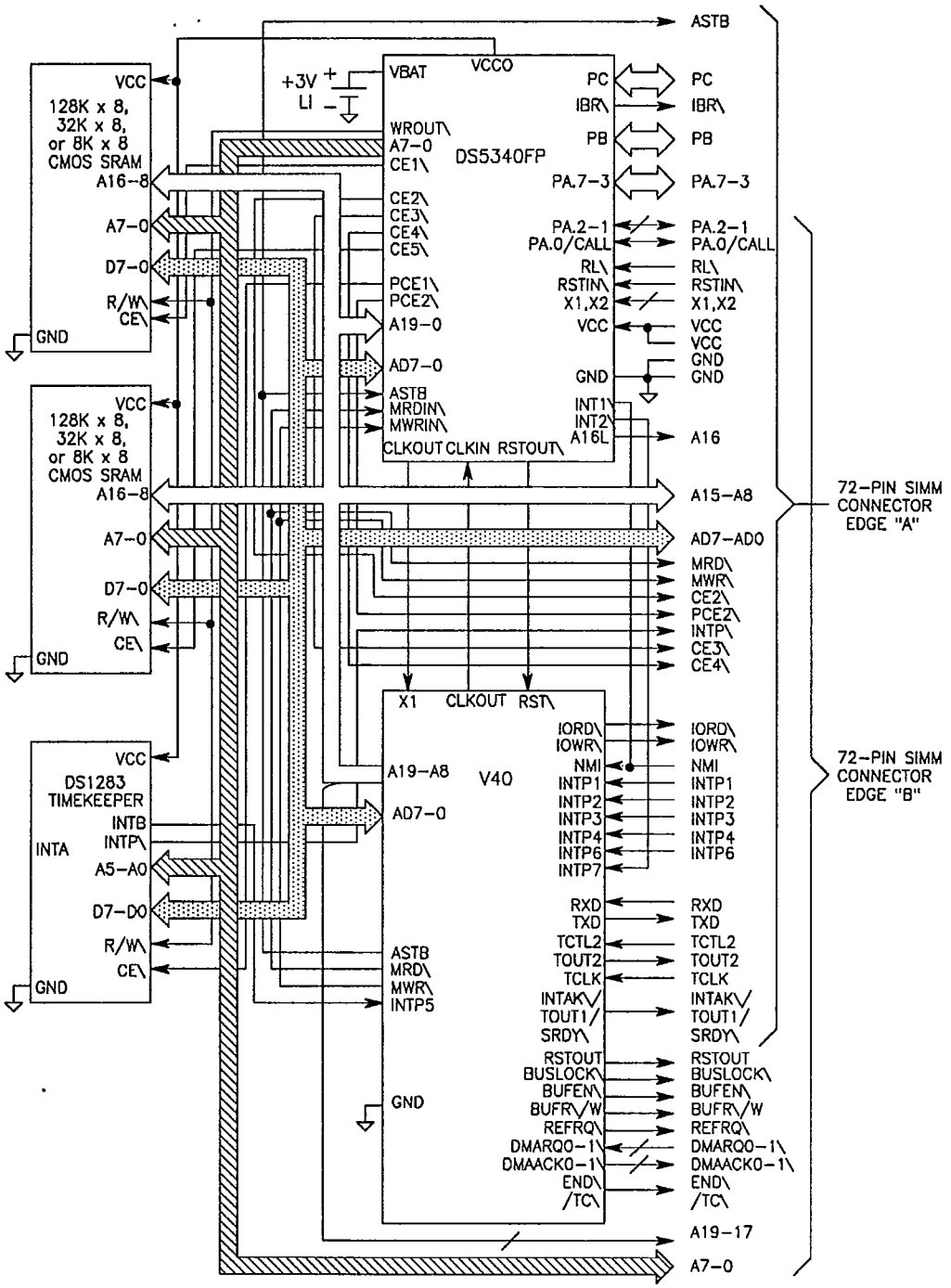

DS2340 MODE 0 MEMORY MAPS Figure 2

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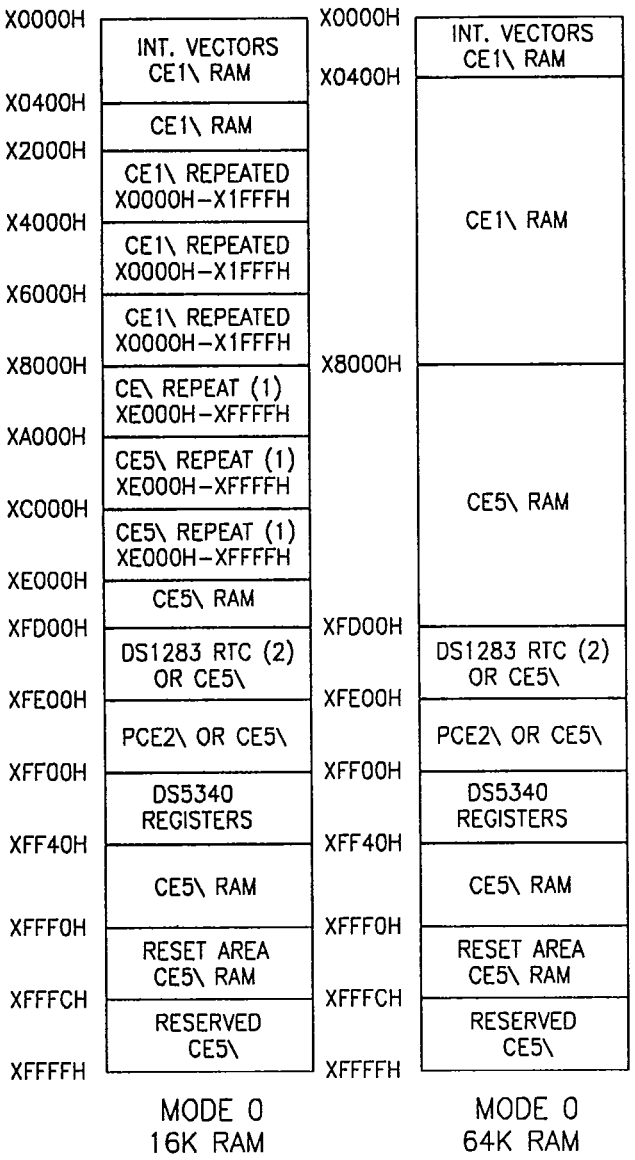

LEGEND:
(1) ONLY CE5\ ADDRESS SPACE IS REPEATED IN THESE AREAS – NOT PCE1\ OR PCE2\
(2) ACCESSIBLE VIA PCE3\ DS2340T

DS2340 MODES 1, 2, 3 AND 4 MEMORY MAPS Figure 3

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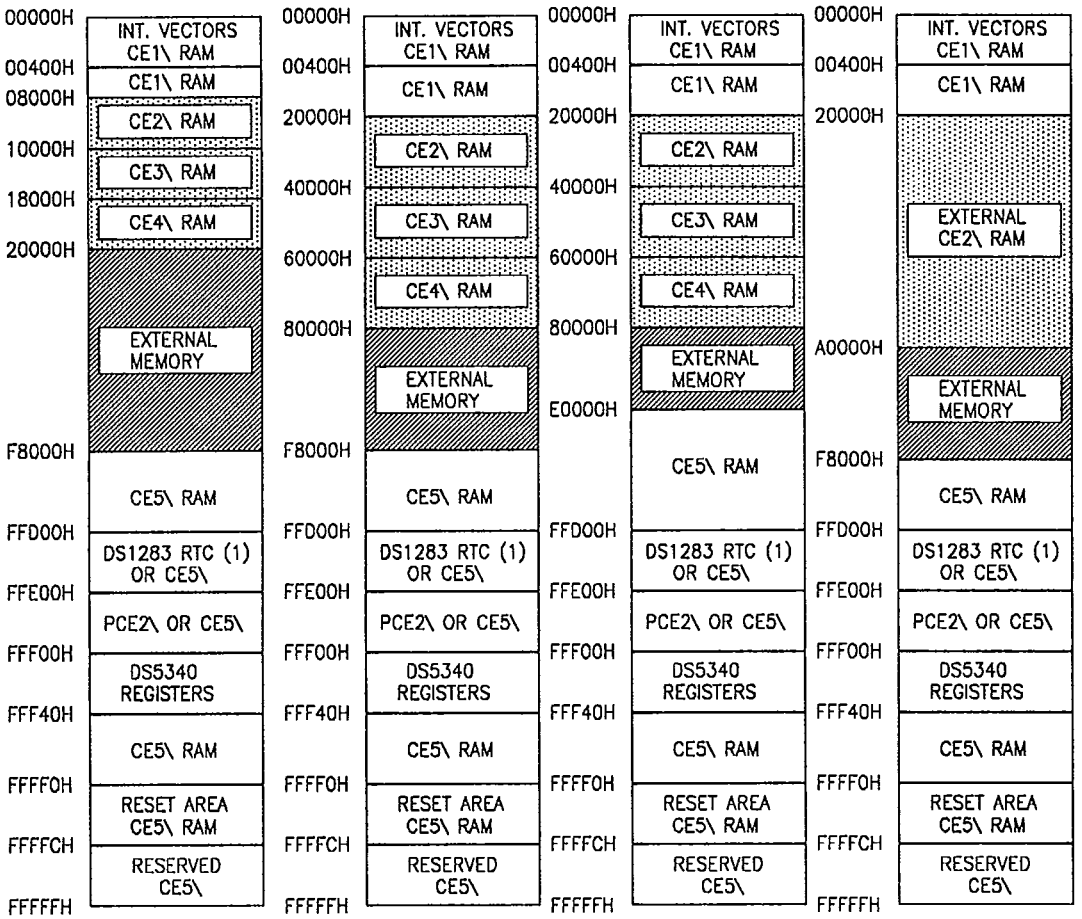

LEGEND: ☐ CEn\ CONTROL ▒ CEn\ DECODED EXTERNAL ▨ EXTERNAL MEMORY – NOT DECODED BY DS5340 (1) ACCESSIBLE VIA PCE3\ DS2340T

MEMORY MAP

The memory map for the DS2340(T) is largely determined by the mode selection within the DS5340 during serial bootstrap loading. The five memory map modes implemented by the V40 Softener Chip are documented in that data sheet.

Versions of the DS2340(T) are available with either 16K, 64K, 160K, or 256K bytes of nonvolatile SRAM. The following discussion describes each of the five operating modes in terms of the typical memory size version for which they would be used in the DS2340(T). Figures 2 and 3 illustrate the resulting memory maps for these typical configurations.

Mode 0 would most likely be selected for a Soft V40 Flip Stik as a single-board system with either 16K bytes or 64K bytes of onboard nonvolatile SRAM. Chip enable outputs CE1\ and CE5\ are each activated for any memory access in the 32K byte ranges of X0000H - X7FFFH and X8000H - XFFFFH, respectively. The memory maps for Mode 0 on a DS2340(T) are illustrated in Figure 2. When a 16K byte version of the DS2340 is used, CE1\ and CE5\ are each connected to an 8K x 8 RAM. Since CE1\ and CE5\ are enabled on 32K byte boundaries, the 8K x 8 RAM space will be replicated four times for each chip enable signal, as shown in Figure 2.

Mode 1 would most likely be selected for a DS2340(T) populated with 64K bytes of NV SRAM in a system requiring offboard expansion. In this configuration, CE1\ and CE5\ would each control one of the two onboard 32K x 8 SRAMs. CE2\, CE3\, and CE4\ would each enable an offboard 32K x 8 memory space. This configuration is illustrated in Figure 3.

Modes 2 and 4 would typically be used for a DS2340(T) populated with 160K bytes of nonvolatile SRAM. In both modes, CE1\ and CE5\ would control the onboard 128K x 8 and 32K x 8 memories, respectively. In Mode 2, CE2\, CE3\, and CE4\ each control an offboard 128K x 8 memory space. In Mode 5, CE2\ controls an offboard 512K x 8 space while CE3\ and CE4\ are always disabled. These configurations are also illustrated in Figure 3.

Mode 3 would most likely be selected for a Flip Stik populated with a full 256K bytes of nonvolatile SRAM. CE1\ and CE5\ each control one of the onboard 128K x 8 SRAMs. CE2\, CE3\, and CE4\ each control an external 128K x 8 memory space as shown in Figure 3.

DS2340(T) PIN FUNCTIONS

As shown in the package outline diagram, the DS2340(T) offers two SIMM card-edges to support single-board and expanded operations. These connectors appear on opposite sides of the card and are designated as card edge A and card edge B. These designators are marked on the Stik PC board itself. This scheme allows the Flip Stik to be installed into a 72-pin SIMM connector in one of two ways to support either single-board or expanded operation.

As illustrated in Figure 1, the pinouts on both card edges support the major functions supplied by the DS5340 and the V40. These functions include the V40's non-multiplexed address lines A15-A8 and multiplexed address/data bus AD7-0, as well as the memory and I/O control lines. Also included are the V40's serial port and counter/timer I/O lines and all of its external interrupt input lines except for INTP5 and INTP7. These two lines are dedicated to the onboard DS1283 Watchdog Timekeeper Chip and V40 Softener Chip, respectively. Both card edges also bring out three lines from the DS5340's Port A as well as its crystal inputs, the Reload pin, its CE2\-CE4\ signals for interface to external memory, and its latched A16 address line from the V40.

In single-board operation using card edge A, the DS2340(T) offers a total of three parallel I/O ports. Port A allows each pin to serve as an interrupt input. Ports B and C can be configured either as parallel I/O or as a high-speed interface to allow the Flip Stik to act as a peripheral controller to a host microprocessor system. Card edge A also supports some offboard expansion capability. The ASTB pin is brought out so that the AD7-AD0 lines can be demultiplexed. For expanded operation, card edge B supports all of the 20 address lines as well as DMA handshake and bus control lines.

ORDERING INFORMATION

The following versions of the DS2340(T) are available as standard products from Dallas Semiconductor:

PART #	TIME-KEEPER	RAM	CLOCK
DS2340 16A	No	16K x 8	8 MHz
DS2340 64A	No	64K x 8	8 MHz
DS2340T 64-B	Yes	64K x 8	10 MHz
DS2340T 256-B	Yes	256K x 8	10 MHz

Please contact Dallas Semiconductor for ordering information on other configurations of the DS2340.

FOR FURTHER INFORMATION

Complete technical specifications for the DS5340 as well as other versions of the Micro Softener and Soft Stik products are available on request from Dallas Semiconductor.

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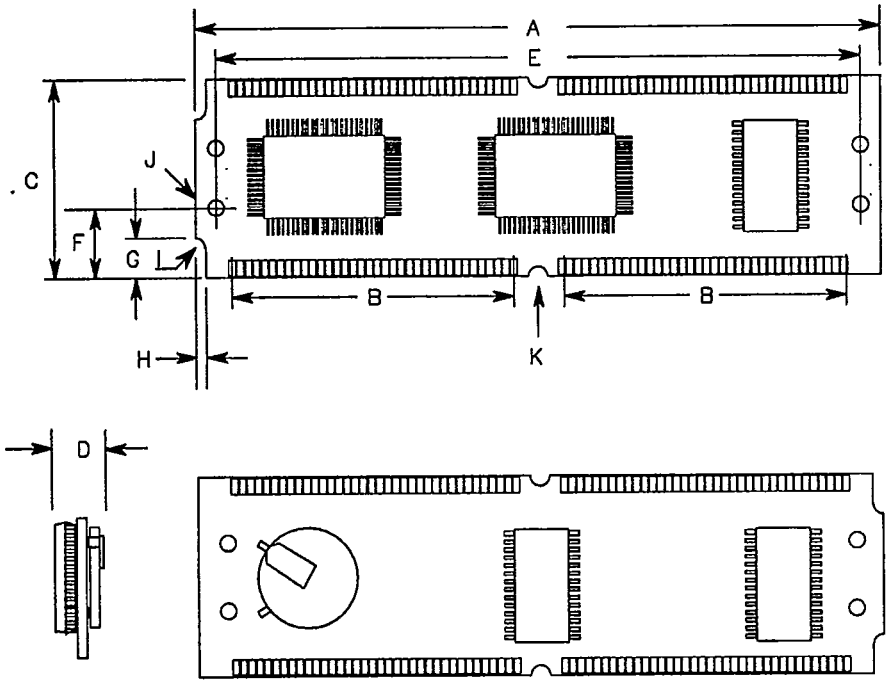
DS2340(T)
Soft V40 Flip Stik



DIM.	INCHES	MM
A	4.250	107.95
B	1.750	44.45
C	1.250	31.75
D	0.472	12.00
E	3.984	101.19
F	0.400	10.16
G	0.250	6.35
H	0.080	2.03
I	R .062	R 1.57
J	D 0.125	D 3.18
K	R .062	R 1.57