

# 82C284

T-52-19

Clock Driver and Ready Interface for iAPX 286 Processors

PRELIMINARY

## DISTINCTIVE CHARACTERISTICS

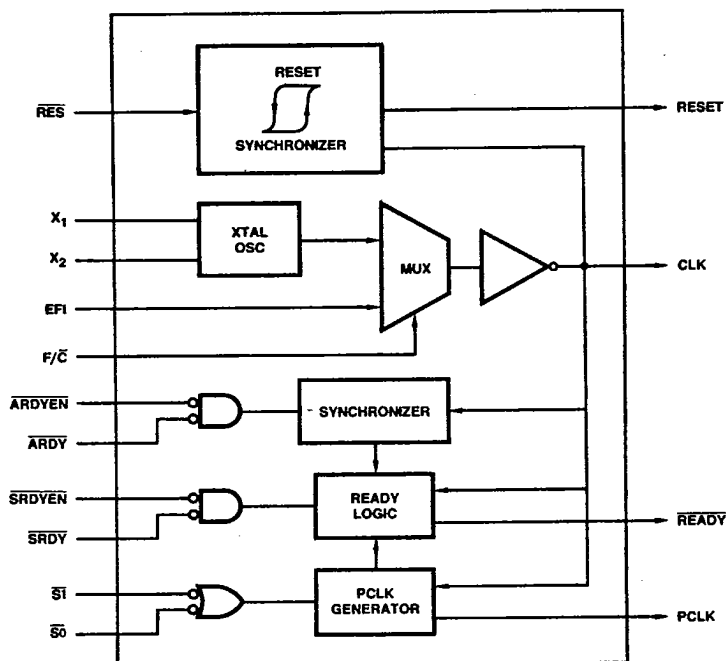
- Generates system clock for iAPX 286 processors
- Uses crystal or TTL signal for frequency source
- Provides local  $\overline{\text{READY}}$  and Multibus\*  $\overline{\text{READY}}$  synchronizer
- Functionally identical to bipolar 82284
- Generates system reset output from Schmitt Trigger input
- 18-pin DIPs
- Single +5-volt power supply
- Low-power operation

## GENERAL DESCRIPTION

The 82C284 is a clock generator/driver which provides clock signals for iAPX 286 processors and support components.

The device contains logic to supply  $\overline{\text{READY}}$  to the CPU from either asynchronous or synchronous sources. It also generates a synchronous reset signal from an asynchronous input with hysteresis.

## BLOCK DIAGRAM



BD005980

\*Multibus is a registered trademark of Intel Corporation.

Order #07747A

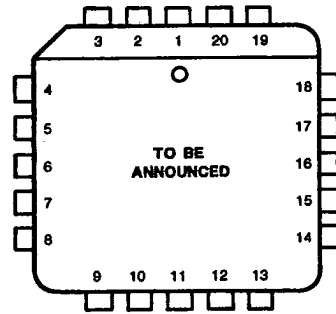
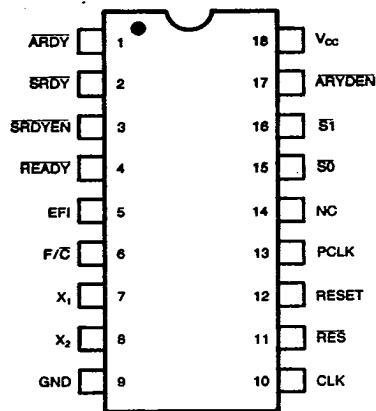
82C284

Advanced Micro Devices

February 1986

CONNECTION DIAGRAMS  
Top View

T-52-19

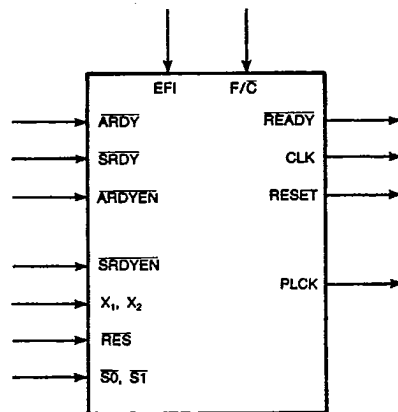


CD009270

CD009240

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002260

VCC = Power Supply  
GND = Ground

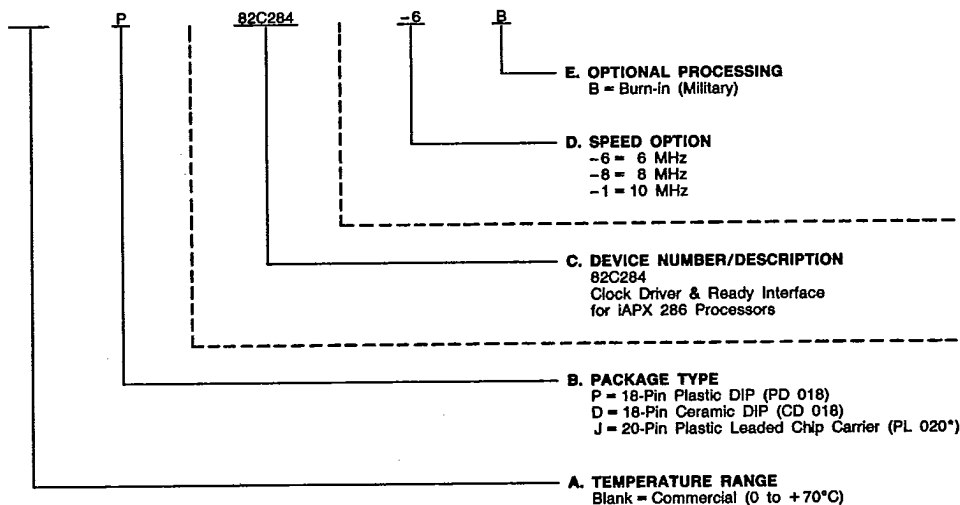
# ORDERING INFORMATION

T-52-19

## Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- A. Temperature Range
- B. Package Type
- C. Device Number
- D. Speed Option
- E. Optional Processing



\*To Be Announced.

| Valid Combinations |        |                                 |
|--------------------|--------|---------------------------------|
| P, D               | 82C284 | -6, -6B,<br>-8, -8B,<br>-1, -1B |

## Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

## PIN DESCRIPTION

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**ARDY Asynchronous Ready (Input, Active LOW)**

ARDY is used to terminate the current bus cycle. The ARDY input is qualified by ARDYEN. Inputs to ARDY may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.

**SRDY Synchronous Ready (Input, Active LOW)**

SRDY is used to terminate the current bus cycle. The SRDY input is qualified by the SRDYEN input. Setup and hold times must be satisfied for proper operation.

**SRDYEN Synchronous Ready Enable (Input, Active LOW)**

SRDYEN qualifies SRDY. SRDYEN selects SRDY as the source for READY to the CPU for the current bus cycle. Setup and hold times must be satisfied for proper operation.

**READY Ready (Output, Active LOW)**

READY signals the current bus cycle is to be completed. The SRDY, SRDYEN, ARDY, ARDYEN, S<sub>0</sub>, S<sub>1</sub>, and RES inputs control READY as explained later under Functional Description. READY is an open-collector output requiring an external 910-ohm pull-up resistor.

**EFI External Frequency In (Input)**

The EFI input drives CLK when F/C is strapped HIGH. The EFI-input frequency must be twice the processor's internal-clock frequency.

**F/C Frequency/Crystal Select (Input)**

F/C is a strapping option used to select the source for the CLK output. When F/C is strapped LOW, the internal crystal drives CLK. When F/C is strapped HIGH, the EFI input drives the CLK output.

**X<sub>1</sub>, X<sub>2</sub> Crystal In (Input)**

These are the pins to which a parallel-resonant, fundamental-mode crystal is attached for the internal oscillator. When F/C is strapped LOW, the oscillator will drive the CLK output at the crystal frequency. The crystal frequency must be twice the processor's internal-clock frequency.

**CLK System Clock (Output)**

CLK output is used by the processor and any support devices which must be synchronized with the processor. The frequency of the CLK output is twice the processor's internal-clock frequency. CLK can drive both TTL- and MOS-level inputs.

**RES Reset In (Input, Active LOW)**

RES generates the system reset signal, RESET. Signals to RES may be applied asynchronously to CLK. A Schmitt Trigger input is provided on RES so that an RC circuit can be used to provide a time delay. Setup and hold times are given to assure a guaranteed response to synchronous inputs.

**RESET Reset (Output, Active HIGH)**

RESET is derived from the RES input. RESET is used to force the system into an initial state. When RESET is active, READY will be active (LOW).

**PCLK Peripheral Clock (Output)**

PCLK is an output which provides a 50% duty cycle clock with one-half the frequency of CLK. PCLK will be in phase with the processor's internal clock following the first bus cycle after the processor has been reset.

**S<sub>0</sub>, S<sub>1</sub> Status (Input, Active LOW)**

These inputs prepare the 82C284 for a subsequent bus cycle. S<sub>0</sub> and S<sub>1</sub> synchronize PCLK to the internal processor clock and control READY. These inputs have pull-up resistors to keep them HIGH if nothing is driving them. Setup and hold times must be satisfied for proper operation.

**ARDYEN Asynchronous Ready Enable (Input, Active LOW)**

ARDYEN qualifies the ARDY input. ARDYEN selects ARDY as the source of READY for the current bus cycle. Inputs to ARDYEN may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.

## FUNCTIONAL DESCRIPTION

The 82C284 generates the clock, ready, and reset signals required for iAPX 286 processors and support components. The 82C284 is packaged in 18-pin plastic and ceramic DIPs and contains a crystal-controlled oscillator, MOS clock generator, peripheral clock generator, Multibus ready-synchronization logic, and reset-generation logic.

**Clock Generator**

The CLK output provides the basic timing control for an iAPX 286 system. CLK has output characteristics sufficient to drive MOS devices. CLK is generated by either an internal crystal or an external source as selected by the F/C strapping option. When F/C is LOW, the crystal oscillator drives the CLK output. When HIGH, the EFI input drives the CLK output.

The 82C284 provides a second clock output (PCLK) for peripheral devices. PCLK is CLK divided by two. PCLK has a duty cycle of 50% and TTL-output drive characteristics. PCLK is normally synchronized to the internal processor clock.

After reset, the PCLK signal may be out of phase with the internal processor clock. The S<sub>1</sub> and S<sub>0</sub> signals of the first bus cycle are used to synchronize PCLK to the internal processor clock. The phase of the PCLK output changes by extending its

HIGH time beyond one system clock (see Switching Waveforms). PCLK is forced HIGH when either S<sub>0</sub> or S<sub>1</sub> was active (LOW) for the two previous CLK cycles. PCLK continues to oscillate when both S<sub>0</sub> and S<sub>1</sub> are HIGH.

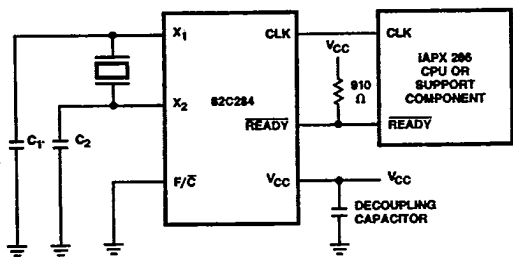
Since the phase of the internal processor clock will not change except during reset, the phase of PCLK will not change except during the first bus cycle after reset.

**Oscillator**

The oscillator circuit of the 82C284 is a linear Pierce oscillator which requires an external parallel-resonant, fundamental-mode crystal. The output of the oscillator is internally buffered. The crystal frequency chosen should be twice the processor's internal-clock frequency. The crystal should have a typical load capacitance of 32 pF.

X<sub>1</sub> and X<sub>2</sub> are the oscillator-crystal connections. For stable operation of the oscillator, two loading capacitors are recommended, as shown in Figure 1. The sum of the board capacitance and loading capacitance should equal the values shown. It is advisable to limit stray board capacitances (not including the effect of the loading capacitors or crystal capacitance) to less than 10 pF between the X<sub>1</sub> and X<sub>2</sub> pins. VCC and GND pins should be decoupled as close to the 82C284 as possible.

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TC003110

Figure 1. Recommended Crystal and Ready Connections\*

\*See Table 1 for capacitor values.

TABLE 1. 82C284 CRYSTAL LOADING CAPACITANCE VALUES

| Crystal Frequency | C <sub>1</sub> Capacitance | C <sub>2</sub> Capacitance |
|-------------------|----------------------------|----------------------------|
| 1 to 8 MHz        | 60 pF                      | 40 pF                      |
| 8 to 16 MHz       | 25 pF                      | 15 pF                      |

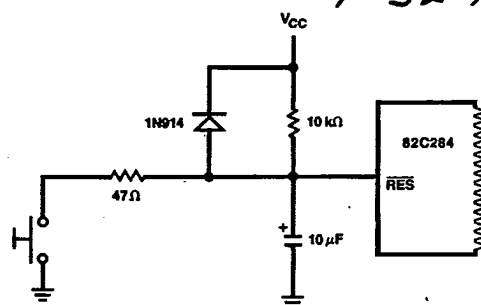
Note: Capacitance values must include stray board capacitance.

### Reset Operation

The reset logic provides the RESET output to force the system into a known, initial state. When the RES input is active (LOW), the RESET output becomes active (HIGH). RES is synchronized internally at the falling edge of CLK before generating the RESET output (see Switching Waveforms). Synchronization of the RES input introduces a one- or two-CLK delay before affecting the RESET output.

At power up, a system does not have a stable V<sub>CC</sub> and CLK. To prevent spurious activity, RES should be asserted until V<sub>CC</sub> and CLK stabilize at their operating values. IAPX 286 processors and support components also require their RESET inputs be HIGH a minimum of sixteen CLK cycles. An RC network (shown in Figure 2) will keep RES LOW long enough to satisfy both needs.

A Schmitt Trigger input with hysteresis on RES assures a single transition of RESET with an RC circuit on RES. The hysteresis separates the input voltage level at which the circuit output switches from HIGH to LOW from the input voltage level at which the circuit output switches from LOW to HIGH. The RES HIGH-to-LOW input-transition voltage is lower than the RES LOW-to-HIGH input-transition voltage. As long as the slope of the RES input voltage remains in the same direction (increasing or decreasing) around the RES input-transition voltage, the RESET output will make a single transition.



TC003100

Figure 2. Typical RC RES Timing Circuit

### Ready Operation

The 82C284 accepts two ready sources for the system-ready signal which terminates the current bus cycle. Either a synchronous ready (SRDY) or asynchronous ready (ARDY) source may be used. Each ready input has an enable (SRDYEN and ARDYEN) for selecting the type of ready source required to terminate the current bus cycle. An address decoder would normally select one of the enable inputs.

READY is enabled (LOW) if either SRDY + SRDYEN = 0, or ARDY + ARDYEN = 0, when sampled by the 82C284 READY-generation logic. READY will remain active for at least two CLK cycles, except when RESET overrides it.

The READY output has an open-collector driver allowing other ready circuits to be wire OR'ed with it, as shown in Figure 1. The READY signal of an IAPX 286 system requires an external 910-ohm,  $\pm 5\%$  pull-up resistor. To force the READY signal inactive (HIGH) at the start of a bus cycle, the READY output floats when either S1 or S0 are sampled LOW at the falling edge of CLK. Two system clock periods are allowed for the pull-up resistor to pull the READY signal to V<sub>IH</sub>. When RESET is active, READY is forced active one CLK later (see Switching Waveforms).

Figure 3 illustrates the operation of SRDY and SRDYEN. These inputs are sampled on the falling edge of CLK when S1 and S0 are inactive and PCLK is HIGH. READY is forced active when both SRDY and SRDYEN are sampled as LOW.

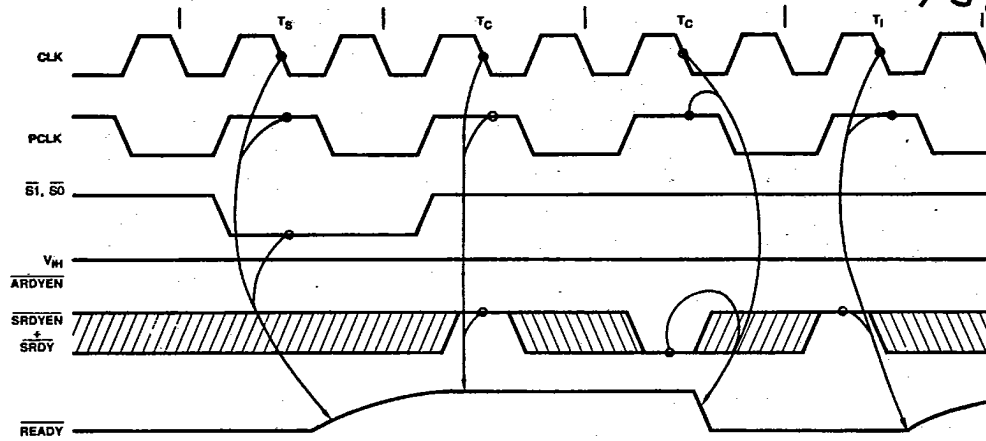
Figure 4 shows the operation of ARDY and ARDYEN. These inputs are sampled by an internal synchronizer at each falling edge of CLK. The output of the synchronizer is then sampled when PCLK is HIGH. If the synchronizer resolved both the ARDY and ARDYEN inputs to have been LOW, READY becomes LOW. When both ARDY and ARDYEN have been resolved as active, the SRDY and SRDYEN inputs are ignored. Either ARDY or ARDYEN must be HIGH at the end of T<sub>S</sub> (see Figure 4).

READY remains active until either S1 or S0 are sampled LOW, or the ready inputs are sampled as inactive.

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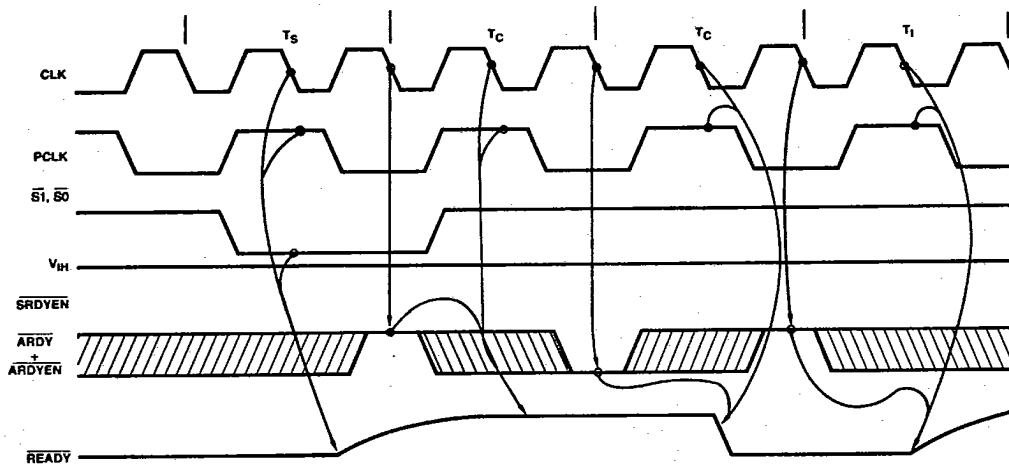
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WF021290

Figure 3. Synchronous Ready Operation



WF021300

Figure 4. Asynchronous Ready Operation

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature ..... -65 to +150°C  
 Ambient Temperature  
   with Power Applied ..... -55 to +125°C  
 DC Supply Voltage  
   with Respect to Ground ..... -0.3 to +7.0 V  
 DC Voltage  
   with Respect to Ground (Any Pin) ..... -0.3 to +7.0 V  
 DC Output Current  
   Into Output (Note 1) ..... +10 mA per pin  
   Out Of Output (Note 2) ..... -10 mA per pin  
 DC Input Current ..... ±10 mA per pin

Notes: 1. Except when powered up with outputs LOW.  
 2. Except when powered up with outputs HIGH.

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

**OPERATING RANGES**

Commercial (C) Devices  
 Temperature (T<sub>A</sub>) ..... 0 to +70°C  
 Supply Voltage (V<sub>CC</sub>) ..... +4.5 to +5.5 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

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**DC CHARACTERISTICS** over operating range unless otherwise specified

| Parameter Symbol  | Parameter Description                 | Test Conditions                                                                    | Min. | Max. | Units  |
|-------------------|---------------------------------------|------------------------------------------------------------------------------------|------|------|--------|
| V <sub>OH</sub>   | Output HIGH Voltage on RESET and PCLK | I <sub>OH</sub> = -1 mA                                                            | 2.4  |      | V      |
| V <sub>OL</sub>   | Output LOW Voltage on RESET and PCLK  | I <sub>OL</sub> = 5 mA                                                             |      | 0.45 | V      |
| V <sub>IH</sub>   | Input HIGH Voltage                    |                                                                                    | 2.0  |      | V      |
| V <sub>IL</sub>   | Input LOW Voltage                     |                                                                                    |      | 0.8  | V      |
| I <sub>IL</sub>   | Input LOW Current                     | V <sub>F</sub> = .45 V                                                             |      | -0.5 | mA     |
| I <sub>IH</sub>   | Input HIGH Current                    | V <sub>R</sub> = V <sub>CC</sub> Max.                                              |      | 50.0 | μA     |
| V <sub>IHR</sub>  | Input HIGH Voltage on RES             |                                                                                    | 2.6  |      | V      |
| V <sub>HYS</sub>  | Input Hysteresis on RES               |                                                                                    | 0.25 |      | V      |
| V <sub>OLR</sub>  | Output LOW Voltage on READY           | I <sub>OL</sub> = 7 mA                                                             |      | 0.45 | V      |
| V <sub>OLC</sub>  | Output LOW Voltage on CLK             | I <sub>OL</sub> = 5 mA                                                             |      | 0.45 | V      |
| V <sub>OHC</sub>  | Output HIGH Voltage on CLK            | I <sub>OH</sub> = -800 μA                                                          | 4.0  |      | V      |
| I <sub>CCSB</sub> | Standby Power Supply Current          | V <sub>CC</sub> = 5.5 V,<br>V <sub>IN</sub> = V <sub>CC</sub> or GND; Outputs open |      |      | μA     |
| I <sub>CCOP</sub> | Operating Power Supply Current        | V <sub>CC</sub> = 5.5 V, Outputs open                                              |      |      | mA/MHz |

**CAPACITANCE\*** (T<sub>A</sub> = 25°C, V<sub>CC</sub> = GND = 0 V, V<sub>IN</sub> = +5 V or GND)

| Parameter Symbol | Parameter Description      | Test Conditions        | Min. | Max. | Units |
|------------------|----------------------------|------------------------|------|------|-------|
| C <sub>I</sub>   | Input Capacitance (Note 1) | F <sub>C</sub> = 1 MHz |      | 10.0 | pF    |

Notes: 1. This specification is provided for reference only.

\* Parameters are not "Tested."

0257525 ADVANCED MICRO DEVICES

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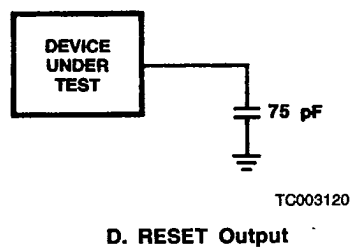
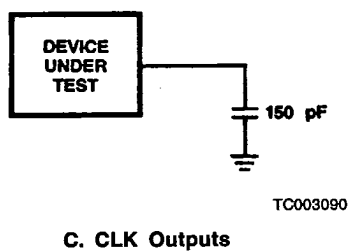
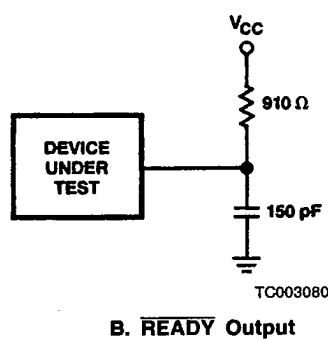
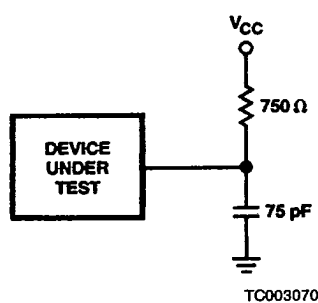
## KEY TO SWITCHING WAVEFORMS

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| WAVEFORM | INPUTS                           | OUTPUTS                                   |
|----------|----------------------------------|-------------------------------------------|
|          | MUST BE STEADY                   | WILL BE STEADY                            |
|          | MAY CHANGE FROM H TO L           | WILL BE CHANGING FROM H TO L              |
|          | MAY CHANGE FROM L TO H           | WILL BE CHANGING FROM L TO H              |
|          | DON'T CARE; ANY CHANGE PERMITTED | CHANGING; STATE UNKNOWN                   |
|          | DOES NOT APPLY                   | CENTER LINE IS HIGH IMPEDANCE "OFF" STATE |

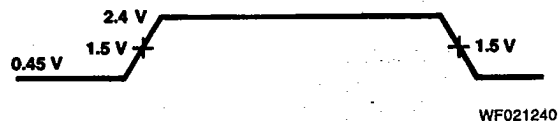
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## SWITCHING TEST CIRCUITS

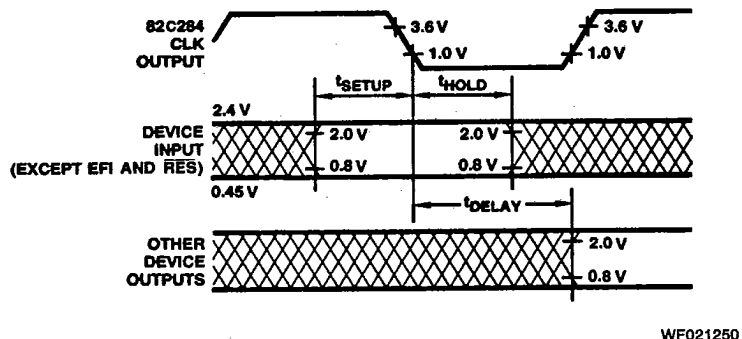


SWITCHING TEST WAVEFORMS

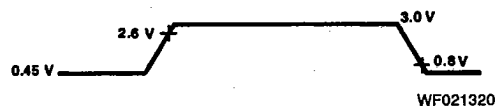
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A. EFI Drive and Measurement Points



B. Setup, Hold, and Delay Time Measurement — General



C. RES Drive and Measurement Points



D. CLK Output Measurement Points

0257525 ADVANCED MICRO DEVICES

76C 21527 D

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

T-52-19

| No. | Parameter Symbol | Parameter Description     | Test Conditions           | 6 MHz               |      | 8 MHz               |      | 10 MHz |      | Units |
|-----|------------------|---------------------------|---------------------------|---------------------|------|---------------------|------|--------|------|-------|
|     |                  |                           |                           | Min.                | Max. | Min.                | Max. | Min.   | Max. |       |
| 1   | t <sub>1</sub>   | EFI-to-CLK Delay          | At 1.5 V (Note 1)         |                     | 35   |                     | 30   |        |      | ns    |
| 2   | t <sub>2</sub>   | EFI LOW Time              | At 1.5 V (Notes 1 & 7)    | 40                  |      | 25                  |      |        |      | ns    |
| 3   | t <sub>3</sub>   | EFI HIGH Time             | At 1.5 V (Notes 1 & 7)    | 35                  |      | 25                  |      |        |      | ns    |
| 4   | t <sub>4</sub>   | CLK Period                |                           | 83                  | 500  | 62                  | 500  |        |      | ns    |
| 5   | t <sub>5</sub>   | CLK LOW Time              | At 1.0 V (Notes 1, 2 & 8) | 20                  |      | 15                  |      |        |      | ns    |
| 6   | t <sub>6</sub>   | CLK HIGH Time             | At 3.6 V (Notes 1, 2 & 8) | 25                  |      | 25                  |      |        |      | ns    |
| 7   | t <sub>7</sub>   | CLK Rise Time             | 1.0 to 3.6 V (Note 1)     |                     | 10   |                     | 10   |        |      | ns    |
| 8   | t <sub>8</sub>   | CLK Fall Time             | 3.6 to 1.0 V (Note 1)     |                     | 10   |                     | 10   |        |      | ns    |
| 9   | t <sub>9</sub>   | Status Setup Time         | (Note 1)                  | 28                  |      | 22                  |      |        |      | ns    |
| 10  | t <sub>10</sub>  | Status Hold Time          | (Note 1)                  | 1                   |      | 1                   |      |        |      | ns    |
| 11  | t <sub>11</sub>  | SRDY or SRDYEN Setup Time | (Note 1)                  | 25                  |      | 17                  |      |        |      | ns    |
| 12  | t <sub>12</sub>  | SRDY or SRDYEN Hold Time  | (Note 1)                  | 0                   |      | 0                   |      |        |      | ns    |
| 13  | t <sub>13</sub>  | ARDY or ARDYEN Setup Time | (Notes 1 & 3)             | 5                   |      | 0                   |      |        |      | ns    |
| 14  | t <sub>14</sub>  | ARDY or ARDYEN Hold Time  | (Notes 1 & 3)             | 30                  |      | 30                  |      |        |      | ns    |
| 15  | t <sub>15</sub>  | RES Setup Time            | (Notes 1 & 3)             | 25                  |      | 20                  |      |        |      | ns    |
| 16  | t <sub>16</sub>  | RES Hold Time             | (Notes 1 & 3)             | 10                  |      | 10                  |      |        |      | ns    |
| 17  | t <sub>17</sub>  | READY Inactive Delay      | At 0.8 V (Note 4)         | 5                   |      | 5                   |      |        |      | ns    |
| 18  | t <sub>18</sub>  | READY Active Delay        | At 0.8 V (Note 4)         | 0                   | 33   | 0                   | 24   |        |      | ns    |
| 19  | t <sub>19</sub>  | PCLK Delay                | (Note 5)                  | 0                   | 45   | 0                   | 45   |        |      | ns    |
| 20  | t <sub>20</sub>  | RESET Delay               | (Note 5)                  | 5                   | 50   | 5                   | 34   |        |      | ns    |
| 21  | t <sub>21</sub>  | PCLK LOW Time             | (Notes 5 & 6)             | t <sub>4</sub> - 20 |      | t <sub>4</sub> - 20 |      |        |      | ns    |
| 22  | t <sub>22</sub>  | PCLK HIGH Time            | (Notes 5 & 6)             | t <sub>4</sub> - 20 |      | t <sub>4</sub> - 20 |      |        |      | ns    |

Notes: 1. CLK loading: C<sub>L</sub> = 150 pF.2. With the internal crystal oscillator using recommended crystal and capacitive loading, or with the EFI input meeting specifications t<sub>2</sub> and t<sub>3</sub>. Use a parallel-resonant, fundamental-mode crystal. The recommended crystal loading for CLK frequencies of 8-16 MHz are 25 pF from pin X<sub>1</sub> to ground, and 15 pF from pin X<sub>2</sub> to ground. These recommended values are ±5 pF and include all stray capacitance. Decouple V<sub>CC</sub> and GND as close to the 82C284 as possible.

3. This is an asynchronous input. This specification is given for testing purposes only, to assure recognition at specific CLK edge.

4. READY loading: I<sub>OL</sub> = 7 mA, C<sub>L</sub> = 150 pF. In system application, use 910-ohm ±5% pull-up resistor to meet 80286 timing requirements. For systems which operate faster than 10 MHz, care should be taken to minimize capacitive loading on READY. The user must insure the RC time constant allows this pin to be pulled HIGH in two clock cycles.5. PCLK and RESET loading: C<sub>L</sub> = 75 pF. PCLK also has 750-ohm pull-up resistor.6. t<sub>4</sub> refers to any allowable CLK period.

7. When driving the 82C284 with EFI, provide minimum EFI HIGH and LOW times as follows:

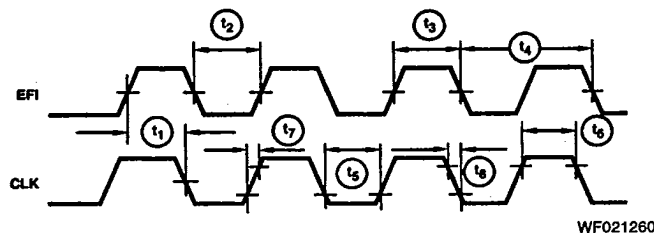
| CLK Output Frequency           | 8 MHz CLK | 12 MHz CLK | 16 MHz CLK* |
|--------------------------------|-----------|------------|-------------|
| Minimum required EFI HIGH Time | 52 ns     | 35 ns      | 25 ns       |
| Minimum required EFI LOW Time  |           | 40 ns      |             |

\*At CLK frequencies above 12 MHz, CLK output HIGH and LOW times are guaranteed only when using a crystal with recommended capacitive loading per Table 1, not when driving component from EFI. All features of the 82C284 remain functional whether EFI or a crystal is used to drive the 82C284.

8. When using a crystal (with recommended loading capacitance per Table 1) appropriate for the speed of the 80286, CLK output HIGH and LOW times are guaranteed to meet 80286 requirements.

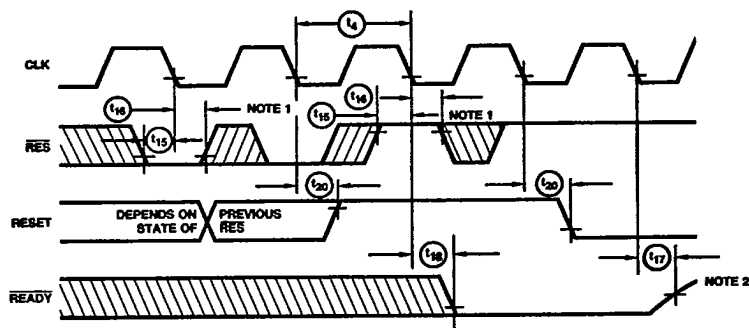
SWITCHING WAVEFORMS

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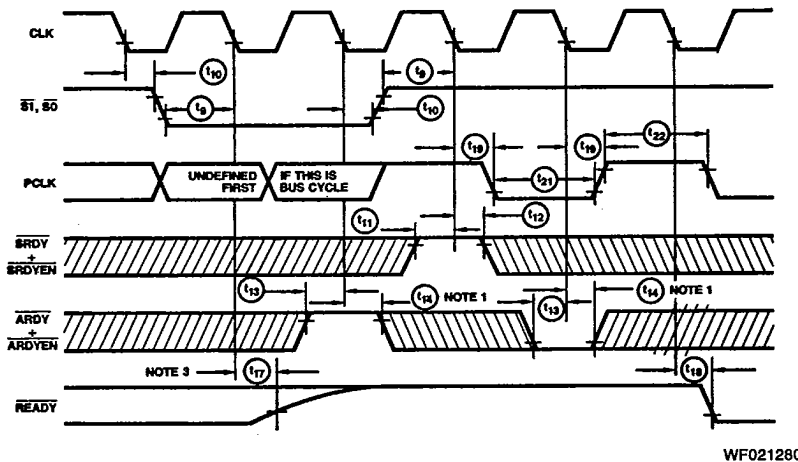
CLK as a Function of EFI

Note: The EFI input LOW and HIGH times as shown are required to guarantee the CLK LOW and HIGH times shown.



RESET and READY Timing as a Function of RES with S1 and S0 HIGH

Notes: 1. This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.  
2. Tie 910-ohm  $\pm 5\%$  pull-up resistor to the READY output. This LOW-to-HIGH transition depends on the state of ARDY, ARDYEN, SRDY, and SRDYEN.



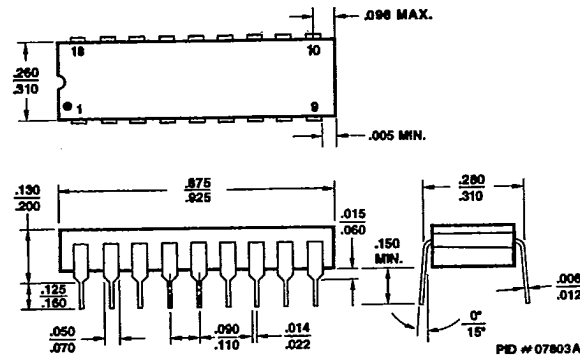
READY and PCLK Timing with RES HIGH

Notes: 1. This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.  
2. Tie 910-ohm  $\pm 5\%$  pull-up resistor to the READY output.

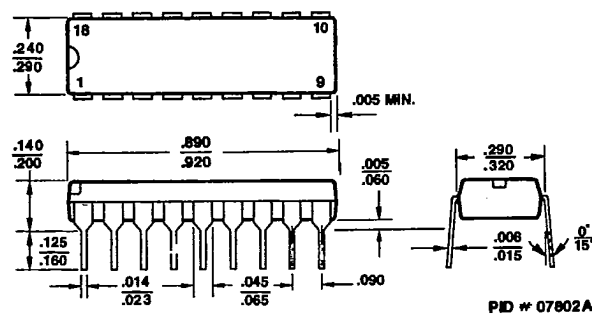
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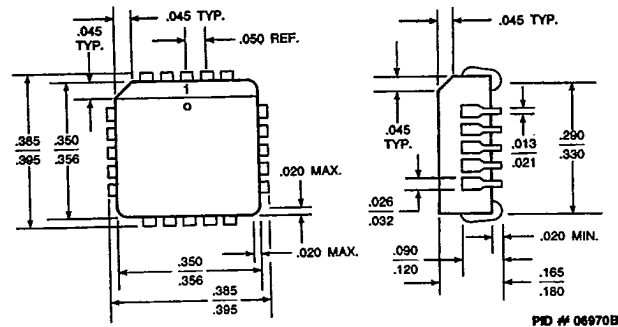
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PD 018



PL 020\*



\* Preliminary. Subject to Change.

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