



CYPRESS
SEMICONDUCTOR

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PRELIMINARY

T-46-19-07

CY7C374

128-Macrocell Flash PLD

Features

- 128 macrocells in eight logic blocks
- 64 I/O pins
- 6 dedicated inputs including 4 clock pins
- No hidden delays
- High speed
 - $t_{PD} = 12$ ns
 - $t_S = 9$ ns
 - $t_{CO} = 9$ ns
- Electrically alterable Flash technology
- Available in 84-pin PLCC, CLCC, and CPGA packages
- Pin compatible with the CY7C373

Functional Description

The CY7C374 is a Flash Erasable Programmable Logic Device (EPLD) and is part of the FLASH370 family of high-density, high-speed PLDs. Like all members of the FLASH370 family, the CY7C374 is designed to bring the ease of use and high

performance of the 22V10 to high-density PLDs.

The 128 macrocells in the CY7C374 are divided between eight logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C374 is rich in I/O resources. Every two macrocells in the device feature an associated I/O pin, resulting in 64 I/O pins on the CY7C374. In addition, there are four dedicated inputs and two input/clock pins.

Finally, the CY7C374 features a very simple timing model. Unlike other high-density PLD architectures, there are no hidden

speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C374 remain the same.

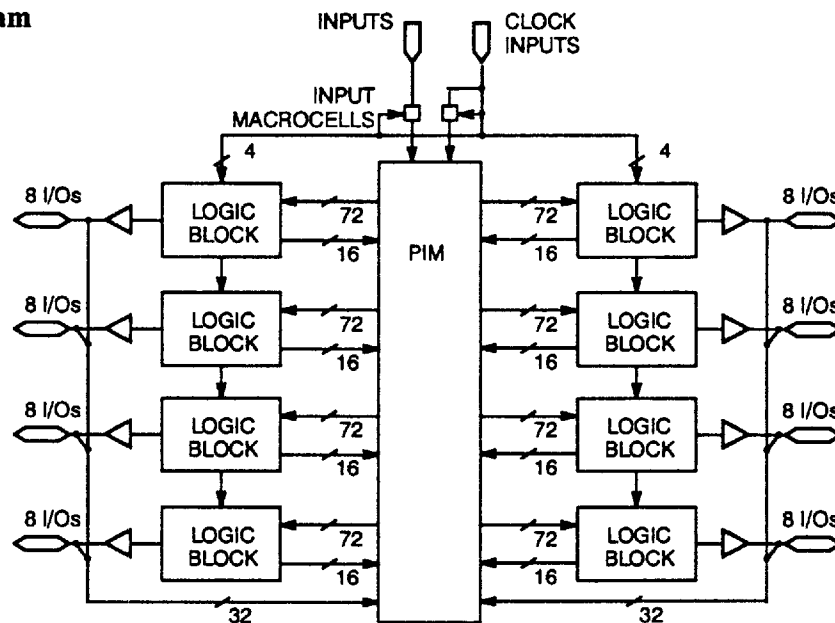
Logic Block

The number of logic blocks distinguishes the members of the FLASH370 family. The CY7C374 includes eight logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370 logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows for very complex functions to be implemented in single passes through the device.

Logic Block Diagram



7C374-1

Selection Guide

| | | 7C374-12 | 7C374-15 | 7C374-20 |
|---|------------|----------|----------|----------|
| Maximum Propagation Delay t_{PD} (ns) | | 12 | 15 | 20 |
| Maximum Standby Current, I_{CC1} (mA) | Commercial | 300 | 300 | 300 |
| | Military | | 370 | 370 |
| Maximum Operating Current, I_{CC2} (mA) | Commercial | 330 | 330 | 330 |
| | Military | | 400 | 400 |

Shaded area contains advanced information.



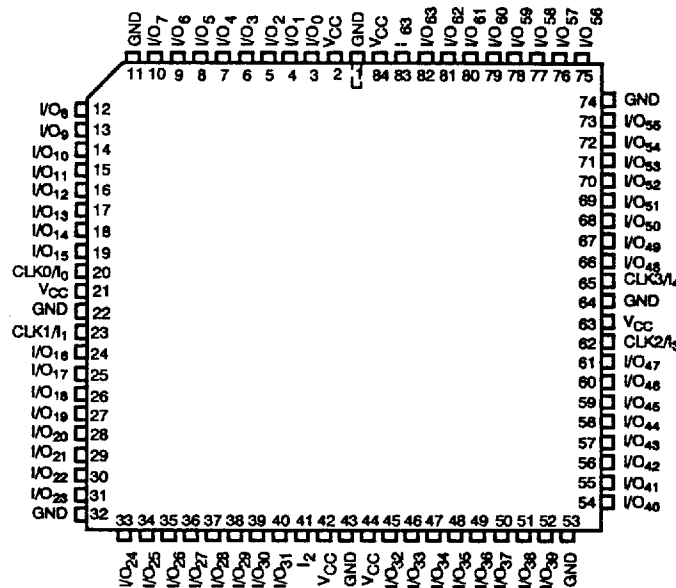
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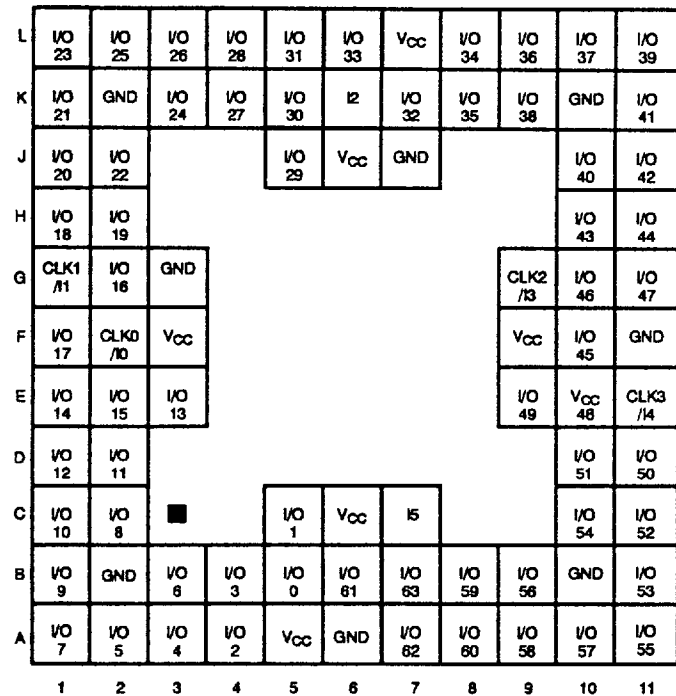
Pin Configurations

PLCC/CLCC
Top View



7C374-3

PGA
Bottom View



7C374-2

Functional Description (continued)

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product terms to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370 PLDs. Note that product term allocation is handled by software and is invisible to the user.

I/O Macrocell

Half of the macrocells on the CY7C374 have I/O pins associated with them. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The I/O macrocell includes a register that can be optionally bypassed, polarity control over the input sum-term, and two global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Buried Macrocell

The buried macrocell is very similar to the I/O macrocell. Again, it includes a register that can be configured as combinatorial, as a D flip-flop, a T flip-flop, or a latch. The clock for this register has the same options as described for the I/O macrocell. One difference on the buried macrocell is the addition of input register capability. The user can program the buried macrocell to act as an input register whose input comes from the I/O pin associated with the neigh-

boring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the eight logic blocks on the CY7C374 to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Development Tools

Development software for the CY7C374 is available from Cypress's *Warp2* and *Warp3* software packages. Both of these products are based on the IEEE standard VHDL language. Cypress also supports third-party vendors such as ABEL, CUPL, and LOG/iC. Please contact your local Cypress representative for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

| | |
|--|------------------|
| Storage Temperature | - 65°C to +150°C |
| Ambient Temperature with | |
| Power Applied | - 55°C to +125°C |
| Supply Voltage to Ground Potential | - 0.5V to +7.0V |
| DC Voltage Applied to Outputs | |
| in High Z State | - 0.5V to +7.0V |
| DC Input Voltage | - 0.5V to +7.0V |
| DC Program Voltage | 12.5V |
| Output Current into Outputs | 16 mA |
| Static Discharge Voltage | >2001V |
| (per MIL-STD-883, Method 3015) | |
| Latch-Up Current | >200 mA |



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Operating Range

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| Range | Ambient Temperature | V _{CC} |
|-------------------------|---------------------|-----------------|
| Commercial | 0°C to +70°C | 5V ± 5% |
| Military ^[1] | -55°C to +125°C | 5V ± 10% |

Electrical Characteristics Over the Operating Range^[2]

| Parameter | Description | Test Conditions | 7C374 | | Unit |
|------------------|---|---|-------|------|------|
| | | | Min. | Max. | |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min. I _{OH} = -3.2 mA (Com'l/Ind) I _{OL} = -2.0 mA (Mil) | 2.4 | | V |
| | | | | | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min. I _{OH} = 16 mA (Com'l/Ind) I _{OL} = 12 mA (Mil) | | 0.5 | V |
| | | | | | V |
| V _{IH} | Input HIGH Voltage | | 2.0 | 7.0 | V |
| V _{IL} | Input LOW Voltage | | -0.5 | 0.8 | V |
| I _{IX} | Input Load Current | GND ≤ V _I ≤ V _{CC} | -10 | +10 | μA |
| I _{OZ} | Output Leakage Current | GND ≤ V _O ≤ V _{CC} , Output Disabled | -50 | +50 | μA |
| I _{OS} | Output Short Circuit Current ^[3] | V _{CC} = Max., V _{OUT} = 0.5V | -30 | -90 | mA |
| I _{CC1} | Power Supply Current (Standby) | V _{CC} = Max., I _{OUT} = 0 mA, f = 0 MHz, V _{IN} = GND, V _{CC} | Com'l | 300 | mA |
| | | | Mil | 370 | |
| I _{CC2} | Power Supply Current | V _I = V _{CC} or GND, f = 40 MHz | Com'l | 330 | mA |
| | | | Mil | 400 | |

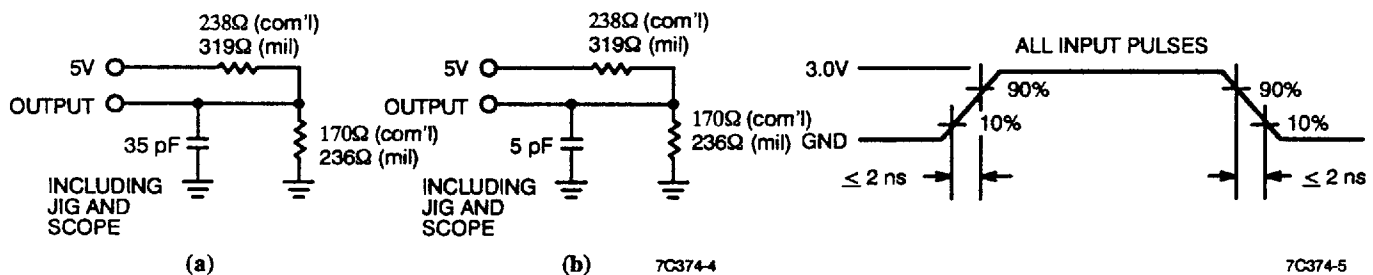
Capacitance^[4]

| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|--------------------|--------------------------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 2.0V at f = 1 MHz | 10 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 2.0V at f = 1 MHz | 12 | pF |

Notes:

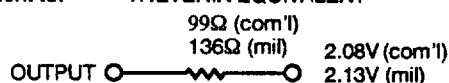
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to:

THÉVENIN EQUIVALENT





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Switching Characteristics Over the Operating Range^[5]

| Parameter | Description | 7C374-12 | | 7C374-15 | | 7C374-20 | | Unit |
|---|---|----------|------|----------|------|----------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Combinatorial Mode Parameters | | | | | | | | |
| t _{PD} | Input to Combinatorial Output | | 12 | | 15 | | 20 | ns |
| t _{PDL} | Input to Output Through Transparent Input or Output Latch | | 14 | | 17 | | 22 | ns |
| t _{PDLL} | Input to Output Through Transparent Input and Output Latches | | 16 | | 19 | | 24 | ns |
| t _{EA} | Input to Output Enable | | 16 | | 19 | | 24 | ns |
| t _{ER} | Input to Output Disable | | 16 | | 19 | | 24 | ns |
| Input Registered/Latched Mode Parameters | | | | | | | | |
| t _{WL} | Clock or Latch Enable Input LOW Time | 5 | | 6 | | 8 | | ns |
| t _{WH} | Clock or Latch Enable Input HIGH Time | 5 | | 6 | | 8 | | ns |
| t _{IS} | Input Register or Latch Set-Up Time | 2 | | 3 | | 4 | | ns |
| t _{IH} | Input Register or Latch Hold Time | 2 | | 3 | | 4 | | ns |
| t _{ICO} | Input Register Clock or Latch Enable to Combinatorial Output | | 16 | | 19 | | 24 | ns |
| t _{ICOL} | Input Register Clock or Latch Enable to Output Through Trans- parent Output Latch | | 18 | | 21 | | 26 | ns |
| f _{MAX1} | Maximum Frequency of (2) CY7C374s in Input Registered Mode (Lesser of 1/(t _{ICO} + t _{IS}) and 1/(t _{WL} + t _{WH})) | 55.5 | | 45.5 | | 35.7 | | MHz |
| f _{MAX2} | Maximum Frequency Data Path in Input Registered/Latched Mode (Least of 1/t _{ICO} , 1/(t _{WL} + t _{WH}), 1/(t _{IS} + t _{IH})) | 62.5 | | 52.6 | | 41.7 | | MHz |
| Output Registered/Latched Mode Parameters | | | | | | | | |
| t _{CO} | Clock or Latch Enable to Output | | 9 | | 12 | | 15 | ns |
| t _S | Set-Up Time from Input to Clock or Latch Enable | 9 | | 12 | | 15 | | ns |
| t _H | Register or Latch Data Hold Time | 0 | | 0 | | 0 | | ns |
| t _{CO2} | Output Clock or Latch Enable to Output Delay (Through Memory Array) | | 16 | | 19 | | 24 | ns |
| t _{SCS} | Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array) | 12 | | 15 | | 20 | | ns |
| t _{SL} | Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable | 12 | | 15 | | 20 | | ns |
| t _{HL} | Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable | 0 | | 0 | | 0 | | ns |
| f _{MAX3} | Maximum Frequency of (2) CY7C374s in Output Registered Mode (Lesser of 1/(t _{CO} + t _S) and 1/(t _{WL} + t _{WH})) | 55.5 | | 41.7 | | 33.3 | | MHz |
| f _{MAX4} | Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of 1/(t _{WL} + t _{WH}), 1/(t _S + t _H), or 1/t _{CO}) | 100 | | 83.3 | | 62.5 | | MHz |
| f _{MAX5} | Maximum Frequency with Internal Feedback in Output Regis- tered Mode (Least of 1/t _{SCS} , 1/(t _S + t _H), or 1/t _{CO}) ^[4] | 83.3 | | 66.6 | | 50 | | MHz |
| Pipelined Mode Parameters | | | | | | | | |
| t _{ICS} | Input Register Clock to Output Register Clock | 12 | | 15 | | 20 | | ns |
| f _{MAX6} | Maximum Frequency in Pipelined Mode (Least of 1/(t _{CO} + t _{IS}), 1/t _{ICS} , 1/(t _{WL} + t _{WH}), 1/(t _{IS} + t _{IH}), or 1/t _{SCS}) | 83.3 | | 66.6 | | 50.0 | | MHz |

Shaded area contains advanced information.

Note:

5. All AC parameters are measured with 16 outputs switching.



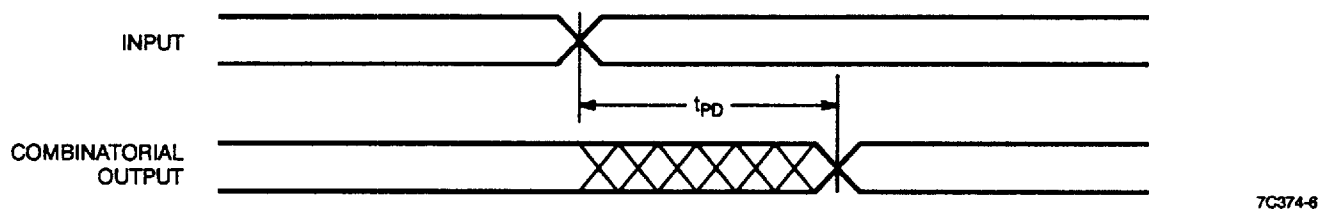
Switching Characteristics Over the Operating Range^[5] (continued)

| Parameter | Description | 7C371-12 | | 7C371-15 | | 7C371-20 | | Unit |
|-------------------------|-----------------------------------|----------|------|----------|------|----------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Reset/Preset Parameters | | | | | | | | |
| t _{RW} | Asynchronous Reset Width | 12 | | 15 | | 20 | | ns |
| t _{RR} | Asynchronous Reset Recovery Time | 14 | | 17 | | 22 | | ns |
| t _{RO} | Asynchronous Reset to Output | | 18 | | 21 | | 26 | ns |
| t _{PW} | Asynchronous Preset Width | 12 | | 15 | | 20 | | ns |
| t _{PR} | Asynchronous Preset Recovery Time | 14 | | 17 | | 22 | | ns |
| t _{PO} | Asynchronous Preset to Output | | 18 | | 21 | | 26 | ns |

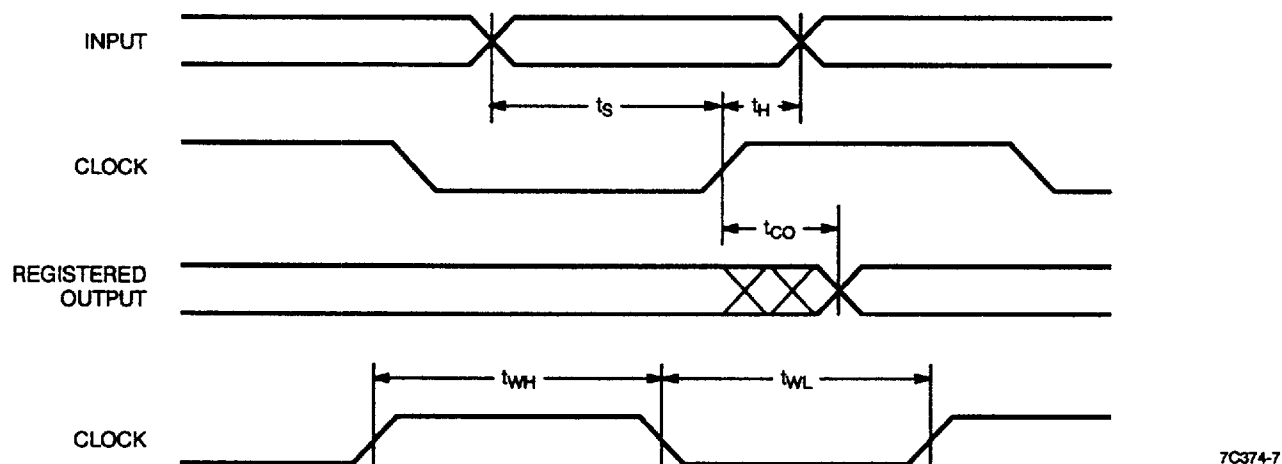
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Switching Waveforms

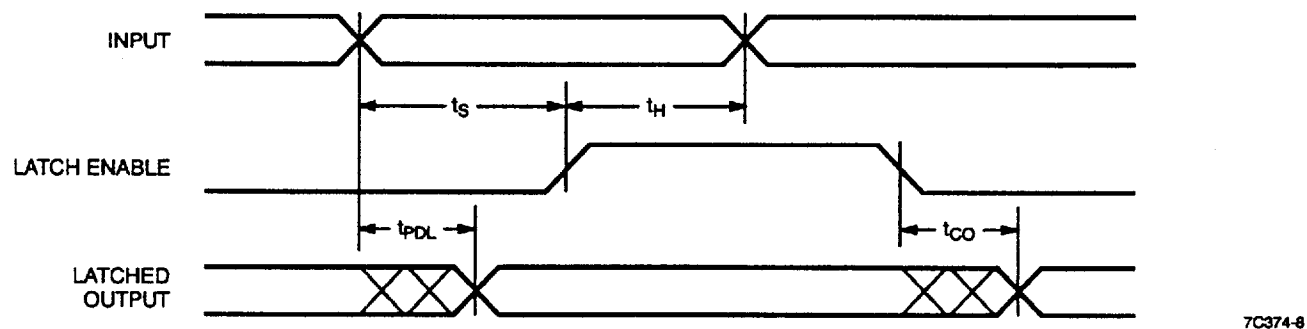
Combinatorial Output



Registered Output



Latched Output





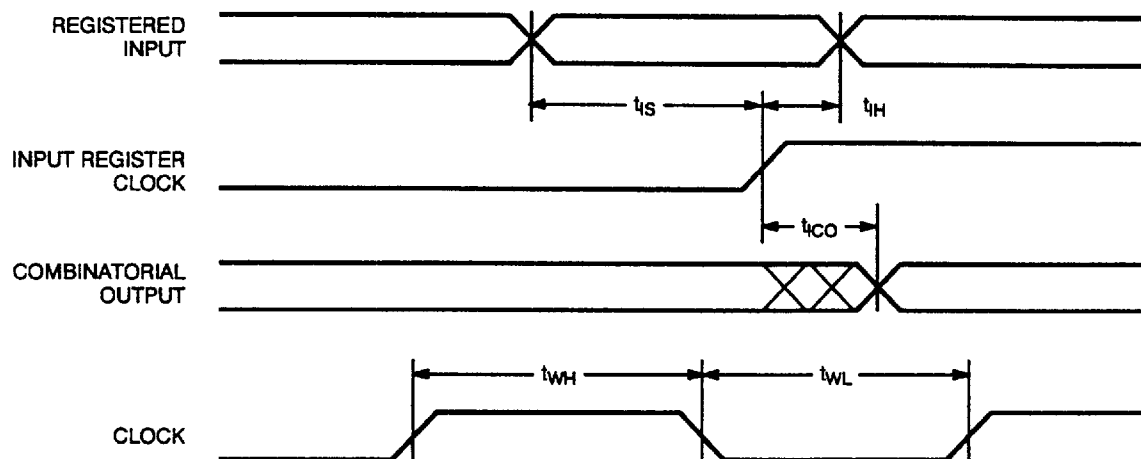
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Switching Waveforms (continued)

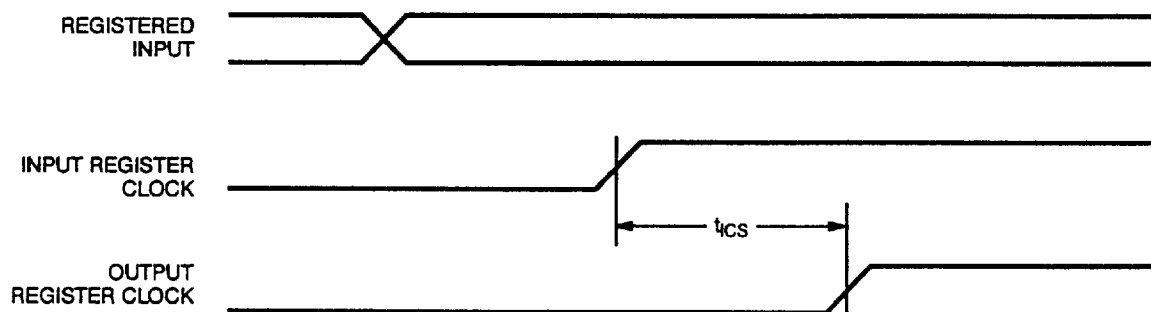
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Registered Input



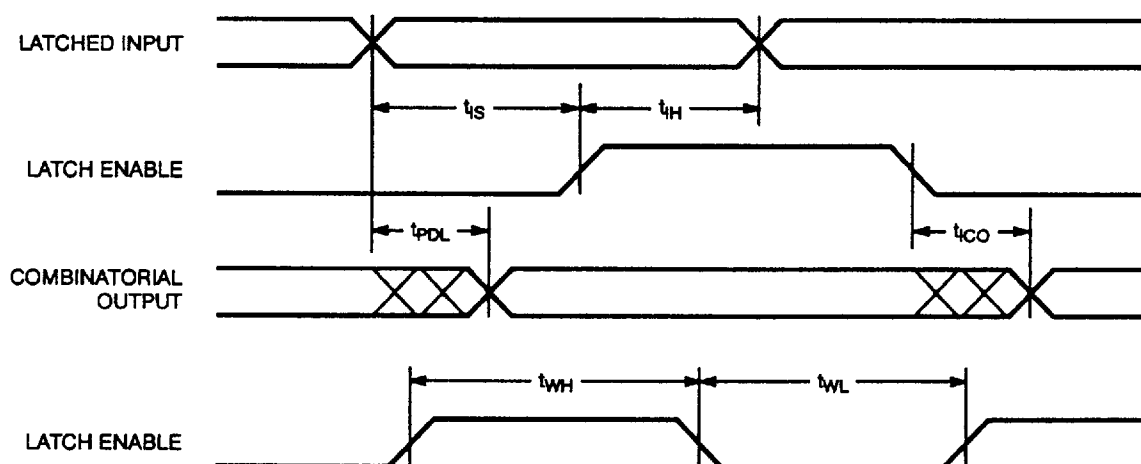
7C374-9

Input Clock to Output Clock



7C374-10

Latched Input



7C374-11



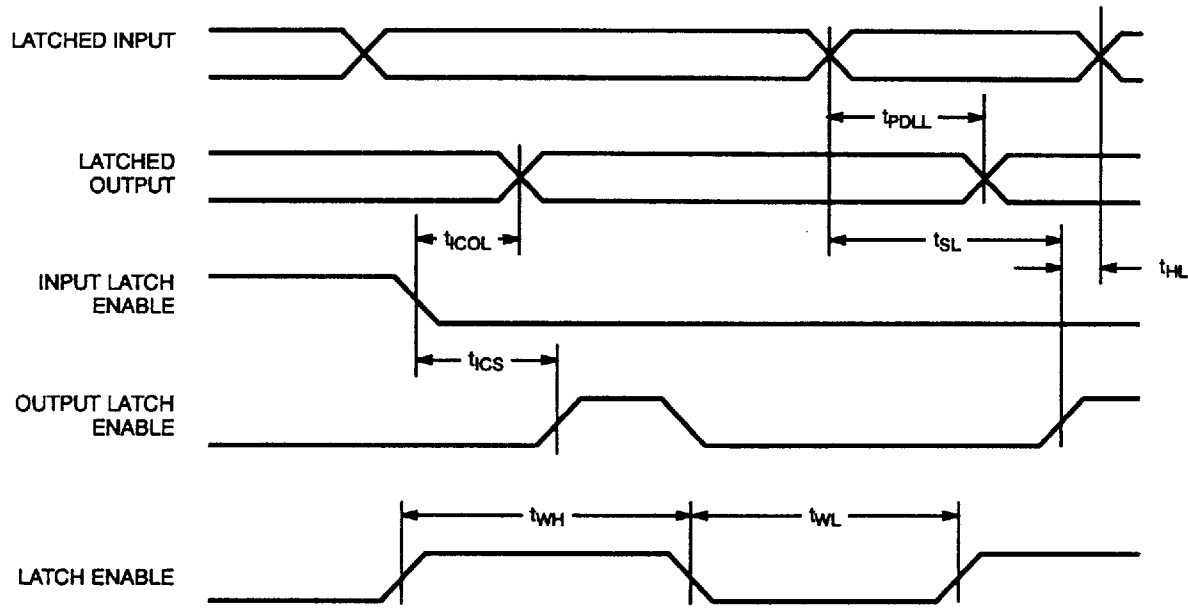
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Switching Waveforms (continued)

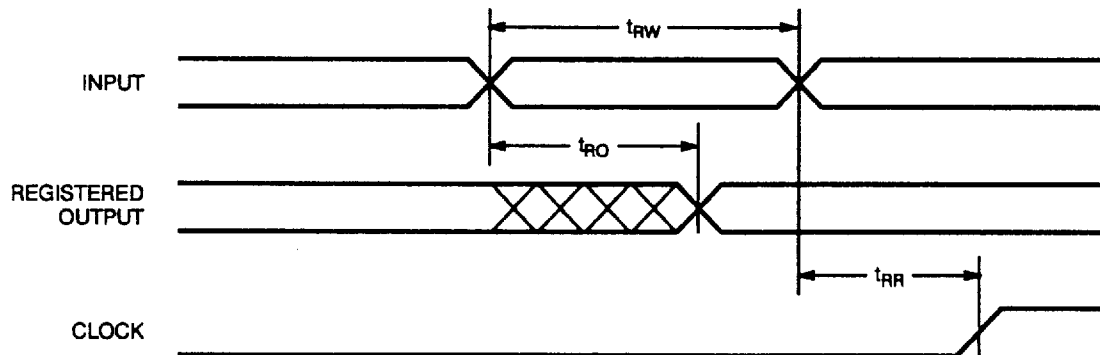
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Latched Input and Output



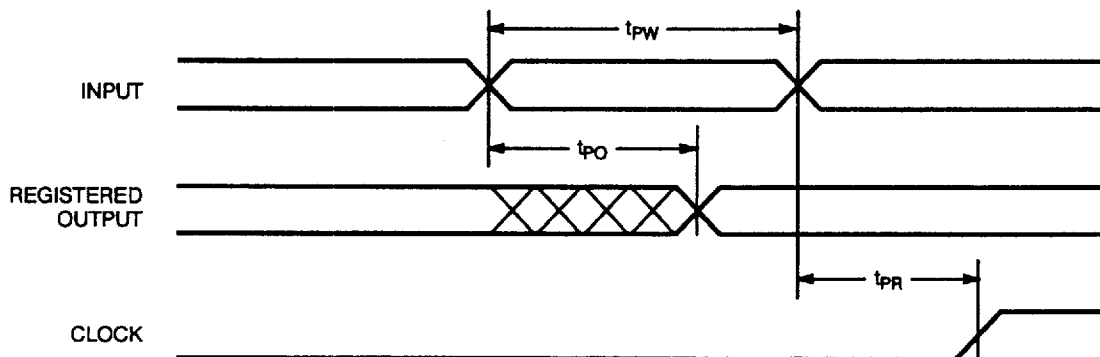
7C374-12

Asynchronous Reset



7C374-13

Asynchronous Preset



7C374-14



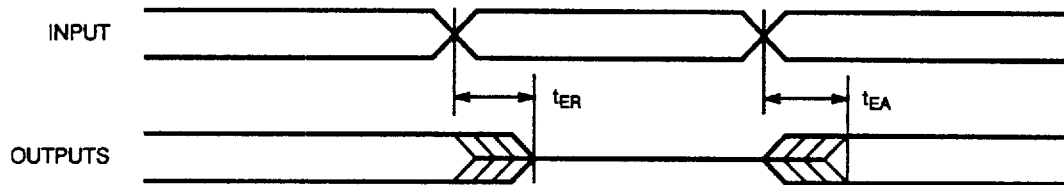
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Switching Waveforms (continued)

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Output Enable/Disable



7C374-15

Ordering Information

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 12 | CY7C374-12GC | G84 | Commercial |
| | CY7C374-12JC | J83 | |
| 15 | CY7C374-15GC | G84 | Commercial |
| | CY7C374-15JC | J83 | |
| | CY7C374-15YMB | Y84 | Military |
| 20 | CY7C374-20GC | G84 | Commercial |
| | CY7C374-20JC | J83 | |
| | CY7C374-20YMB | Y84 | Military |

Shaded areas contain advanced information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

| Parameter | Subgroups |
|------------------|-----------|
| V _{OH} | 1, 2, 3 |
| V _{OL} | 1, 2, 3 |
| V _{IH} | 1, 2, 3 |
| V _{IL} | 1, 2, 3 |
| I _{IX} | 1, 2, 3 |
| I _{OZ} | 1, 2, 3 |
| I _{CC1} | 1, 2, 3 |
| I _{CC2} | 1, 2, 3 |

Switching Characteristics

| Parameter | Subgroups |
|-------------------|-----------------|
| t _{PD} | 7, 8, 9, 10, 11 |
| t _{PDL} | 7, 8, 9, 10, 11 |
| t _{PDLL} | 7, 8, 9, 10, 11 |
| t _{CO} | 7, 8, 9, 10, 11 |
| t _{ICO} | 7, 8, 9, 10, 11 |
| t _{ICOL} | 7, 8, 9, 10, 11 |
| t _S | 7, 8, 9, 10, 11 |
| t _{SL} | 7, 8, 9, 10, 11 |
| t _H | 7, 8, 9, 10, 11 |
| t _{HL} | 7, 8, 9, 10, 11 |
| t _{IS} | 7, 8, 9, 10, 11 |
| t _{IH} | 7, 8, 9, 10, 11 |
| t _{ICS} | 7, 8, 9, 10, 11 |
| t _{EA} | 7, 8, 9, 10, 11 |
| t _{ER} | 7, 8, 9, 10, 11 |



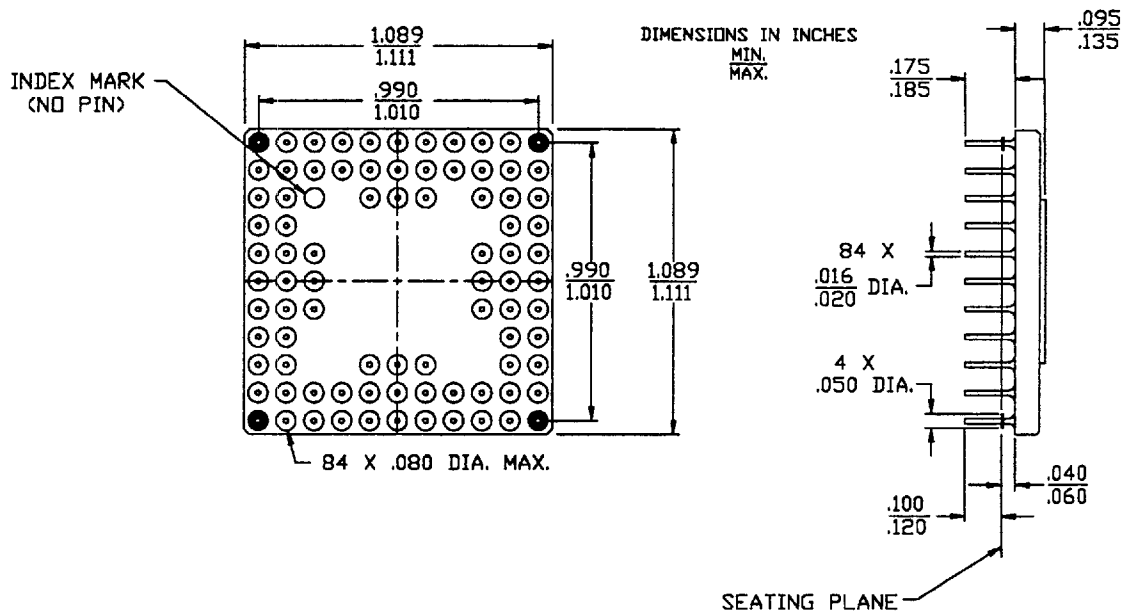
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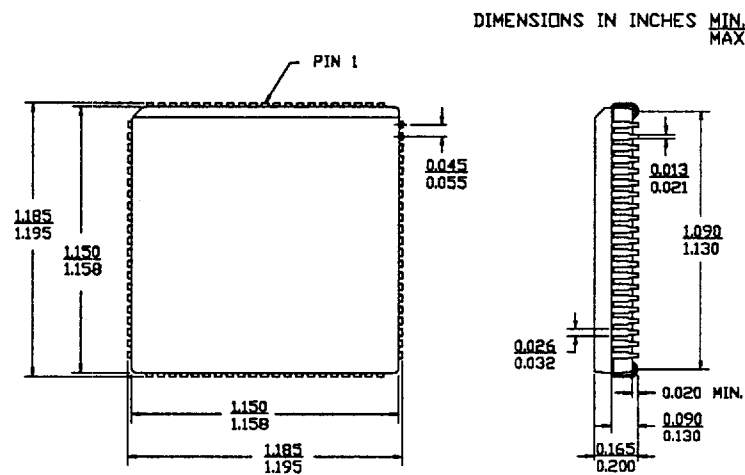
Package Diagrams

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84-Pin Grid Array (Cavity Up) G84



84-Lead Plastic Leaded Chip Carrier J83





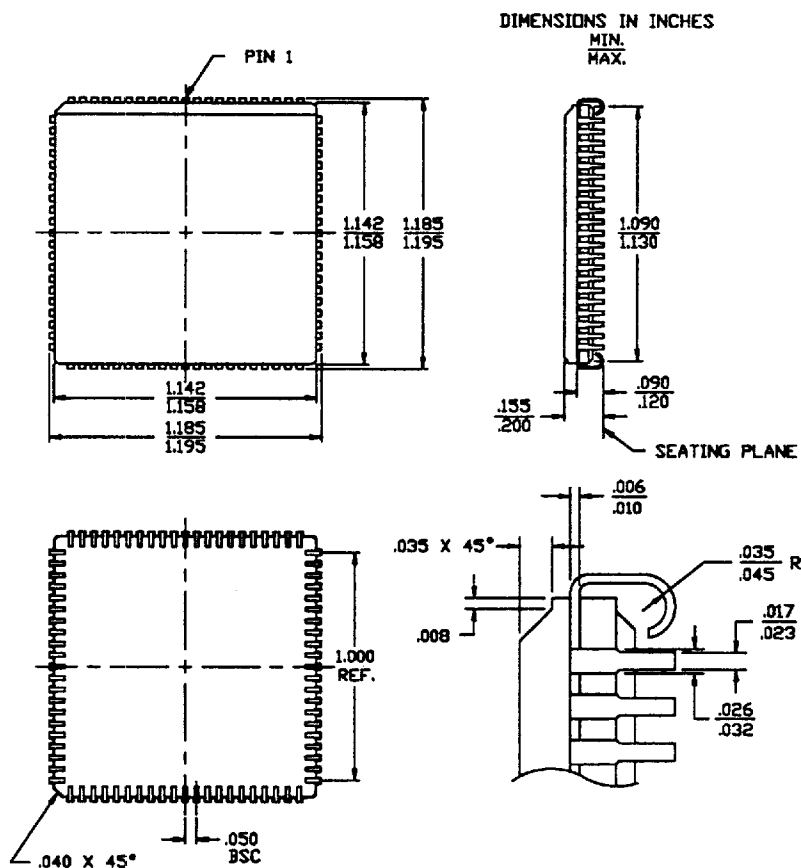
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Package Diagrams (continued)

84-Pin Ceramic Leaded Chip Carrier Y84



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