

Am29C334

CMOS Four-Port Dual-Access Register File



Am29C334

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- **64 x 18 Bit Wide Register File**

The Am29C334 is a 64 x 18-bit, dual-access RAM with two read ports and two write ports.

- **Pipelined Data Path**

The Am29C334 can be configured to support either a non-pipelined data path (similar to the Am29334) or a pipelined data path.

- **Cascadable**

The Am29C334 is cascadable to support either wider word widths, deeper register files, or both.

- **Built in Forwarding Logic**

The Am29C334 provides simultaneous read/write access to the same address for double pipelined systems.

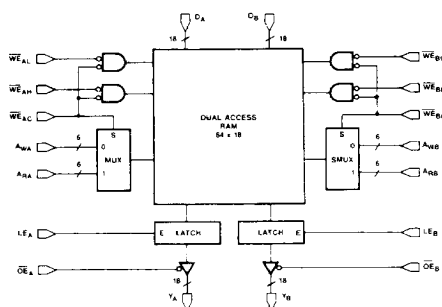
- **Byte Parity Storage**

Width of 18 bits facilitates byte parity storage for each port and provides consistency with the Am29C332 32-bit ALU.

- **Byte Write Capability**

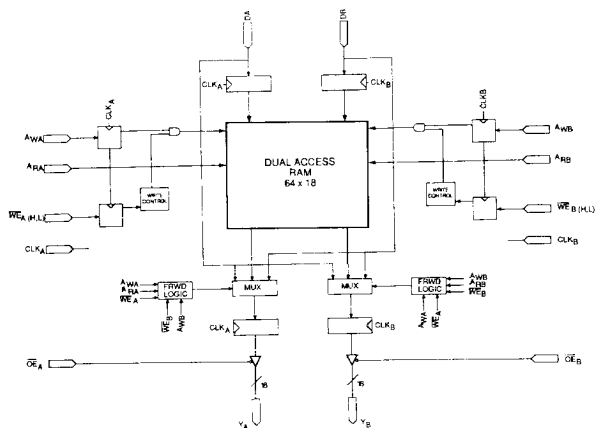
Individual byte-write enables allow byte or full word write.

BLOCK DIAGRAMS



BD003022

Non-Pipelined Mode



BD007021

Pipelined Mode

GENERAL DESCRIPTION

The Am29C334 is a 64-word by 18-bit dual-access RAM with two read ports and two write ports. Two independent, simultaneous accesses are possible and each access can be either a read or a write. It is designed to be used in a system that requires as many as two reads and two writes in a single cycle. The device can be configured to support either a non-pipelined data path or a pipelined data path.

The Am29C334 is also fully compatible with the bipolar Am29334. When the device is connected to the pinout specified for the Am29334, it will appear as a 64-word by 18-bit array without support for pipelined operation. The pipelined operation of the Am29C334 is made possible because of the availability of unused power pins not required by the CMOS part. The pipelined operation is disabled by attaching the PIPE pin to VCC.

RELATED AMD PRODUCTS

Part No.	Description
Am29C323	CMOS 32-Bit Parallel Multiplier
Am29325	32-Bit Floating Point Processor
Am29C325	CMOS 32-Bit Floating Point Processor
Am29331	16-Bit Microprogram Sequencer
Am29C331	CMOS 16-Bit Microprogram Sequencer
Am29332	32-Bit Extended Function ALU
Am29C332	CMOS 32-Bit Extended Function ALU
Am29334	64 x 18 Four-Port Dual-Access Register File
Am29337	16-Bit Bounds Checker
Am29338	128 x 9 Byte Queue

CONNECTION DIAGRAM

120 Lead PGA*

	A	B	C	D	E	F	G	H	J	K	L	M	N
1	AWA2	ARB2	AWA1	DA00	DA02	DA04	DA06	DA09	DA12	DA15	LEA	WEAC	WEAL
2	ARA3	AWA3	ARA1	ARA0	DA03	DA05	DA07	DA10	DA13	DA15	ARA5	AWA5	WEAH
3	AWA4	ARA4	YB00	AWA0	DA01	GND	DA08	PIPE	DA11	DA14	DA17	ARB4	AWB4
4	YB01	YB02	YB03								YA00	YA01	YA02
5	GND4	YB04	YB05								YA03	YA04	GND4
6	YB07	YB06	VCCA								OEA	YA06	YA05
7	YB08	YB09	YB10								YA07	YA08	YA09
8	YB12	YB11	OEB								VCCA	YA11	YA10
9	GND4	YB13	YB14								YA12	YA13	GND4
10	YB15	YB16	YB17								YA14	YA15	YA16
11	WEBL	WEBH	DB01	DB04	VCC	DB06	DB09	DB15	GND	ARB0	YA17	ARB3	AWB3
12	WEBC	LEB	DB00	DB03	VCC	DB05	DB11	DB12	GND	DB17	AWB0	AWB2	ARB2
13	AWB5	ARB5	DB07	DB02	VCC	DB08	DB19	DB14	GND	DB16	DB13	ARB1	AWB1

CD010320

*Pins facing up.

TABLE OF INTERCONNECTIONS

(Sorted by Pin Name)

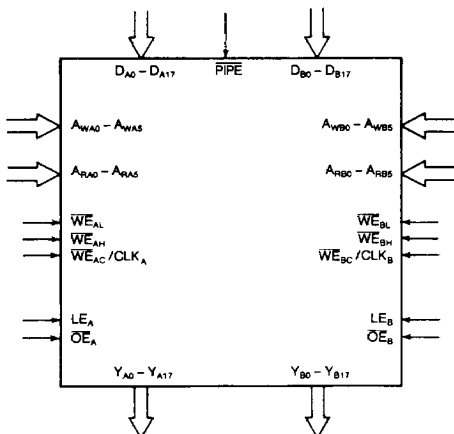
PIN NAME	PIN NO.	PAD NO.	PIN NAME	PIN NO.	PAD NO.	PIN NAME	PIN NO.	PAD NO.	PIN NAME	PIN NO.	PAD NO.
			DA03	E02	65	DB16	K13	93	YA05	N06	21
			DA04	F01	6	DB17	K12	33	YA06	M06	81
			DA05	F02	66	GND	F03	8	YA07	L07	22
			DA06	G03	7	GND	J11	37	YA08	M07	82
			DA07	G02	67	GND	J12	38	YA09	N07	24
ARA0	D02	63	DA08	G01	9	GND	J13	39	YA10	N08	84
ARA1	C02	62	DA09	H01	69	GND4	N05	20	YA11	M08	25
ARA2	B01	61	DA10	H02	10	GND4	N09	26	YA12	L09	85
ARA3	A02	120	DA11	J03	70	GND4	A09	50	YA13	M09	86
ARA4	B03	119	DA12	J01	11	GND4	A05	56	YA14	L10	27
ARA5	L02	74	DA13	J02	71	LEA	L01	14	YA15	M10	87
ARB0	K11	92	DA14	K03	12	LEB	B12	45	YA16	N10	28
ARB1	M13	91	DA15	K02	72	OEA	L06	23	YA17	L11	88
ARB2	N12	90	DA16	K01	13	OEB	C08	53	YB00	C03	118
ARB3	M11	89	DA17	L03	73	PIPE	H03	68	YB01	A04	58
ARB4	M03	77	DB00	C12	104	VCC	E11	97	YB02	B04	117
ARB5	B13	105	DB01	C11	44	VCC	E12	98	YB03	C04	57
AWA0	D03	3	DB02	D13	103	VCC	E13	99	YB04	B05	116
AWA1	C01	2	DB03	D12	43	VCCA	L08	83	YB05	C05	115
AWA2	A01	1	DB04	D11	102	VCCA	C06	113	YB06	B06	55
AWA3	B02	60	DB05	F12	42	WEAC/CLKA	M01	75	YB07	A06	114
AWA4	A03	59	DB06	F13	101	WEAH	N02	76	YB08	A07	54
AWA5	M02	15	DB07	C13	41	WEAL	N01	16	YB09	B07	112
AWB0	L12	32	DB08	F11	100	WEBC/CLKB	A12	106	YB10	C07	52
AWB1	N13	31	DB09	G11	40	WEBH	B11	107	YB11	B08	111
AWB2	M12	30	DB10	G13	96	WEBL	A11	47	YB12	A08	51
AWB3	N11	29	DB11	G12	36	YA00	L04	18	YB13	B09	110
AWB4	N03	17	DB12	H12	95	YA01	M04	78	YB14	C09	109
AWB5	A13	46	DB13	L13	35	YA02	N04	19	YB15	A10	49
DA00	D01	4	DB14	H13	94	YA03	L05	79	YB16	B10	108
DA01	E03	64	DB15	H11	34	YA04	M05	80	YB17	C10	48
DA02	E01	5									

TABLE OF INTERCONNECTIONS (Cont'd.)

(Sorted by Pin No.)

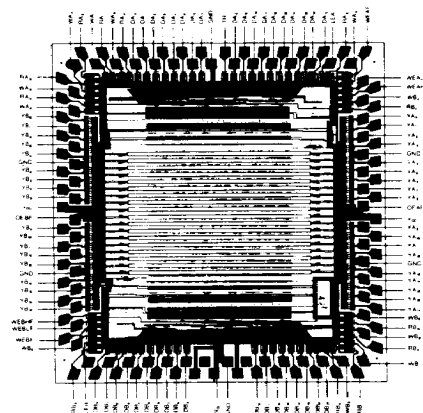
PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.
A01	AWA2	1	C05	YB05	115	H02	DA10	10	M05	YA04	80
A02	ARA3	120	C06	VCCA	113	H03	PIPE	68	M06	YA06	81
A03	AWA4	59	C07	YB10	52	H11	DB15	34	M07	YA08	82
A04	YB01	58	C08	OE _B	53	H12	DB12	95	M08	YA11	25
A05	GNDA	56	C09	YB14	109	H13	DB14	94	M09	YA13	86
A06	YB07	114	C10	YB17	48	J01	DA12	11	M10	YA15	87
A07	YB08	54	C11	DB01	44	J02	DA13	71	M11	ARB3	89
A08	YB12	51	C12	DB00	104	J03	DA11	70	M12	ARB2	30
A09	GNDA	50	C13	DB07	41	J11	GND	37	M13	ARB1	91
A10	YB15	49	D01	DA00	4	J12	GND	38	N01	WE _{AL}	16
A11	WE _{BL}	47	D02	ARA0	63	J13	GND	39	N02	WE _{AH}	76
A12	WE _{BC} /CLK _B	106	D03	AWA0	3	K01	DA16	13	N03	AWB4	17
A13	AWB5	46	D11	DB04	102	K02	DA15	72	N04	YA02	19
B01	ARA2	61	D12	DB03	43	K03	DA14	12	N05	GNDA	20
B02	AWA3	60	D13	DB02	103	K11	ARB0	92	N06	YA05	21
B03	ARA4	119	E01	DA02	5	K12	DB17	33	N07	YA09	24
B04	YB02	117	E02	DA03	65	K13	DB16	93	N08	YA10	84
B05	YB04	116	E03	DA01	64	L01	LEA	14	N09	GNDA	26
B06	YB06	55	E11	VCC	97	L02	ARA5	74	N10	YA16	28
B07	YB09	112	E12	VCC	98	L03	DA17	73	N11	AWB3	29
B08	YB11	111	E13	VCC	99	L04	YA00	18	N12	ARB2	90
B09	YB13	110	F01	DA04	6	L05	YA03	79	N13	ARB1	31
B10	YB16	108	F02	DA05	66	L06	OE _A	23			
B11	WE _{BH}	107	F03	GND	8	L07	YA07	22			
B12	LE _B	45	F11	DB08	100	L08	VCCA	83			
B13	ARB5	105	F12	DB05	42	L09	YA12	85			
C01	AWA1	2	F13	DB06	101	L10	YA14	27			
C02	ARA1	62	G01	DA08	9	L11	YA17	88			
C03	YB00	118	G02	DA07	67	L12	AW _{B0}	32			
C04	YB03	57	G03	DA06	7	L13	D _{B13}	35			
			G11	DB09	40	M01	WE _{AC} /CLK _A	75			
			G12	DB11	36	M02	AW _{A5}	15			
			G13	DB10	96	M03	ARB4	77			
			H01	DA09	69	M04	YA01	78			

LOGIC SYMBOL



LS00222

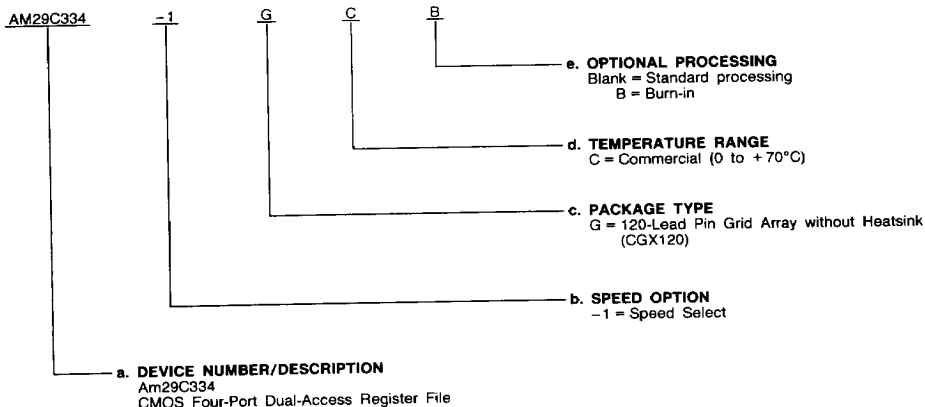
METALLIZATION AND PAD LAYOUT



ORDERING INFORMATION Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

Valid Combinations	
AM29C334	GC, GCB
AM29C334-1	

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**

AM29C334

/B

Z

C

e. **LEAD FINISH**
C = Gold

d. **PACKAGE TYPE**
Z = 120-Lead Pin Grid Array without Heatsink
(CGX120)

c. **DEVICE CLASS**
/B = Class B

b. **SPEED OPTION**
Not Applicable

a. **DEVICE NUMBER/DESCRIPTION**
Am29C334
CMOS Four-Port Dual-Access Register File

Valid Combinations	
AM29C334	/BZC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

ARA0 – ARA5 Read Address A-Side (Input)

The 6-bit read address input selects one of the 64 memory locations for output to the Y_A Data Latch.

ARB0 – ARB5 Read Address B-Side (Input)

The 6-bit read address input selects one of the 64 memory locations for output to the Y_B Data Latch.

AWA0 – AWA5 Write Address A-Side (Input)

The 6-bit write address input selects one of the 64 memory locations for writing new data from the D_A input.

AWB0 – AWB5 Write Address B-Side (Input)

The 6-bit write address input selects one of the 64 memory locations for writing new data from the D_B input.

DA0 – DA17 Data A-Side (Input)

New data is written into memory from this input, as selected by the AW_A address input.

DB0 – DB17 Data B-Side (Input)

New data is written into memory from this input, as selected by the AW_B address input.

GND, VCC Power

Power supply for the internal logic (0, 5 V).

GNDA, VCCA Power

Power supply for the output drivers (0, 5 V).

LEA Y_A Data Latch Enable (Input, Active HIGH)

The LE_A input controls the latch for the Y_A output port. When LE_A is HIGH, the latch is open (transparent) and data from the RAM, as selected by the AR_A address inputs, is passed to the Y_A output. When LE_A is LOW, the latch is closed and it retains the last data read from the RAM. LE_A is disabled in the pipelined mode.

LEB Y_B Data Latch Enable (Input, Active HIGH)

The LE_B input controls the latch for the Y_B output port. When LE_B is HIGH, the latch is open (transparent), and data from the RAM, as selected by the AR_B address inputs, is passed to the Y_B output. When LE_B is LOW, the latch is closed and it retains the last data read from the RAM. LE_A is disabled in the pipelined mode.

OE $_A$ Y_A Output Enable (Input, Active LOW)

When OE_A is LOW, data in the Y_A Data Latch is driven on the Y_A output. When OE_A is HIGH, Y_A output is in the high-impedance (off) state.

OE $_B$ Y_B Output Enable (Input, Active LOW)

When OE_B is LOW, data in the Y_B Data Latch is driven on the Y_B outputs. When OE_B is HIGH, Y_B output is in the high-impedance (off) state.

PIPE Pipeline Enable (Input, Active LOW)

When PIPE is LOW, the input and output registers are enabled, allowing for pipelined operation. When HIGH, these registers are made transparent.

WE $_AC$ /CLK $_A$ Write Enable A-Side Common (Input, Active LOW)

When WE_{AC} is LOW together with WE_{AH} or WE_{AL} , new data is written into the location selected by the AW_A address. When WE_{AC} is HIGH, no data is written into the RAM through the A port. WE_{AC} acts as a clock input in the pipeline mode for the A side.

WE $_BC$ /CLK $_B$ Write Enable B-Side Common (Input, Active LOW)

When WE_{BC} is LOW together with WE_{BH} or WE_{BL} , new data is written into the location selected by the AW_B address. When WE_{BC} is HIGH, no data is written into the RAM through the B port. WE_{BC} acts as a clock input in the pipeline mode for the B side.

WE $_AH$ High-Byte Write Enable A-Side (Input, Active LOW)

When WE_{AH} is LOW together with WE_{AC} , new data is written into the high byte of the location selected by the AW_A address input. When WE_{AH} is HIGH, no data is written into the high byte.

WE $_BH$ High-Byte Write Enable B-Side (Input, Active LOW)

When WE_{BH} is LOW together with WE_{BC} , new data is written into the high byte of the location selected by the AW_B address input. When WE_{BH} is HIGH, no data is written into the high byte.

WE $_AL$ Low-Byte Write Enable A-Side (Input, Active LOW)

When WE_{AL} is LOW together with WE_{AC} , new data is written into the low byte of the location selected by the AW_A address input. When WE_{AL} is HIGH, no data is written into the low byte.

WE $_BL$ Low-Byte Write Enable B-Side (Input, Active LOW)

When WE_{BL} is LOW together with WE_{BC} , new data is written into the low byte of the location selected by the AW_B address input. When WE_{BL} is HIGH, no data is written into the low byte.

Y $_A0$ – Y $_A17$ Data Latch (Outputs, Three-State)

The 18-bit Y_A Data Latch outputs.

Y $_B0$ – Y $_B17$ Data Latch (Outputs, Three-State)

The 18-bit Y_B Data Latch outputs.

FUNCTIONAL DESCRIPTION

The heart of the Am29C334 is a high-speed 64-word by 18-bit dual RAM cell array. Six write enables permit the RAM word to be written in one or both of its 9-bit bytes. Data to be written is presented to each side of the RAM array through the two data ports (D_A and D_B).

The remainder of the logic surrounding the RAM array supports pipelining the RAM access and providing a forwarding path for data around the RAM. This forwarding path is needed to eliminate the latency cycle associated with consecutive write/read accesses to the same memory location in a pipelined system.

Pipelining of the RAM is controlled by the $\overline{PIPE}$ pin. When not asserted (i.e., in non-pipelined mode) the registers on the inputs (write ports $D_{A/B}$, write addresses $A_{W_{A/B}}$, and write enables $WE_{A/B}$) are made fully transparent, while the registers at the outputs (the read ports $Y_{A/B}$) are turned into latches, controlled by the latch enables $LE_{A/B}$.

In either mode of operation, each side of the RAM is controlled by its individual control signals. This means that the two sides of the RAM can operate at different clock rates to one

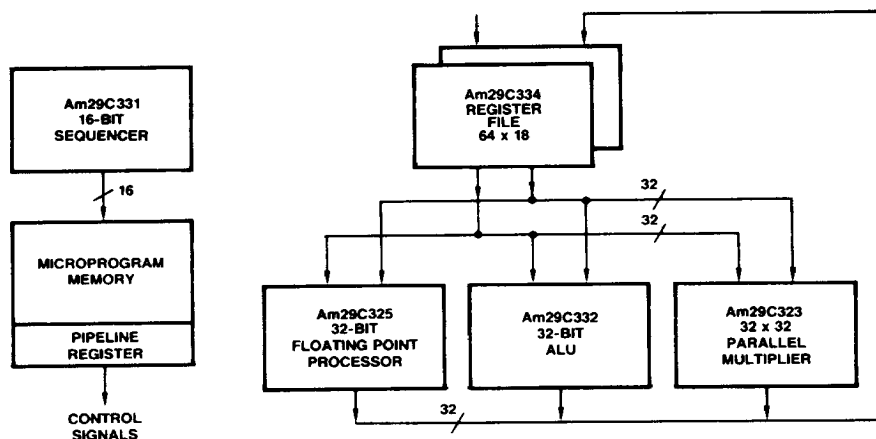
another. In the pipelined mode, these clock rates must have a known relationship between each other.

In the non-pipelined mode, there is no need for a relationship between the clock rates. Two special cases of operation arise because of this. The first is where the location written to by one side is being read from the other side. In this case, known as A-to-B transparency, the value read is the value being written. The second occurs when two writes to the same location occur at the same time. In this case the value written can not be defined, but the operation is not harmful to the device.

The transparency mode (A-A or B-B) during a write ($WE_A = LOW$) allows the data in (D_A) to not only be written into memory, but also to appear at the output (Y_A) when the output latch (LE_A) is HIGH and the output enable control (OE_A) is LOW.

Extensions to Four Read Ports and Two Write Ports

A RAM with four read ports and two write ports can be made by using two dual-access RAMs and connecting each of the write ports, write addresses, and write enables in parallel for the two devices. Figure 2 details this in a non-pipelined mode.



AF003482

Figure 1. Am29C300 CMOS Family High-Performance System Block Diagram

32 Word x 36 Bit Single-Access RAM

It is possible to convert the 64 word x 18 bit dual-access RAM into a 32 word x 36 bit single-access RAM. This is performed by storing the upper half of the 36 bits in the upper half of the 64 words and addressing these from the A side, and storing the lower half of the 36 bits in the lower half of the 64 words and addressing these from the B side. This arrangement does not change the capacity of the RAM, but the dual access is lost (see Figure 4).

Operational Modes

The Am29C334 may be configured in a non-pipelined mode or in a pipelined mode by controlling the $\overline{PIPE}$ pin. This mode is selected via hardwiring the pin to either LOW or HIGH. This option should not be changed during operation.

Non-Pipelined Data Path

In non-pipelined mode ($\overline{PIPE} = 1$), the Am29C334 is a flow-through device; data is read out, used, and written back all in the same cycle. In this mode all the registers are made transparent except the registers at the two read ports that are configured as latches. The read port latches are controlled individually by the LE_A and LE_B , so that they are transparent when the latch enables are HIGH and retain the data when the latch enables are LOW. The "forwarding logic" incorporated to support the pipelined mode of operation is also disabled in this mode of operation (specifically, the address comparators are disabled).

In the non-pipelined mode of operation it is possible to simultaneously read two ports, read one port and write to the other, or write to two ports, concurrently. The read and write

addresses are internally multiplexed on each side. The selection of the read and write addresses is controlled by the exclusive-OR of the PIPE pin and $\overline{WE}_{AC/BC}$. Normally, the $\overline{WE}_{AC/BC}$ are connected to the system clock. With PIPE deasserted, the read address will be selected in the high part of the clock cycle ($\overline{WE}_{AC/BC} = 1$) and the write address selected only in the low part. Byte selection for writing on either ports is controlled by the $\overline{WE}_{H/L}$ pins.

Two interesting cases arise as a result of the dual access capability. The first occurs if a location is written into by one side while it is being read out by the other side. In this case, known as A-to-B transparency, the data being written will appear on the read port after the Transparency_{AB} time (if other read access time parameters are met). The second case of interest occurs if both sides write to the same location at the same time. The value written as a result of this operation cannot be defined.

Pipelined Data Path

The Am29C334 can be configured in a pipelined system by asserting the PIPE signal ($\text{PIPE} = 0$) and adding an additional external register in the write address and the write control path on both A and B ports as shown in Figure 3. The registers on each side are controlled by separate clocks that are supplied over the $\overline{WE}_{AC}$ and $\overline{WE}_{BC}$ pins.

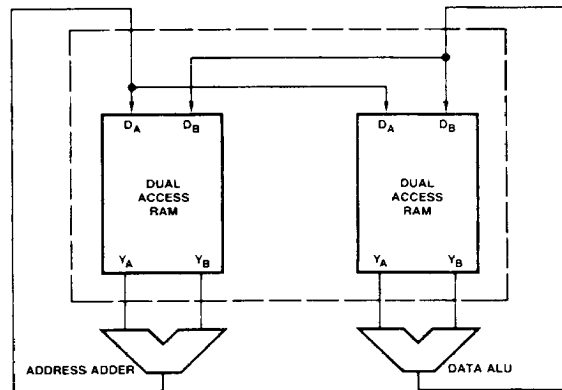
Typically, in a pipelined system a read - modify - write would span three cycles. In the second half of the first cycle, a read of the operand(s) is performed and the data is clocked into the output registers at the end of the cycle. In the second cycle, the operation is performed on the operands and the result is clocked into the data register on the write port at the end of the second cycle. In the first half of the third cycle, the data is written to the register file. Therefore, in any cycle, a pipelined system is writing the result of instruction n (in the first half),

executing instruction $n + 1$, and reading the operands needed in instruction $n + 2$. In any case, a write operation followed by a read operation is performed in the RAM in a cycle.

A special case arises if the data to be written by the previous instruction is needed in the next instruction as an operand. Due to the pipeline register being at its write port, the location is not written into until the next cycle, and hence only the previous value is available in the current cycle. To overcome this problem, "forwarding logic" is included as shown in the block diagram. This logic consists of three elements: an address comparator, an AND gate, and a three-to-one multiplexer, as shown. If the read address of the current instruction is the same as the write address of the previous instruction, and if the result is to be written, then the data to be written is forwarded by the forwarding multiplexer to the output registers. Since there are two write ports, forwarding paths on both ports are provided. As each write port has byte write capability, the forwarding is further broken into the upper and lower bytes.

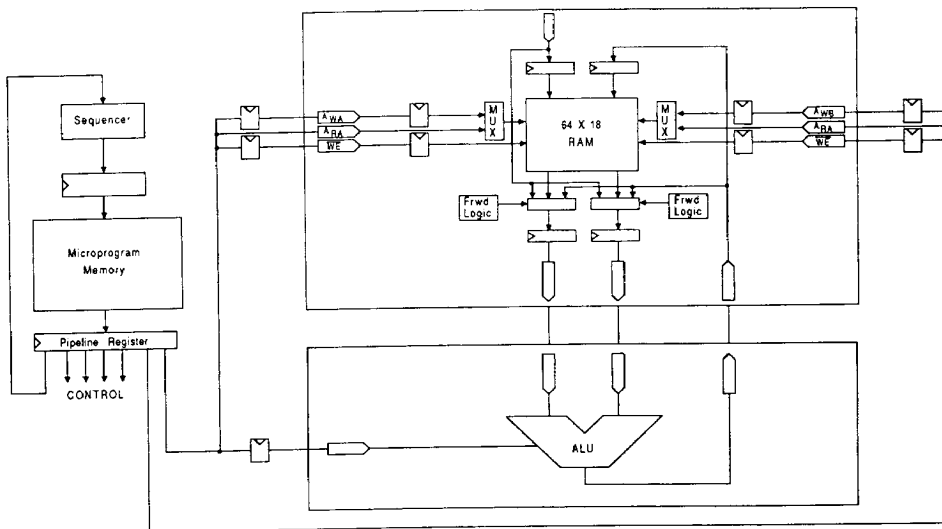
Since each side has its own $\overline{WE}_C/\text{CLK}$ control, it is possible to clock each side of the chip differently. However, if the part is used at different frequencies, the forwarding cannot be guaranteed unless the addresses compared are held valid long enough to allow for a comparison to be made and the results of the forwarding setup on the output register.

As mentioned earlier, it is necessary to use an external write address and write control registers in a pipelined system. These registers have not been included for two reasons. First, it is possible for the user to abort the writing before it fills the internal pipe. This situation may arise in cases such as in "traps." Second, by providing an external write address register it provides the flexibility of obtaining the write address from several sources by using an external multiplexer.



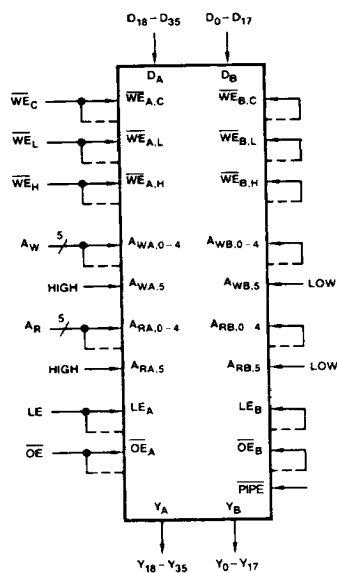
AF003490

Figure 2. RAM with Four Read Ports and Two Write Ports for Non-pipelined Mode



BD006880

Figure 3. System Diagram With the Am29C334 in a Double Pipelined Data Path



LS001791

Figure 4. 32 x 36 RAM (Single Access) Using 64 x 18 Dual-Access RAM

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65 to +150°C
 Temperature Under Bias - T_C -55 to +125°C
 Supply Voltage to Ground Potential
 Continuous -0.3 to +7.0 V
 DC Voltage Applied to Outputs
 for HIGH Output State -0.3 V to + V_{CC} + 0.3 V
 DC Input Voltage -0.3 V to + V_{CC} + 0.3 V
 DC Output Current, Into LOW Outputs 30 mA
 DC Input Current -10 mA to +10 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) 0 to +70°C
 Supply Voltage +4.75 to +5.25 V

Military* (M) Devices

Temperature (T_A) -55 to +125°C
 Supply Voltage (V_{CC}) +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

* Military product 100% tested at T_A = +25°C, +125°C, and -55°C.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions (Note 1)		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IL} or V _{IH} I _{OH} = -4 mA		2.4		Volts
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IL} or V _{IH} I _{OL} = 8 mA			0.5	Volts
V _{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage (Note 2)		2.0		Volts
V _{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage (Note 2)			0.8	Volts
I _{IL}	Input LOW Current	V _{CC} = Max. V _{IN} = 0.5 V			-10	μA
I _{IH}	Input HIGH Current	V _{CC} = Max. V _{IN} = V _{CC} - 0.5 V			10	μA
I _{OZH}	Off State (High-Impedance) Output Current	V _{CC} = Max.	V _O = 2.4 V		10	μA
I _{OZL}			V _O = 0.5 V		-10	
I _{CC}	Static Power Supply Current	V _{IN} = V _{CC} or GND V _{CC} = Max I _O = 0 μA	T _A = -55 to 125°C		80	mA
			T _A = 0 to +70°C		70	mA
C _{PD}	Power Dissipation Capacitance (Note 3)	V _{CC} = 5.0 V T _A = 25°C No Load		900 pF Typical		

Notes: 1. V_{CC} conditions shown as Min. or Max. refer to the commercial ($\pm 5\%$) V_{CC} limits.

2. These input levels provide zero-noise immunity and should only be statically tested in a noise-free environment (not functionally tested).

3. C_{PD} determines the no-load dynamic current consumption:

$I_{CC}(\text{Total}) = I_{CC}(\text{Static}) + C_{PD} V_{CC} f$, where f is the switching frequency of the majority of the internal nodes, normally one-half of the clock frequency. This specification is not tested.

SWITCHING CHARACTERISTICS over **COMMERCIAL** operating range unless otherwise specified

NON-PIPELINED MODE (Note 1)

No.	Parameter	Description	Test Conditions	29C334		29C334-1		29C334-2		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
1	Access Time	ARA or ARB to YA or YB	LEA or LEB = H		32		26		21	ns
2	Access Time	WEAC or WEBC to YA or YB	LEA or LEB = H		30		25		20	ns
3	Turn-On Time	OE _A or OE _B ↓ to YA or YB Active		0	20	0	16	0	16	ns
4	Turn-Off Time (Note 2)	OE _A or OE _B ↑ to YA or YB = High Impedance		0	20	0	16	0	16	ns
5	Enable Time	LEA or LEB ↑ to YA or YB		0	16	0	12	0	11	ns
6	Transparency	WE _A or WE _B ↓ to YA or YB	LEA or LEB = H							ns
7	Transparency	DA or DB to YA or YB	LEA or LEB = H, WE _A or WE _B = L		39		33		27	ns
8	Write Recovery Time	ARA or ARB to WEAC or WEBC		(2)(1)		(2)(1)		(2)(1)		ns
9	Data Setup Time	DA or DB to WE _A or WE _B ↑		15		13		13		ns
10	Data Hold Time	DA or DB to WE _A or WE _B ↓		0		0		0		ns
11	Address Setup Time	AWA or AWB to WE _A or WE _B ↓		2		2		2		ns
12	Address Hold Time	AWA or AWB to WE _A or WE _B ↑		1		1		1		ns
13	Address Setup Time	ARA or ARB to LEA or LEB ↓		20		17		17		ns
14	Address Hold Time	ARA or ARB to LEA or LEB ↑		1		1		1		ns
15	Latch Close Before Write	LEA or LEB to WE _A or WE _B ↓		0		0		0		ns
16	Read Before Latch Close	WEAC or WEBC to LEA or LEB ↓		20		16		16		ns
17	Write Pulse Width	WE _A or WE _B (LOW)		20		16		16		ns
18	Latch Data Capture Pulse Width	LEA or LEB (HIGH)		14		12		12		ns

Notes: See notes following Military table.

SWITCHING CHARACTERISTICS over **MILITARY** operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

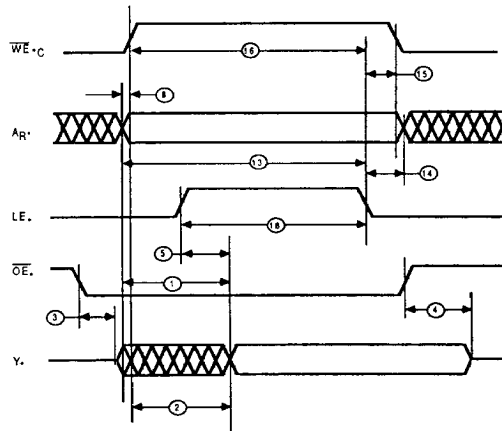
NON-PIPELINED MODE (Note 1)

No.	Parameter	Description	Test Conditions	29C334		Unit
				Min.	Max.	
1	Access Time	A_{RA} or A_{RB} to Y_A or Y_B	LE_A or $LE_B = H$		40	ns
2	Access Time	$\overline{WE}_{AC}$ or $\overline{WE}_{BC}$ to Y_A or Y_B	LE_A or $LE_B = H$	0	37	ns
3	Turn-On Time	$\overline{OE}_A$ or $\overline{OE}_B \downarrow$ to Y_A or Y_B Active		0	16	ns
4	Turn-Off Time (Note 2)	$\overline{OE}_A$ or $\overline{OE}_B \uparrow$ to Y_A or $Y_B = \text{High Impedance}$		0	25	ns
5	Enable Time	LE_A or $LE_B \uparrow$ to Y_A or Y_B		0	21	ns
6	Transparency	$\overline{WE}_A$ or $\overline{WE}_B \downarrow$ to Y_A or Y_B	LE_A or $LE_B = H$	0	47	ns
7	Transparency	D_A or D_B to Y_A or Y_B	LE_A or $LE_B = H$, $\overline{WE}_A$ or $\overline{WE}_B = L$		47	ns
8	Write Recovery Time	A_{RA} or A_{RB} to $\overline{WE}_{AC}$ or $\overline{WE}_{BC}$			(2)-(1)	ns
9	Data Setup Time	D_A or D_B to $\overline{WE}_A$ or $\overline{WE}_B \uparrow$		19		ns
10	Data Hold Time	D_A or D_B to $\overline{WE}_A$ or $\overline{WE}_B \uparrow$		2		ns
11	Address Setup Time	A_{WA} or A_{WB} to $\overline{WE}_A$ or $\overline{WE}_B \downarrow$		4		ns
12	Address Hold Time	A_{WA} or A_{WB} to $\overline{WE}_A$ or $\overline{WE}_B \uparrow$		2		ns
13	Address Setup Time	A_{RA} or A_{RB} to LE_A or $LE_B \downarrow$		23		ns
14	Address Hold Time	A_{RA} or A_{RB} to LE_A or $LE_B \downarrow$		1		ns
15	Latch Close Before Write	LE_A or LE_B to $\overline{WE}_A$ or $\overline{WE}_B \downarrow$		0		ns
16	Read Before Latch Close	$\overline{WE}_{AC}$ or $\overline{WE}_{BC}$ to LE_A or $LE_B \downarrow$		24		ns
17	Write Pulse Width	$\overline{WE}_A$ or $\overline{WE}_B$ (LOW)		23		
18	Latch Data Capture Pulse Width	LE_A or LE_B (HIGH)		17		ns

Notes: 1. $\overline{WE}_A = \overline{WE}_{AC} + \overline{WE}_{AL/H}$
 $\overline{WE}_B = \overline{WE}_{BC} + \overline{WE}_{BL/H}$
 2. Y_A and Y_B are tested independently.
 3. Minimum delays are not tested.

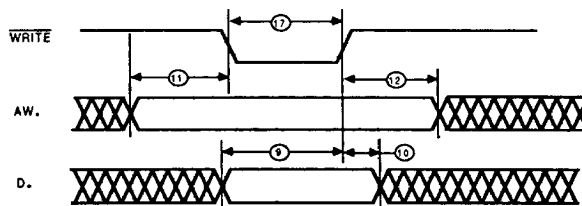
SWITCHING WAVEFORMS

NON-PIPELINED MODE



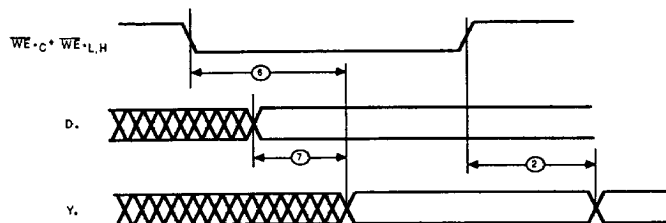
WF023330

Read Function (* means A or B)



WF023340

Write Function (* means A or B)



WF023320

Transparency

NOTE: LE_{H} = HIGH
 OE_{L} = LOW
 * means A or B

SWITCHING CHARACTERISTICS over **COMMERCIAL** operating range (Cont'd.)

PIPELINED MODE

No.	Parameter	Description	29C334		29C334-1		29C334-2		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
19	Write Data Setup Time	D_A or D_B to CLK_A or CLK_B †	15		13		13		ns
20	Write Data Hold Time	D_A or D_B to CLK_A or CLK_B †	1		1		1		ns
21	Write Address Setup Time	A_{WA} or A_{WB} to CLK_A or CLK_B †	23		20		20		ns
22	Write Address Hold Time	A_{WA} or A_{WB} to CLK_A or CLK_B †	0		0		0		ns
23	Write Enable Setup Time	$\overline{WE}_H$ or $\overline{WE}_L$ to CLK_A or CLK_B †	20		16		16		ns
24	Write Enable Hold Time	$\overline{WE}_H$ or $\overline{WE}_L$ to CLK_A or CLK_B †	0		0		0		ns
25	Read Address Setup Time	A_{RA} or A_{RB} to CLK_A or CLK_B †	24		20		20		ns
26	Read Address Hold Time	A_{RA} or A_{RB} to CLK_A or CLK_B †	0		0		0		ns
27	Minimum Clock Cycle	CLK_A or CLK_B (LOW)	50		40		40		ns
28	Minimum Clock Pulse	CLK_A or CLK_B (HIGH)	17		14		14		ns
29	Minimum Clock Pulse	CLK_A or CLK_B (LOW)	17		14		14		ns
30	Clock to Y	Y_A or Y_B to CLK_A or CLK_B	14		12		10		ns

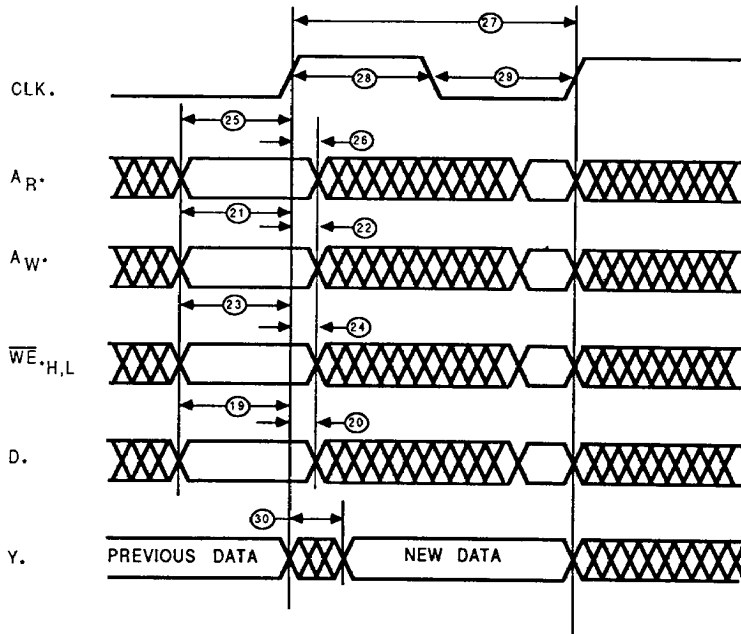
SWITCHING CHARACTERISTICS over **MILITARY** operating range (Cont'd.)

PIPELINED MODE

No.	Parameter	Description	29C334		Unit
			Min.	Max.	
19	Write Data Setup Time	D_A or D_B to CLK_A or CLK_B †	19		ns
20	Write Data Hold Time	D_A or D_B to CLK_A or CLK_B †	2		ns
21	Write Address Setup Time	A_{WA} or A_{WB} to CLK_A or CLK_B †	27		ns
22	Write Address Hold Time	A_{WA} or A_{WB} to CLK_A or CLK_B †	2		ns
23	Write Enable Setup Time	$\overline{WE}_H$ or $\overline{WE}_L$ to CLK_A or CLK_B †	23		ns
24	Write Enable Hold Time	$\overline{WE}_H$ or $\overline{WE}_L$ to CLK_A or CLK_B †	2		ns
25	Read Address Setup Time	A_{RA} or A_{RB} to CLK_A or CLK_B †	28		ns
26	Read Address Hold Time	A_{RA} or A_{RB} to CLK_A or CLK_B †	0		ns
27	Minimum Clock Cycle	CLK_A or CLK_B (LOW)	55		ns
28	Minimum Clock Pulse	CLK_A or CLK_B (HIGH)	20		ns
29	Minimum Clock Pulse	CLK_A or CLK_B (LOW)	20		ns
30	Clock to Y	Y_A or Y_B to CLK_A or CLK_B	18		ns

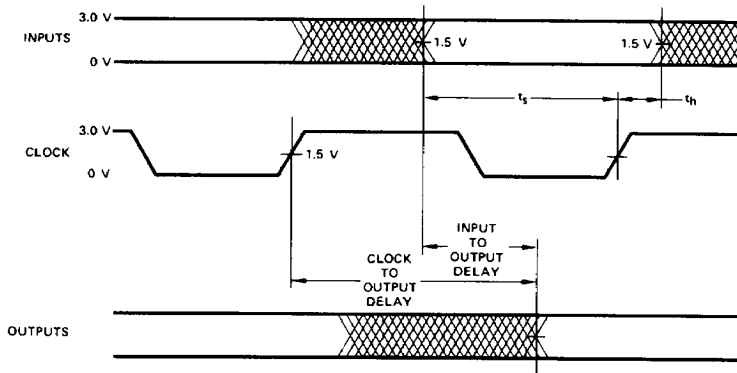
SWITCHING WAVEFORMS (Cont'd.)

PIPELINED MODE



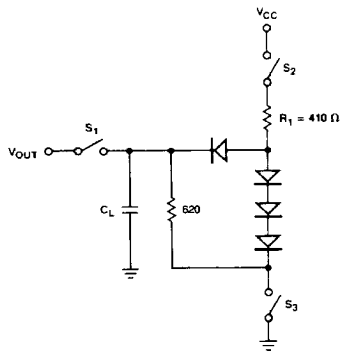
WF023310

* means A or B



WFR02990

SWITCHING TEST CIRCUIT



TC003424

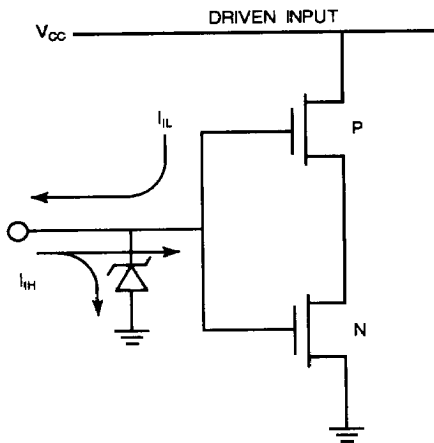
- Notes:**
1. $C_L = 50\text{pF}$ includes scope probe, wiring and stray capacitances without device in test fixture.
 2. S_1, S_2, S_3 are closed during functions tests and all AC tests except output enable tests.
 3. S_1 and S_3 are closed while S_2 is open for t_{pZH} test. S_1 and S_2 are closed while S_3 is open for t_{pZL} test.
 4. $C_L = \text{TBD}$ for output disable tests.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

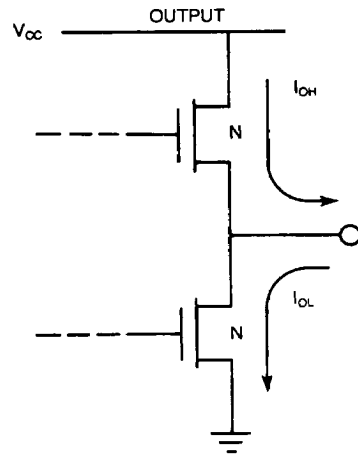
KS000010

INPUT/OUTPUT CIRCUIT DIAGRAMS



IC000861

$C_I \approx 5.0 \text{ pF}$, all inputs



IC000870

$C_O \approx 5.0 \text{ pF}$, all outputs