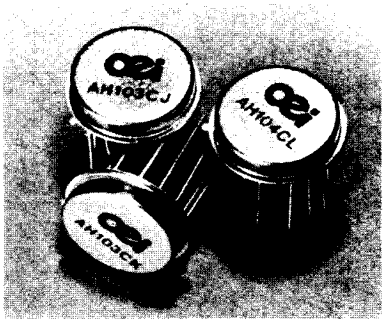
Fast-Settling FET Op Amp



Features
- Fast Settling: 160ns max to 0.1% (AH104)
- Low Offset/Low Drift: 1mV max, 5μV/° C max (CL grade)
- Wide Bandwidth: 400MHz GBW (AH104)
- Internally compensated for unity gain (AH103)
- Drive Capability: ±30mA min at ±10V min

Applications
- Pulse amplifiers
- Fast D/A converters
- Waveform generators
- High speed test equipment

The AH103 and AH104 op amps are designed for minimal tradeoff between AC and DC specifications, allowing operation over a wide frequency range. The AH103 is internally compensated for unity gain stability with pulse inputs, while the AH104 allows optimum high frequency performance by allowing the user to externally compensate for the input frequency and form.

Both are available in three grades relating to the input offset. A maximum initial offset of 1mV and maximum drift of 5μV/°C are available with the AH103CL and the AH104CL. Each unit can also be externally trimmed for even tighter offset requirements.

When compensated for pulse inputs and $A_{CL} = -1$, the AH104 will typically settle to within 0.01% in only 240ns, and is tested and guaranteed not to exceed 160ns to 0.1%. The AH103 is only slightly slower, but requires no external compensation capacitor.

When compensated for pulse inputs and $A_{CL} = -1$, the AH104 will slew at least 220V/μsecond. With reduced compensation for sine waves, the slew rate for $A_{CL} = -1$ will typically be 320V/μsecond.

All of these characteristics are well complemented by the high input impedence of these FET devices, and when combined with a minimum output capability of 30mA at 10V, both the AH103 and AH104 solve a number of problems often faced in high speed test equipment and in sonar and radar applications.

AH103/AH104 Specifications

Specifications at $T_A = +25°C$ and $V_{cc} = \pm 15$ VDC unless otherwise specified

Parameter	Condition	Min	Typ	Max	Units
Open-Loop Gain, DC					
Full Load	$V_O = \pm 10V$; $R_L = 330\Omega$	80	86		dB
No Load			88		dB
Rated Output					
Voltage	$I_O = \pm 30mA$	± 10	± 12		V
Current	$V_O = \pm 10V$	± 30	± 50		mA
Output Resistance	Open Loop		100		Ω
Short Circuit Current	Internal Limits			± 100	mA
Capacitive Load, $A_{CL} = -1$	(C_C = 20pF on AH104)	500			pF
Input Bias Current					
Initial Bias			35	100	pA
vs Temperature	0°C to +70°C		Note 1		
vs Supply Voltage			0.2		pA/V
Input Impedance					
Differential Resistance			10^{11}		Ω
Differential Capacitance			3		pF
Common-Mode Resistance			10^{11}		Ω
Common-Mode Capacitance			3		pF
Input Voltage Range					
Common-Mode Voltage Range	Linear Operation		+5/−10		V
Common-Mode Rejection	1KHz	58			dB
Power Supply Requirements					
Rated Voltage			± 15		V
Voltage Range	Derated Performance	± 10		± 20	
Current, Quiescent	$V_{CC} = \pm 15V$		± 16	± 19	mA
Temperature Range					
Specifications		0		70	°C
Derated Operation		−25		+100	°C
Storage		−65		+150	°C

Dynamic Response AH104

Parameter	Condition	Min	Typ	Max	Units
Gain-Bandwidth Product					
$A_{CL} = -30$		400	450		MHz
$A_{CL} = -1$	$C_C = 10pF$, $C_f = 2pF$		35		MHz
Slew Rate	$R_L = 330\Omega$, $V_O = \pm 10V$ Step Function				
$A_{CL} = -1$	$C_C = 17pF$, $C_f = 5pF$	220	270		V/μsec
Full Power Bandwidth	$R_L = 330\Omega$, $V_O = \pm 10V$ AC				
$A_{CL} = -1$	$C_C = 10pF$, $C_f = 5pF$	4.8	5.2		MHz
Settling Time, $A_{CL} = -1$	$C_C = 17pF$, $R_L = 330\Omega$				
$\epsilon = 1\%$	$C_f = 5pF$, $V_O = \pm 10V$ Step Function		80	100	ns
$\epsilon = 0.1\%$			130	160	ns
$\epsilon = 0.01\%$			240		ns
Small-Signal Overshoot	$C_C = 17pF$, $R_L = 330\Omega$				
$A_{CL} = -1$	$C_f = 5pF$		2	10	%

Dynamic Response AH103

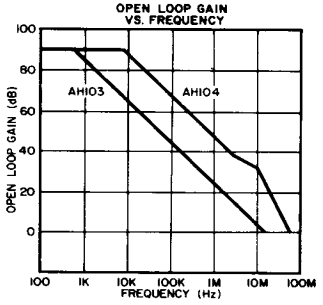
Parameter	Condition	Min	Typ	Max	Units
Gain-Bandwidth Product					
$A_{CL} = -30$			100		MHz
$A_{CL} = -1$	$C_f = 2pF$		18		MHz
Slew Rate	$R_L = 330\Omega$, $V_O = \pm 10V$ Step Function				
	$C_f = 5pF$	190	230		V/μsec
Full Power Bandwidth	$R_L = 330\Omega$, $V_O = \pm 10V$ AC				
$A_{CL} = -1$	$C_f = 5pF$	3.0	3.7		MHz
Settling Time, $A_{CL} = -1$	$R_L = 330\Omega$				
$\epsilon = 1\%$	$C_f = 5pF$, $V_O = \pm 10V$ Step Function		90	120	ns
$\epsilon = 0.1\%$			150	200	ns
$\epsilon = 0.01\%$			250		ns
Small-Signal Overshoot					
$A_{CL} = -1$	$R_L = 330\Omega$, $C_f = 5pF$		2	10	%

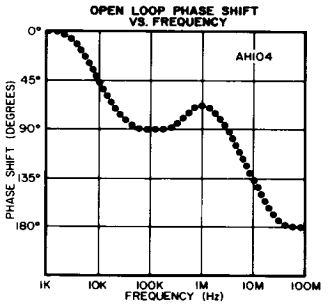
Note 1: Doubles every 10°C

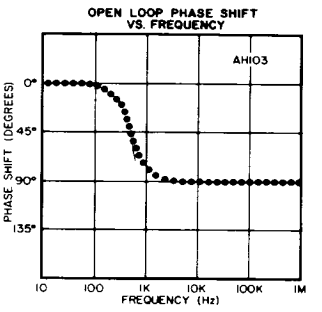
Input Offset Voltage

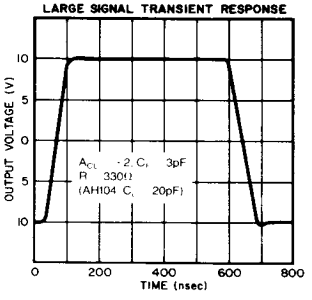
Parameter	Condition	AH103CJ AH104CJ	AH103CK AH104CK	AH103CL AH104CL	Units
Voltage Noise Spectral Density Rs≤100 Ω		Voltage		Current	
		$NV/\sqrt{Hz}$		$A/\sqrt{Hz}$	
		20		10fA	
Initial Offset	+25°C	±2.0	±1.0	±1.0	mVmax
vs. Temperature	0°C to 70°C	±20	±10	±5	µV/°Cmax
vs. Supply Voltage		±1.0	±1.0	±1.0	mV/V max
Adjustment Range		±25	±25	±25	mV typ

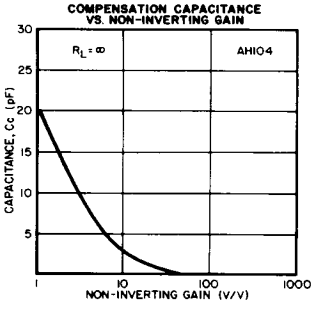
Typical Performance Curves

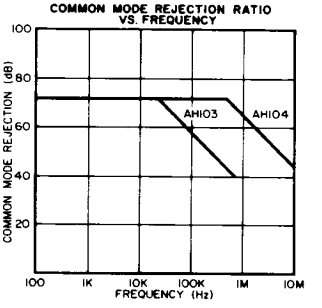


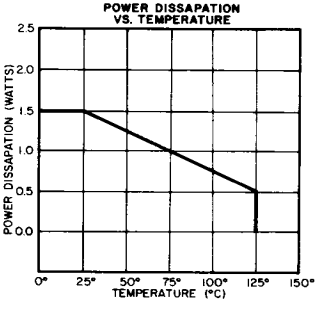


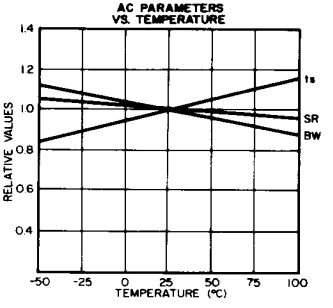


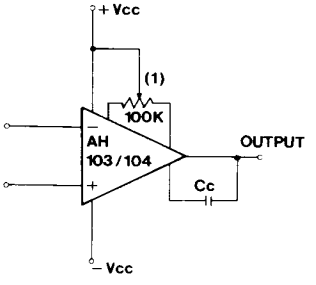








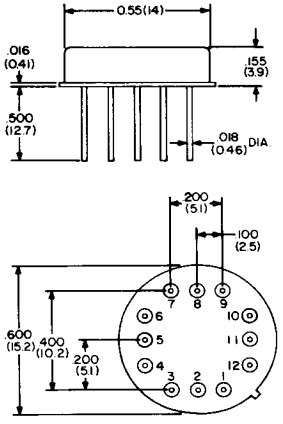




(1) Offset Voltage Adjustment

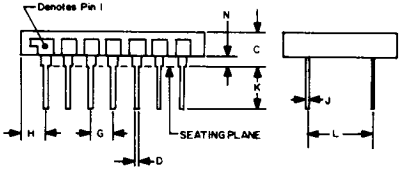
Mechanical Description

The AH103/AH104 package is a standard 12-pin TO-8 package.



Bottom View

1) No Connection
2) Offset Adjust
3) − Input
4) + Input
5) − Vcc
6) No Connection
7) No Connection
8) Offset Adjust
9) Output
10) + Vcc
11) Compensation
12) Case Ground



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.770	.810	19.56	20.57
B	.480	.500	12.19	12.70
C	.155	.215	3.94	5.46
D	.016	.020	.41	.51
G	.100 NOM.		2.54 NOM.	
H	.080	.110	2.03	2.79
J	.009	.012	.23	.30
K	.150	.210	3.81	5.33
L	.300 NOM		7.62 NOM.	
N	.015	.035	.38	.89

NOTES:
1. LEADS IN TRUE POSITION WITHIN .010" (.255mm)

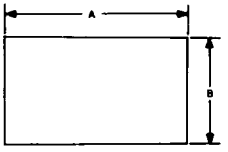
Absolute Maximum Ratings

Supply	±20VDC
Internal Power Dissipation	(1)
Differential Input Voltage	±20VDC
Input Voltage, Either Input(2)	±20VDC
Storage Temperature Range	−55°C to +125°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-Circuit Duration(3)	Continuous

Notes
1) Package must be derated according to details in the Applications information section.
2) For supply voltages less than ±20VDC, the absolute maximum input is equal to the supply voltage.
3) Short circuit to ground only. See Short Circuit Protection discussion in the Application Information section.

AH 103/104DJ

PIN CONNECTIONS
1 NO CONNECTION
2 NO CONNECTION
3 OFFSET ADJUST
4 INVERTING INPUT
5 NON-INVERTING INPUT
6 −Vcc
7 NO CONNECTION
8 NO CONNECTION
9 OFFSET ADJUSTMENT
10 OUTPUT
11 +Vcc
12 FREQUENCY COMPENSATION
13 NO CONNECTION
14 NO CONNECTION



Application Information

The basic difference between the AH103 and the AH104 is the internal 20pF compensating capacitor used on the AH103 to provide inverting unity gain stability. This may simplify board layout and reduce component count, and hence may be advantageous in specific designs. The AH104 is uncompensated internally, allowing the user to optimize the normal trade-offs associated with slew rate, stability, bandwidth, settling time, etc. The compensation capacitor needed depends on the waveform, frequency and gain requirements of the system. A typical performance curve shows the C_c normally required to stabilize the AH104 for pulse applications at various non-inverting gains.

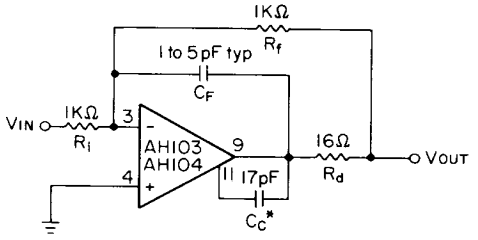
Basic Operation

Figure 1 shows the basic connections in a typical unity gain inverting circuit. The use of a compensation capacitor (C_c) is required on the AH104, unless the gain is fairly high, while the AH103 would only need additional external compensation in special cases, such as when used as a non-inverting unity gain follower. Compensation is done between pins 11 and 9.

Frequency stability, especially with capacitive loads, can be improved by a small resistor in series with the output. (R_d in Figure 1.)

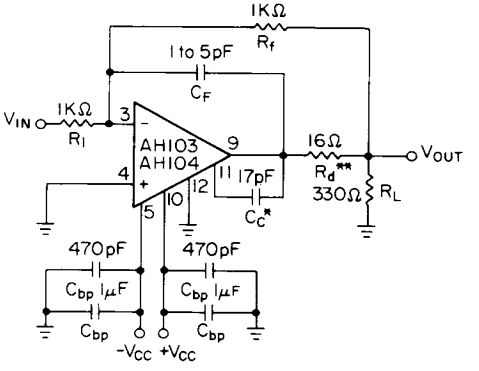
Closed loop frequency response can be considerably improved by use of a small feedback capacitor. This capacitor also reduces peaking at high frequencies. The capacitor (C_f in the figures) will compensate for a pole in the closed loop transfer function caused by the input capacitance and feedback resistors.

Figure 1: Unity Gain Inverting



*Not needed on the AH103

Figure 2: Pulse Amplifier Test Circuit



Not needed for the AH103

**R_d especially critical for capacitive loads. May be unneeded on resistive loads.

Circuit Layout

Grounding is critical on the AH103/AH104, as on any high speed devices. Whenever possible, a ground plane should be used, covering as much of the circuit board as possible to provide low resistance and low impedance paths for all signal and power common returns.

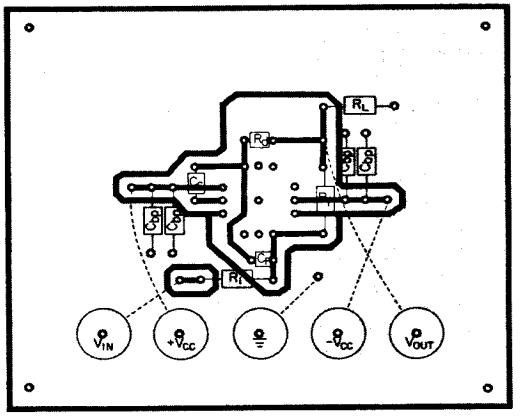
If a ground plane is not practical, we recommend use of a single point ground, where all of the signal and power common returns are made. This will help eliminate ground loops or common current paths which could cause signal modulation or unwanted feedback.

Although they are not exceptionally sensitive, it is recommended that power supplies should be bypassed as close as possible to the supply pins of the AH103/AH104. Similarly, leads or traces should be kept as short as possible, to minimize stray capacitances. This is most important at the inverting input (pin 3).

Feedback resistors should be kept as small as practical, in part to keep associated time constants low. If possible, they should not exceed 5.6KΩ. Lower limits are normally determined by the signal source and gain requirements.

Figures 2 and 3 show the complete circuit for an inverting unity gain pulse amplifier test board and a suggested board layout.

Figure 3: Pulse Amplifier Suggested Layout



Short Circuit Protection

Internal current limiting resistors provide short circuit protection to the common line, with a limit of 100mA maximum. A short to either supply line can destroy the unit.

For high current applications, or where shorts are a possibility, the power dissipation curve in the Typical Performance Curve section needs to be taken into consideration.

Figure 4: Video Amplifier

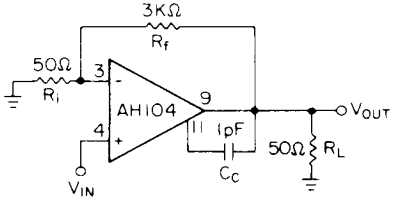
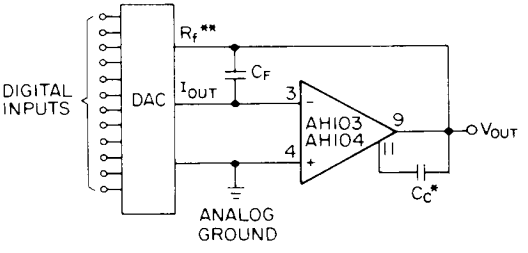


Figure 5: DAC Output Amplifier



Optional on the AH103

**Often denoted as R_{FB} or span adjust in DAC data sheets.

Offset Null
If the low initial offset of the AH103/AH104 needs to be further reduced, offset adjust pins 2 and 8 can be used. A 20KΩ potentiometer should be tied between pins 2 and 8, with the wiper tied to the positive supply. (Care should be taken to prevent the wiper from being at either end of the pot, which would short the supply line to an adjust pin, possibly damaging the unit.) With the analog input to the circuit grounded, adjust the pot for zero output.

Adjusting the offset normally affects offset drift, sometimes increasing it significantly. Thus, if adjustment is required, it should be performed with the AH103/AH104 as close as possible to expected operating temperature.

Typical Circuits
Figure 4 shows the AH104 used as a high gain video amplifier. Its high output current capability makes it suitable for such high frequency driver applications. In this circuit, a closed loop gain of 60 can be obtained to 10MHz. For lower gains, C_c would need to be larger to promote stability.

The AH103 could also be used in the circuit, without C_c, but the internal 20pF compensation capacitor would reduce the gain at any given bandwidth.

Figure 5 shows the basic connections for using the AH103/AH104 as an output amplifier for current output digital to analog converters. The FET input, high output current and fast settling time make the AH103/AH104 useful for various DAC applications.

For use with a fast settling current DAC, such as the AD565A, an overall DAC plus amp voltage output settling time of about 300ns can be achieved, with the advantages of 30mA drive capability, and the ability to drive capacitive loads. (Total settling time is the root mean square of the DAC settling time and the AH103/AH104 settling time.)

For use with a CMOS DAC, such as the AD7545, the FET input helps overcome the varying output impedance of the DAC, which is digital input code dependent. If the DAC has a differential nonlinearity of ½ LSB, it needs to be matched with an amplifier with less than ½ LSB of offset error to remain monotonic. For a 12 bit 0 to 10V output, ½ LSB is 1.22mV (1LSB = 10 volts/4096.) Thus, the AH103CK, AH103CL, AH104CK or AH104CL would add less than ½ LSB to differential linearity.

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