W238-02

FTG for Integrated Core Logic with 133-MHz FSB

Features

- **Maximized EMI suppression using Cypress's Spread Spectrum technology**
- **Low jitter and tightly controlled clock skew**
- **Highly integrated device providing clocks required for CPU, core logic, and SDRAM**
- **Two copies of CPU clock at 66/100/133 MHz**
- **Thirteen copies of SDRAM clocks at 100/133 MHz**
- **Five copies of PCI clock compliant to PCI spec 2-1 and capable of driving a maximum load of 40 pF**
- **One copy of synchronous APIC clock**
- **Two copies of 48-MHz clock (non-spread spectrum) optimized for USB reference input and video dot clock**
- **Three copies of 66-MHz fixed clock**
- **One copy of 14.31818-MHz reference clock**
- **Power down control**
- **SMBus interface for turning off unused clocks**

Key Specifications

CPU, SDRAM Outputs Cycle-to-Cycle Jitter:.............. 250 ps

APIC, 48-MHz, 3V66, PCI Outputs
Cycle-to-Cycle Jitter:.. 500 ps

APIC, 48-MHz, SDRAM Output Skew:........................250 ps

CPU, 3V66 Output Skew:...175 ps

PCI Output Skew:...500 ps

CPU to SDRAM Skew (@ 133 MHz):.........................±0.5 ns

CPU to SDRAM Skew (@ 100 MHz):.................4.5 to 5.5 ns

CPU to 3V66 Skew (@ 66 MHz): ....7.0 to 8.0 ns

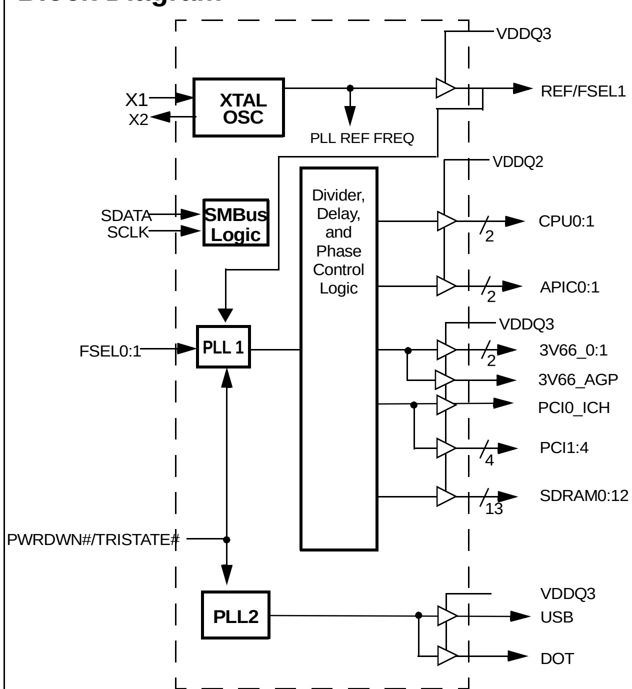
3V66 to PCI Skew (3V66 lead):..........................1.5 to 3.5 ns

PCI to APIC Skew: ....±0.5 ns

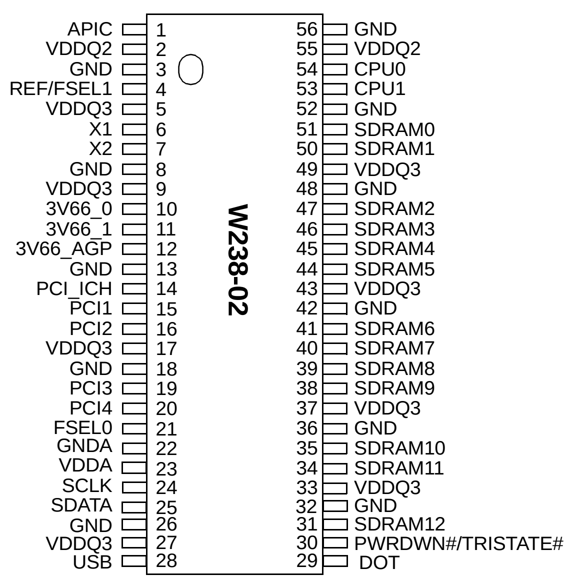
Table 1. Pin Selectable Functions

Tristate#	FSEL1	FSEL0	Function	SDRAM
0	X	0	Three -State	Three-State
0	X	1	Test	Test
1	0	0	66 MHz	100 MHz
1	0	1	100 MHz	100 MHz
1	1	0	133 MHz	133 MHz
1	1	1	133 MHz	100 MHz

Block Diagram



Pin Configuration



Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
REF/FSEL1	4	I/O	***Reference Clock/Function Select:*** 3.3V 14.318-MHz clock output. This pin also serves as a strap option for CPU frequency selection. See *Table 1* for detailed descriptions.
X1	6	I	***Crystal Input:*** This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.
X2	7	I	***Crystal Output:*** An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
PCI0_ICH, PCI1:4	14, 15, 16, 19, 20	O	***PCI Clock 0 through 4:*** 3.3V 33-MHz PCI clock outputs. PCI1:4 can be individually turned off via SMBus interface.
3V66_0:1 3V66_AGP	10, 11, 12	O	***66-MHz Clock Output:*** 3.3V fixed 66-MHz clock.
USB	28	O	***USB Clock Output:*** 3.3V fixed 48-MHz, non-spread spectrum USB clock outputs.
DOT	29	O	***Dot Clock Output:*** 3.3V 48-MHz, non-spread spectrum signal.
FSEL0	21	I	***Clock Function Selection Pins:*** LVTTL-compatible input (latched) to select device functions. See *Table 1* for detailed descriptions. This is a latched input. The status of this pin will be ignore after the internal POR.
PWRDWN#/ TRISTATE#	30	I	***TRISTATE#/PWRDWN#:*** During power-up, this pin defaults to the PWRDWN# input function. This pin can be configured as the TRISTATE# input function by control register at Byte[3], Bit[1]. This input can be used as the VTT_PWRGD input to support Intel® VRM 8.5 implementation.
CPU0:1	54, 53	O	***CPU Clock Outputs:*** Clock outputs for the host bus interface and integrated test port. Output frequencies run at 66 MHz, 100 MHz, or 133 MHz, depending on the configuration of FSEL0:1 and TRISTATE#. Voltage swing set by V_{DDQ2}.
SDRAM0:12	51, 50, 47, 46, 45, 44, 41, 40, 39, 38, 35, 34, 31	O	***SDRAM Clock Outputs:*** 3.3V outputs running to 133 MHz. SDRAM0:7 can be individually turned off via SMBus interface.
APIC	1	O	***Synchronous APIC Clock Outputs:*** Clock outputs running synchronous with the PCI clock outputs (33 MHz). Voltage swing set by V_{DDQ2}.
SDATA	25	I/O	Data pin for SMBus circuitry.
SCLK	24	I	Clock pin for SMBus circuitry.
VDDQ3	5, 9, 17, 27, 33, 37, 43, 49	P	***3.3V Power Connection:*** Power supply for SDRAM output buffers, PCI output buffers, 3V66 output buffers, reference output buffers, and 48-MHz output buffers. Connect to 3.3V.
VDDA	23	O	***3.3V Power Connection:*** Power supply for core logic, PLL circuitry. Connect to 3.3V.
VDDQ2	2, 55	P	***2.5V Power Connection:*** Power supply for IOAPIC and CPU output buffers. Connect to 2.5V or 3.3V.
GNDA	22	G	***Ground Connections:*** Ground for core logic, PLL circuitry.
GND	3, 8, 13, 18, 26, 32, 36, 42, 48, 52, 56	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.

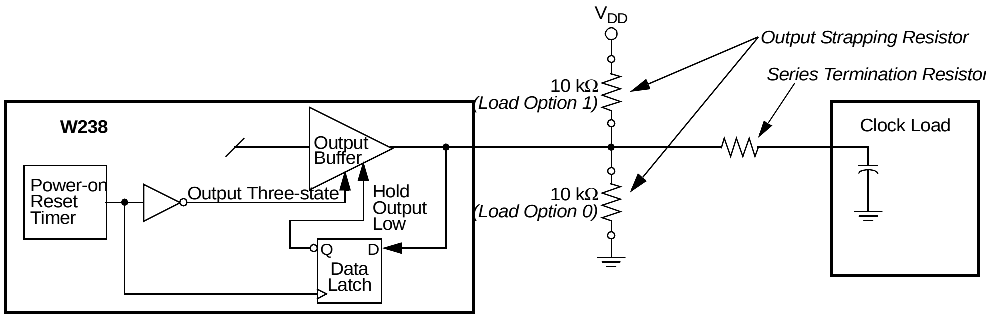


Figure 1. Input Logic Selection Through Resistor Load Option

Overview

The W238 is a highly integrated frequency timing generator, supplying all the required clock sources for an Intel architecture platform using graphics integrated core logic.

Functional Description

I/O Pin Operation

REF/SEL1 is a dual-purpose I/O pin. Upon power-up the pin acts as a logic input. CPU clock outputs will be determined by the status of FSEL0:1 input pins. An external 10-kΩ strapping resistor should be used. *Figure 1* shows a suggested method for strapping resistor connections.

After 2 ms, the pin becomes an output. Assuming the power supply has stabilized by then, the specified output frequency is delivered on the pins. If the power supply has not yet reached full value, output frequency initially may be below target but will increase to target once supply voltage has stabilized. In either case, a short output clock cycle may be produced from the CPU clock outputs when the outputs are enabled.

Pin Selectable Functions

Table 1 outlines the device functions selectable through Tristate# and FSEL0:1. Specific outputs available at each pin are detailed in *Table 2* below.

Table 2. CK Solano Truth Table

Tristate#	FSEL1	FSEL0	CPU	SDRAM	3V66	PCI	48MHz	REF	APIC	Notes
0	X	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	1
0	X	1	TCLK/4	TCLK/4	TCLK/6	TCLK/12	TCLK/2	TCLK	TCLK/12	2, 3
1	0	0	66 MHz	100 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	33 MHz	4, 5, 6
1	0	1	100 MHz	100 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	33 MHz	4, 5, 6
1	1	1	133 MHz	133MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	33 MHz	1, 3, 5
1	1	1	133 MHz	100 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	33 MHz	1, 3, 5

Notes:

1. Provided for board-level “bed of nails” testing.
2. TCLK is a test clock overdriven on the XTAL_IN input during test mode.
3. Required for DC output impedance verification.
4. “Normal” mode of operation.
5. Range of reference frequency allowed is min. = 14.316 MHz, nominal = 14.31818 MHz, max. = 14.32 MHz.
6. Frequency accuracy of 48 MHz must be +167 PPM to match USB default.

How to use PD# input to support VTT_PWRGD

The PD# input can be used to support the VTT_PWRGD signal specified in the Intel VRM 8.5 specification. The VTT_PWRGD is used to indicated that the frequency select output pins (BSEL[0:1]) from the CPU are valid and the clock generator can use them to determine the CPU FSB frequency. The assertion of PD# input pin during initial power-up will delay the start of the PLL, keep all the multiplexed I/O pins as input and keep all the output inactive. The functionality of PD# will allow the system designer to use this input to support the VTT_PWRGD output from the VRM 8.5 module. Please refer to the *Figure 2* for power-up sequence details.

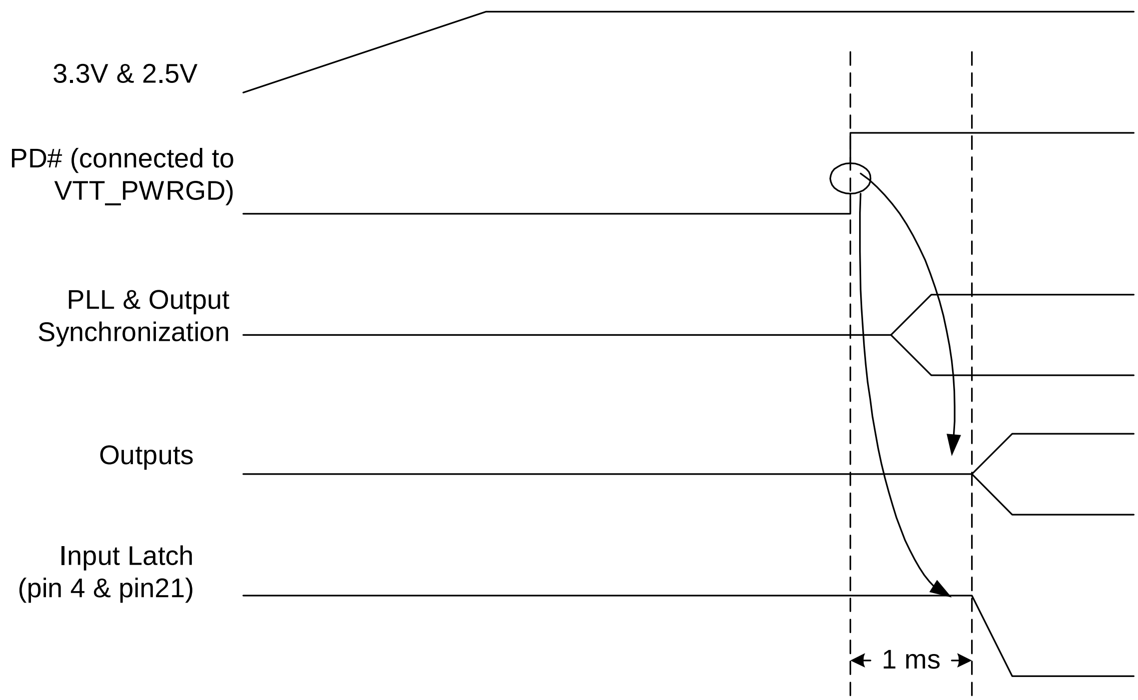


Figure 2. Power-up sequence with PD# (VTT_PWRGD) hold LOW

Offsets Among Clock Signal Groups

Figure 3 and *Figure 4* represent the phase relationship among the different groups of clock outputs from W238 when it is providing a 66-MHz CPU clock and a 100-MHz CPU clock, respectively. It should be noted that when CPU clock is operating at 100 MHz, CPU clock output is 180 degrees out of phase with SDRAM clock outputs.

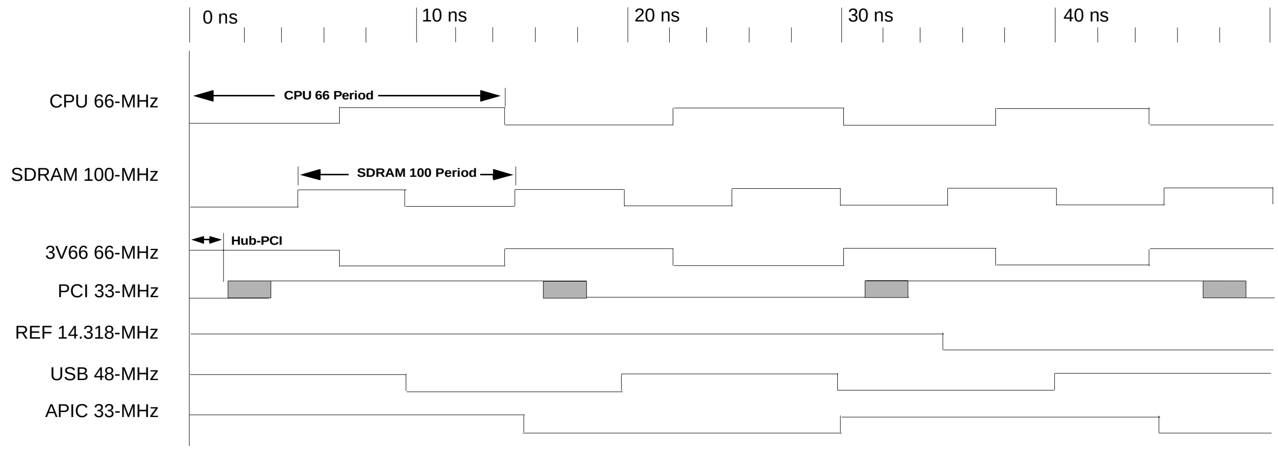


Figure 3. Group Offset Waveforms (66-MHz CPU/100-MHz SDRAM)

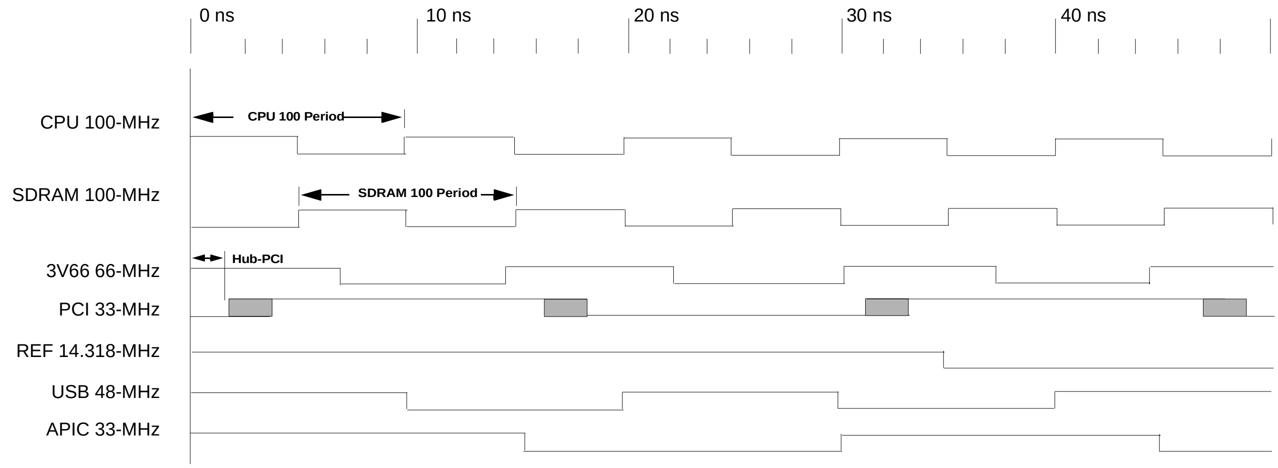


Figure 4. Group Offset Waveforms (100-MHz CPU/100-MHz SDRAM)

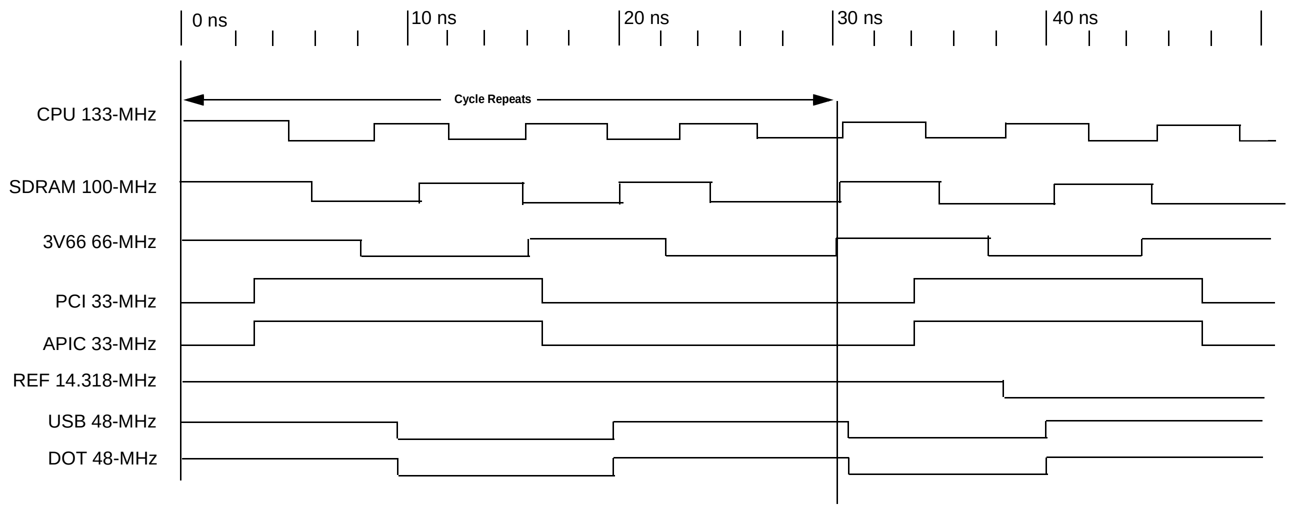


Figure 5. Group Offset Waveforms (133-MHz CPU/100-MHz SDRAM)

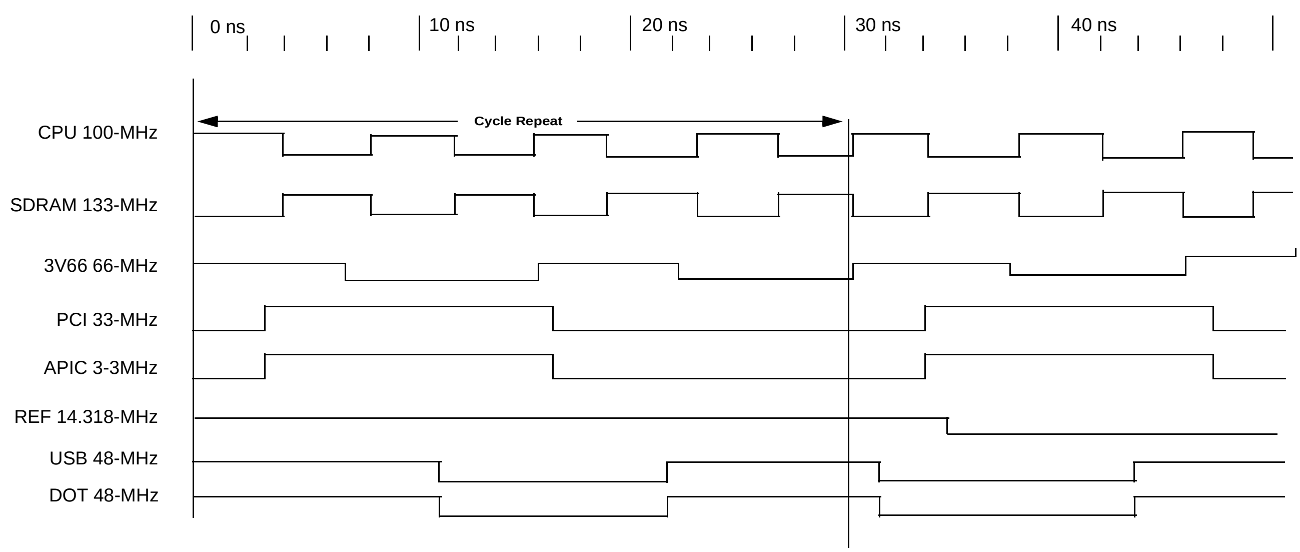


Figure 6. Group Offset Waveform (133-MHz CPU/133-MHz SDRAM)

Power Down Control

W238 provides one PWRDWN# signal to place the device in low-power mode. In low-power mode, the PLLs are turned off and all clock outputs are driven LOW.

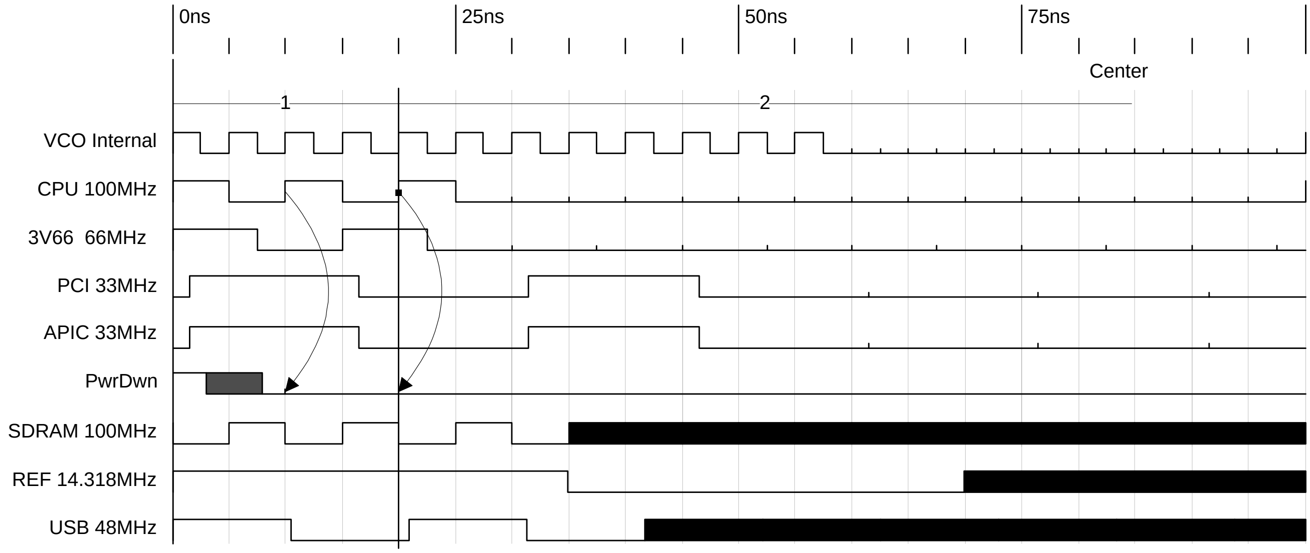


Figure 7. W238 PWRDWN# Timing Diagram[7, 8, 9, 10]

Table 3. W238 Maximum Allowed Current

W238 Condition	Max. 2.5V supply consumption Max. discrete cap loads, $V_{DDQ2} = 2.625V$ All static inputs = V_{DDQ3} or V_{SS}	Max. 3.3V supply consumption Max. discrete cap loads $V_{DDQ3} = 3.465V$ All static inputs = V_{DDQ3} or V_{SS}
Powerdown Mode (PWRDWN# = 0)	100 µA	500 µA
Full Active 66 MHz FSEL1:0 = 00 (PWRDWN# =1)	30 mA	280 mA
Full Active 100 MHz FSEL1:0 = 01 (PWRDWN# =1)	40 mA	280 mA
Full Active 133 MHz FSEL1:0 = 10, 11 (PWRDWN# =1)	50 mA	400 mA

Notes:

7. Once the PWRDWN# signal is sampled LOW for two consecutive rising edges of CPU, clocks of interest will be held LOW on the next HIGH-to-LOW transition.
8. PWRDWN# is an asynchronous input and metastable conditions could exist. This signal is synchronized inside W238.
9. The shaded sections on the SDRAM, REF, and USB clocks indicate “Don’t Care” states.
10. Diagrams shown with respect to 100 MHz. Similar operation when CPU is 66 MHz.

Spread Spectrum Frequency Timing Generator

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 8*.

As shown in *Figure 8*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is:

$$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$$

Where *P* is the percentage of deviation and *F* is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 9*. This waveform, as discussed in “Spread Spectrum Clock Generation for the Reduction of Radiated Emissions” by Bush, Fessler, and Hardin, produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is –0.5% of the selected frequency. *Figure 9* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

Spread Spectrum clocking is activated or deactivated by selecting the appropriate value for bit 3 in data byte 0 of the SMBus data stream. Refer to page 10 for more details.

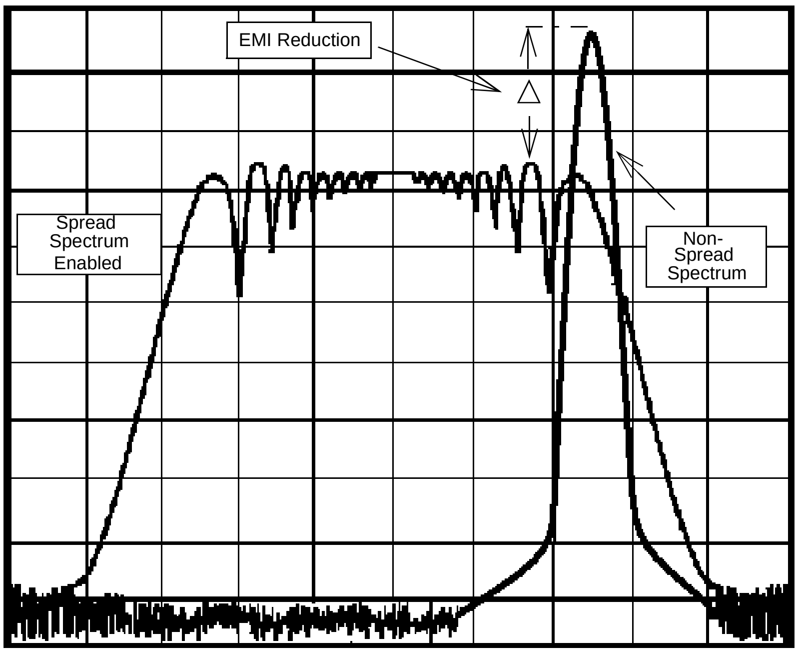


Figure 8. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation

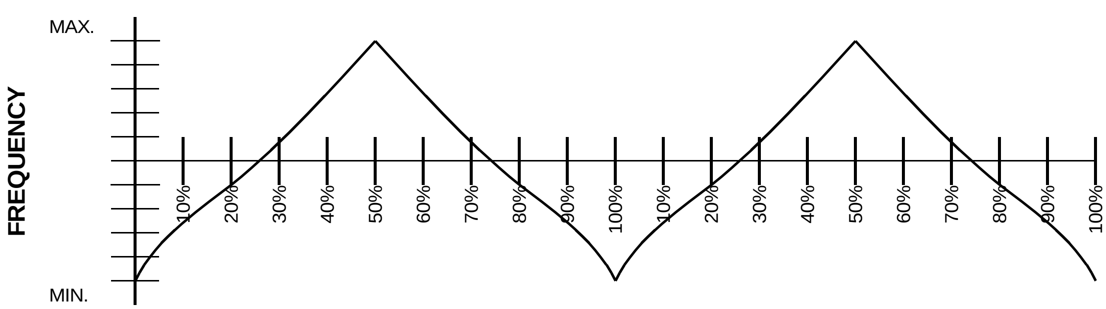


Figure 9. Typical Modulation Profile

1 bit	7 bits	1	1	8 bits	1	
Start bit	Slave Address	R/W	Ack	Command Code	Ack	Byte Count = N

Ack	Data Byte 1	Ack	Data Byte 2	Ack	...	Data Byte N	Ack	Stop
1 bit	8 bits	1	8 bits	1		8 bits	1	1

Figure 10. An Example of a Block Write[11]

Serial Data Interface

The W238 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions.

Data Protocol

The clock driver serial protocol accepts only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. Indexed bytes are not allowed.

A block write begins with a slave address and a write condition. After the command code the core logic issues a byte count which describes how many more bytes will follow in the message. If the host had 20 bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count may not be 0. A block write command is allowed to transfer a maximum of 32 data bytes. The slave receiver address for W238 is 11010010. *Figure 10* shows an example of a block write.

The command code and the byte count bytes are required as the first two bytes of any transfer. W238 expects a command code of 0000 0000. The byte count byte is the number of additional bytes required for the transfer, not counting the command code and byte count bytes. Additionally, the byte count byte is required to be a minimum of 1 byte and a maximum of 32 bytes to satisfy the above requirement. *Table 4* shows an example of a possible byte count value.

A transfer is considered valid after the acknowledge bit corresponding to the byte count is read by the controller. The command code and byte count bytes are ignored by the W238. However, these bytes must be included in the data write sequence to maintain proper byte allocation.

Table 4. Example of Possible Byte Count Value

Byte Count Byte		Notes
MSB	LSB	
0000	0000	Not allowed. Must have at least one byte
0000	0001	Data for functional and frequency select register (currently byte 0 in spec)
0000	0010	Reads first two bytes of data. (byte 0 then byte 1)
0000	0011	Reads first three bytes (byte 0, 1, 2 in order)
0000	0100	Reads first four bytes (byte 0, 1, 2, 3 in order)
0000	0101	Reads first five bytes (byte 0, 1, 2, 3, 4 in order)[12]
0000	0110	Reads first six bytes (byte 0, 1, 2, 3, 4, 5 in order)[12]
0000	0111	Reads first seven bytes (byte 0, 1, 2, 3, 4, 5, 6 in order)
0010	0000	Max. byte count supported = 32

Table 5. Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held LOW.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots.
Spread Spectrum Enabling	Enables or disables spread spectrum clocking.	For EMI reduction.
(Reserved)	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

Notes:
11. The acknowledgment bit is returned by the slave/receiver (W238).
12. Data Bytes 3 to 7 are reserved.

W238 Serial Configuration Map

1. The serial bits will be read by the clock driver in the following order:

   Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

   Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

   Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

2. All unused register bits (reserved and N/A) should be written to a “0” level.
3. All register bits labeled “Initialize to 0" must be written to zero during initialization. Failure to do so may result in higher than normal operating current. The controller will read back the written value.

Byte 0: Control Register (1 = Enable, 0 = Disable)[13]

Bit	Pin#	Name	Default	Pin Function
Bit 7	-	Reserved	0	Reserved
Bit 6	-	Reserved	0	Reserved
Bit 5	-	Reserved	0	Reserved
Bit 4	-	Reserved	0	Reserved
Bit 3	-	Spread Spectrum (1 = On/0 = Off)[14]	0	(Disabled/Enabled)
Bit 2	29	DOT	1	(Active/Inactive)
Bit 1	28	USB	1	(Active/Inactive)
Bit 0	-	Reserved	0	Reserved

Byte 1: Control Register (1 = Enable, 0 = Disable)[13]

Bit	Pin#	Name	Default	Pin Description
Bit 7	40	SDRAM7	1	(Active/Inactive)
Bit 6	41	SDRAM6	1	(Active/Inactive)
Bit 5	44	SDRAM5	1	(Active/Inactive)
Bit 4	45	SDRAM4	1	(Active/Inactive)
Bit 3	46	SDRAM3	1	(Active/Inactive)
Bit 2	47	SDRAM2	1	(Active/Inactive)
Bit 1	50	SDRAM1	1	(Active/Inactive)
Bit 0	51	SDRAM0	1	(Active/Inactive)

Notes:

Byte 2: Control Register (1 = Enable, 0 = Disable)

Bit	Pin#	Name	Default	Pin Description
Bit 7	12	3V66_AGP	1	(Active/Inactive)
Bit 6	31	SDRAM12	1	(Active/Inactive)
Bit 5	34	SDRAM11	1	(Active/Inactive)
Bit 4	35	SDRAM10	1	(Active/Inactive)
Bit 3	38	SDRAM9	1	(Active/Inactive)
Bit 2	39	SDRAM8	1	(Active/Inactive)
Bit 1	15	PCI1	1	(Active/Inactive)
Bit 0	--	Reserved	1	(Active/Inactive)

Notes:

13. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
14. Spread Spectrum percentage is –0.5%.

Byte 3: Reserved Register (1 = Enable, 0 = Disable)

Bit	Pin#	Name	Default	Pin Description
Bit 7	-	Reserved	0	Reserved
Bit 6	-	Reserved	0	Reserved
Bit 5	-	Reserved	0	Reserved
Bit 4	-	Reserved	0	Reserved
Bit 3	--	Reserved	0	Reserved
Bit 2	--	Reserved	0	Reserved
Bit 1	30	PWRDWN#/ TRISTATE#	1	1 = PWRDWN# 0 = TRISTATE#
Bit 0	--	SDRAM 133 Mode Enable Disabled ='0', Enabled ='1'	0	(Disabled/Enabled)

Byte 4: Reserved Register (1 = Enable, 0 = Disable)

Bit	Pin#	Name	Default	Pin Function
Bit 7	-	Reserved	0	Reserved
Bit 6	-	Reserved	0	Reserved
Bit 5	-	Reserved	0	Reserved
Bit 4	-	Reserved	0	Reserved
Bit 3	-	Reserved	0	Reserved
Bit 2	20	PCI4	1	Active/Inactive
Bit 1	19	PCI3	1	Active/Inactive
Bit 0	16	PCI2	1	Active/Inactive

Byte 5: Reserved Register (1 = Enable, 0 = Disable)

Bit	Pin#	Name	Default	Pin Description
Bit 7	-	Reserved	0	Reserved
Bit 6	-	Reserved	0	Reserved
Bit 5	-	Reserved	0	Reserved
Bit 4	-	Reserved	0	Reserved
Bit 3	-	Reserved	0	Reserved
Bit 2	-	Reserved	0	Reserved
Bit 1	-	Reserved	0	Reserved
Bit 0	-	Reserved	0	Reserved

Byte 6: Reserved Register (1 = Enable, 0 = Disable)

Bit	Pin#	Name	Default	Pin Description
Bit 7	-	Reserved	0	Reserved
Bit 6	-	Reserved	0	Reserved
Bit 5	-	Reserved	0	Reserved
Bit 4	-	Reserved	0	Reserved
Bit 3	-	Reserved	0	Reserved
Bit 2	-	Reserved	0	Reserved
Bit 1	-	Reserved	0	Reserved
Bit 0	-	Reserved	0	Reserved

DC Electrical Characteristics[15]

Absolute Maximum DC Power Supply

Parameter	Description	Min.	Max.	Unit
V_{DD3}	3.3V Core Supply Voltage	–0.5	4.6	V
V_{DDQ2}	2.5V I/O Supply Voltage	–0.5	3.6	V
V_{DDQ3}	3.3V Supply Voltage	–0.5	4.6	V
T_S	Storage Temperature	–65	150	°C

Absolute Maximum DC I/O

Parameter	Description	Min.	Max.	Unit
V_{ih3}	3.3V Input High Voltage	–0.5	4.6	V
V_{il3}	3.3V Input Low Voltage	–0.5		V
ESD prot.	Input ESD Protection	2000		V

DC Operating Requirements

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{DD3}	3.3V Core Supply Voltage	3.3V ±5%	3.135		3.465	V
V_{DDQ3}	3.3V I/O Supply Voltage	3.3V ±5%	3.135		3.465	V
V_{DDQ2}	2.5V I/O Supply Voltage	2.5V ±5%	2.375		2.625	V
V_{DD3} = 3.3V±5%						
V_{ih3}	3.3V Input High Voltage	V_{DD3}	2.0		V_{DD} + 0.3	V
V_{il3}	3.3V Input Low Voltage		V_{SS} – 0.3		0.8	V
I_{il}	Input Leakage Current[16]	$0<V_{in}<V_{DD3}$	–5		+5	µA
V_{DDQ2} = 2.5V±5%						
V_{oh2}	2.5V Output High Voltage	I_{oh} = (–1 mA)	2.0			V
V_{ol2}	2.5V Output Low Voltage	I_{ol} = (1 mA)			0.4	V
V_{DDQ3} = 3.3V±5%						
V_{oh3}	3.3V Output High Voltage	I_{oh} = (–1 mA)	2.4			V
V_{ol3}	3.3V Output Low Voltage	I_{ol} = (1 mA)			0.4	V
V_{DDQ3} = 3.3V±5%						
V_{poh3}	PCI Bus Output High Voltage	I_{oh} = (–1 mA)	2.4			V
V_{pol3}	PCI Bus Output Low Voltage	I_{ol} = (1 mA)			0.55	V
C_{in}	Input Pin Capacitance				5	pF
C_{xtal}	Xtal Pin Capacitance		13.5		22.5	pF
C_{out}	Output Pin Capacitance				6	pF
L_{pin}	Pin Inductance		0		7	nH
T_a	Ambient Temperature	No Airflow	0		70	°C

Note:

15. The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT requried.
16. Input Leakage Current does not include inputs with pull-up or pull-down resistors.

DC Operating Requirements (continued)

Parameter	Description		Condition	Min.	Typ.	Max.	Unit
I_{OL}	Output Low Current	PCI0:7	V_{OL} = 1.5V	20	40	90	mA
		REF2X/FS3	V_{OL} = 1.5V	20	40	90	mA
		48 MHz	V_{OL} = 1.5V	20	40	90	mA
		24 MHz	V_{OL} = 1.5V	20	40	90	mA
		SDRAM0:12	V_{OL} = 1.5V	60	100	160	mA
		CPU0:1	V_{OL} = 1.25V	25	50	95	mA
I_{OH}	Output High Current	PCI0:7	V_{OH}= 1.5V	20	40	90	mA
		REF2X/FS3	V_{OH}= 1.5V	20	40	90	mA
		48 MHz	V_{OH}= 1.5V	20	40	90	mA
		24 MHz	V_{OH}= 1.5V	20	40	90	mA
		SDRAM0:12	V_{OH}= 1.5V	60	100	160	mA
		CPU0:1	V_{OH}= 1.25V	25	50	95	mA

AC Electrical Characteristics[15]

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V ±5%, V_{DDQ2}= 2.5V ±5%
f_{XTL} = 14.31818 MHz
Spread Spectrum function turned off

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.[17]

Parameter	Description	66.6-MHz Host		100-MHz Host		133-MHz Host		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
T_{Period}	Host/CPUCLK Period	15.0	15.5	10.0	10.5	7.5	8.0	ns	17
T_{HIGH}	Host/CPUCLK High Time	5.2	N/A	3.0	N/A	1.87	N/A	ns	18
T_{LOW}	Host/CPUCLK Low Time	5.0	N/A	2.8	N/A	1.67	N/A	ns	19
T_{RISE}	Host/CPUCLK Rise Time	0.4	1.6	0.4	1.6	0.4	1.6	ns	
T_{FALL}	Host/CPUCLK Fall Time	0.4	1.6	0.4	1.6	0.4	1.6	ns	
T_{Period}	SDRAM CLK Period	10.0	10.5	10.0	10.5	10.0	10.5	ns	17
T_{HIGH}	SDRAM CLK High Time	3.0	N/A	3.0	N/A	3.0	N/A	ns	18
T_{LOW}	SDRAM CLK Low Time	2.8	N/A	2.8	N/A	2.8	N/A	ns	19
T_{RISE}	SDRAM CLK Rise Time	0.4	1.6	0.4	1.6	0.4	1.6	ns	
T_{FALL}	SDRAM CLK Fall Time	0.4	1.6	0.4	1.6	0.4	1.6	ns	
T_{Period}	APIC 33-MHz CLK Period	30.0	N/A	30.0	N/A	30.0	N/A	ns	17
T_{HIGH}	APIC 33-MHz CLK High Time	12.0	N/A	12.0	N/A	12.0	N/A	ns	18
T_{LOW}	APIC 33-MHz CLK Low Time	12.0	N/A	12.0	N/A	12.0	N/A	ns	19
T_{RISE}	APIC CLK Rise Time	0.4	1.6	0.4	1.6	0.4	1.6	ns	
T_{FALL}	APIC CLK Fall Time	0.4	1.6	0.4	1.6	0.4	1.6	ns	
T_{Period}	3V66 CLK Period	15.0	16.0	15.0	16.0	15.0	16.0	ns	17, 20
T_{HIGH}	3V66 CLK High Time	5.25	N/A	5.25	N/A	5.25	N/A	ns	18
T_{LOW}	3V66 CLK Low Time	5.05	N/A	5.05	N/A	5.05	N/A	ns	19
T_{RISE}	3V66 CLK Rise Time	0.5	2.0	0.5	2.0	0.5	2.0	ns	
T_{FALL}	3V66 CLK Fall Time	0.5	2.0	0.5	2.0	0.5	2.0	ns	
T_{Period}	PCI CLK Period	30.0	N/A	30.0	N/A	30.0	N/A	ns	17, 21
T_{HIGH}	PCI CLK High Time	12.0	N/A	12.0	N/A	12.0	N/A	ns	18
T_{LOW}	PCI CLK Low Time	12.0	N/A	12.0	N/A	12.0	N/A	ns	19
T_{RISE}	PCI CLK Rise Time	0.5	2.0	0.5	2.0	0.5	2.0	ns	
T_{FALL}	PCI CLK Fall Time	0.5	2.0	0.5	2.0	0.5	2.0	ns	
tp_{ZL}, tp_{ZH}	Output Enable Delay (All outputs)	1.0	10.0	1.0	10.0	1.0	10.0	ns	
tp_{LZ}, tp_{ZH}	Output Disable Delay (All outputs)	1.0	10.0	1.0	10.0	1.0	10.0	ns	
t_{stable}	All Clock Stabilization from Power-Up		3		3		3	ms	

Notes:

17. Period, jitter, offset, and skew measured on rising edge at 1.25 for 2.5V clocks and at 1.5V for 3.3V clocks.
18. The time specified is measured from when V_{DDQ3} achieves its nominal operating level (typical condition V_{DDQ3} = 3.3V) until the frequency output is stable and operating within specification.
19. T_{RISE} and T_{FALL} are measured as a transition through the threshold region V_{ol} = 0.4V and V_{oh} = 2.0V (1 mA) JEDEC specification.
20. T_{LOW} is measured at 0.4V for all outputs.
21. T_{HIGH} is measured at 2.0V for 2.5V outputs, 2.4V for 3.3V outputs.

Group Skew and Jitter Limits

Output Group	Pin-Pin Skew Max.	Cycle-Cycle Jitter	Duty Cycle	Nom Vdd	Skew, Jitter Measure Point	Typical Output Impedance
CPU	175 ps	250 ps	45/55	2.5V	1.25V	31Ω
SDRAM	250 ps	250 ps	45/55	3.3V	1.5V	22Ω
APIC	250 ps	500 ps	45/55	2.5V	1.25V	21Ω
48MHz	250 ps	500 ps	45/55	3.3V	1.5V	USB 31Ω Dot 22Ω
3V66	175 ps	500 ps	45/55	3.3V	1.5V	31Ω
PCI	500 ps	500 ps	45/55	3.3V	1.5V	31Ω
REF	N/A	1000 ps	45/55	3.3V	1.5V	21Ω

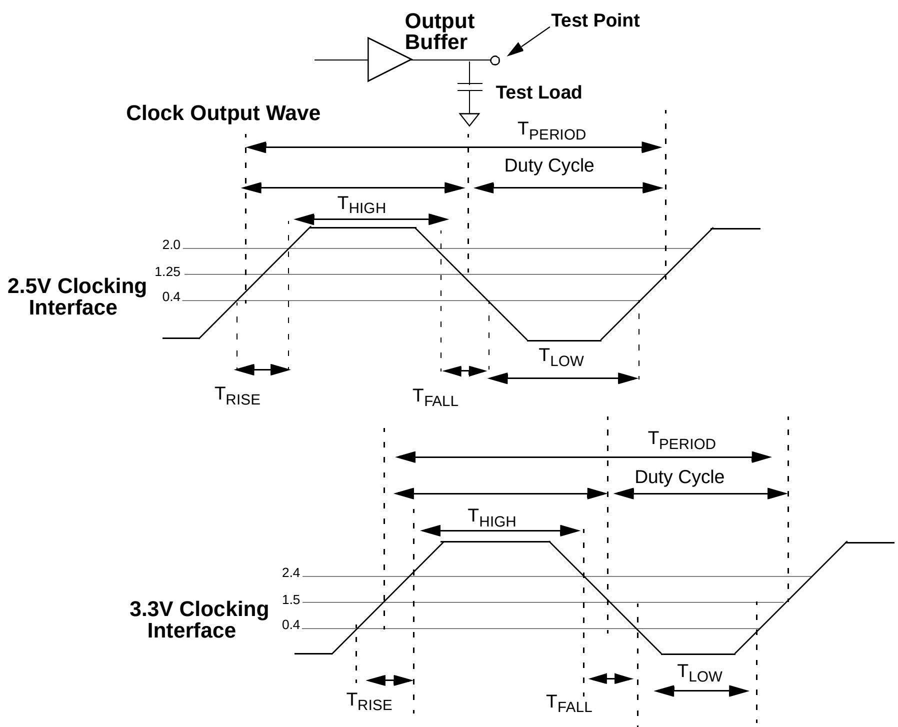


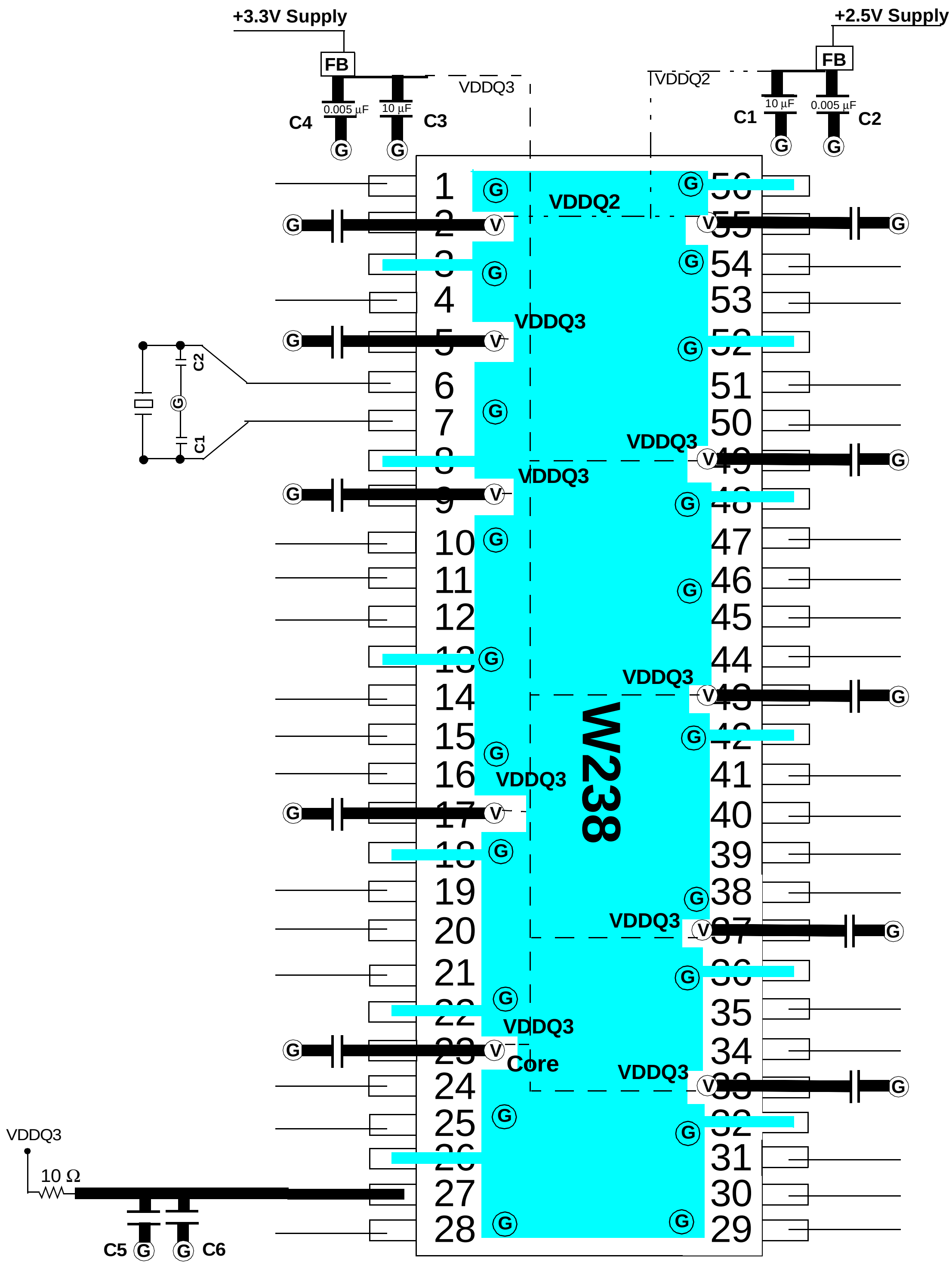
Figure 11. Output Buffer

Ordering Information

Ordering Code	Package Name	Package Type
W238-02	H	56-pin SSOP (300 mils)

Intel is a registered trademark of Intel Corporation

Layout Diagram



FB = Dale ILB1206 - 300 (300Ω @ 100 MHz)

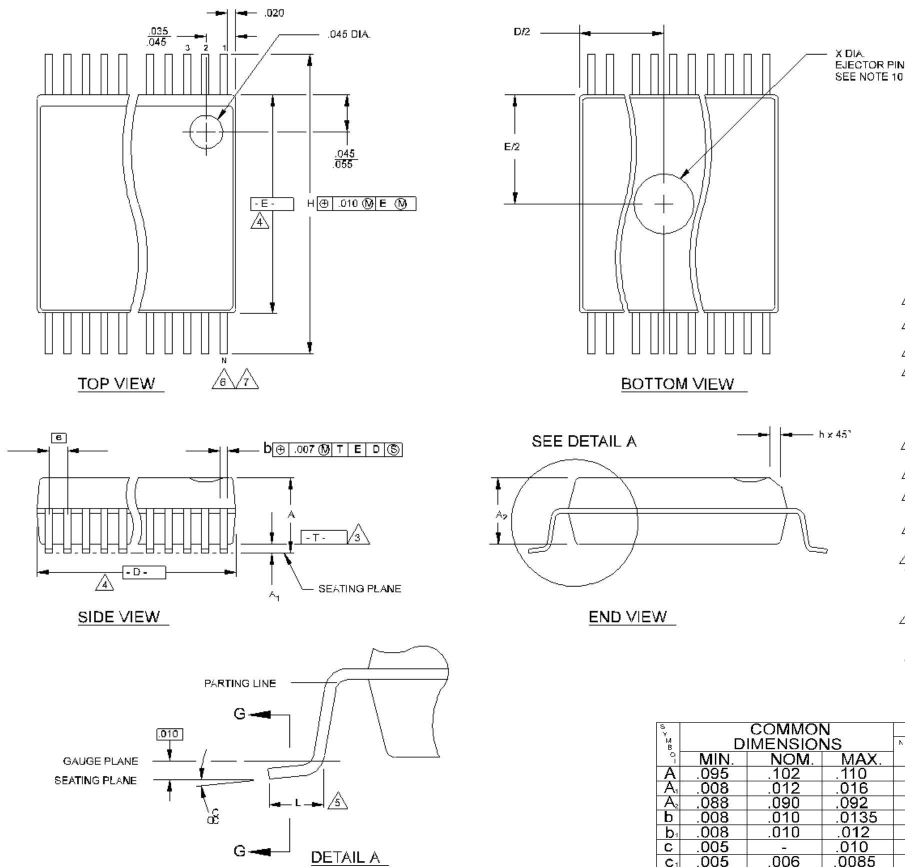
Ceramic Caps C1 & C3 = 10–22 µF C2 & C4 = 0.005 µF C5 = 10 µF C6 = 0.1 µF

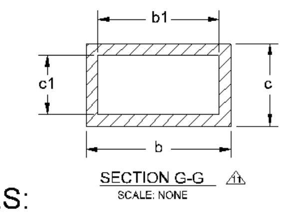
G = VIA to GND plane layer V =VIA to respective supply plane layer

Note: Each supply plane or strip should have a ferrite bead and capacitors

Package Diagram

56-Pin Shrink Small Outline Package (SSOP, 300 mils)





NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. CONTROLLING DIMENSION: INCHES.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 INCHES AND .010 INCHES FROM THE LEAD TIPS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-118, VARIATIONS AA, AB, EXCEPT CHAMFER DIMENSION h. JEDEC SPECIFICATION FOR h IS .015"/.025".

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	.095	.102	.110	
A_1	.008	.012	.016	
A_2	.088	.090	.092	
b	.008	.010	.0135	
b_1	.008	.010	.012	
c	.005	-	.010	
c_1	.005	.006	.0085	
D	SEE VARIATIONS			4
E	.292	.296	.299	
e		.025 BSC		
H	.400	.406	.410	
h	.010	.013	.016	
L	.024	.032	.040	
N	SEE VARIATIONS			6
X	.085	.093	.100	10
α	0°	5°	8°	

NOTE	4			6
VARIATIONS	D MIN.	NOM.	MAX.	N
AA	.620	.625	.630	48
AB	.720	.725	.730	56

THIS TABLE IN INCHES

Summary of nominal dimensions in inches:

Body Width: 0.296
Lead Pitch: 0.025
Body Length: 0.625
Body Height: 0.102

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	2.41	2.59	2.79	
A_1	0.20	0.31	0.41	
A_2	2.24	2.29	2.34	
b	0.203	0.254	0.343	
b_1	0.203	0.254	0.305	
c	0.127	-	0.254	
c_1	0.127	0.152	0.216	
D	SEE VARIATIONS			4
E	7.42	7.52	7.59	
e		0.635 BSC		
H	10.16	10.31	10.41	
h	0.25	0.33	0.41	
L	0.61	0.81	1.02	
N	SEE VARIATIONS			6
X	2.16	2.36	2.54	10
α	0°	5°	8°	

NOTE	4			6
VARIATIONS	D MIN.	NOM.	MAX.	N
AA	15.75	15.88	16.00	48
AB	18.29	18.42	18.54	56

THIS TABLE IN MILLIMETERS

Document Title: W238-02 FTG for Integrated Core Logic w/ 133 MHz FSB Document Number: 38-07103				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107459	08/08/01	IKA	New Data Sheet
*A	122782	12/26/02	RBI	Add power up requirements to AC/DC Electrical Characteristics information.