

# UT54ACS139/UT54ACTS139

## Radiation-Hardened

## Dual 2-Line to 4-Line Decoders/Demultiplexers

### FEATURES

- Incorporates two enable inputs to simplify cascading and/or data reception
- 1.2μ radiation-hardened CMOS
  - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
  - 16-pin DIP
  - 16-lead flatpack

### DESCRIPTION

The UT54ACS139 and the UT54ACTS139 are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times.

The devices consist of two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

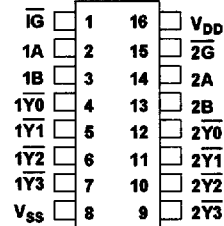
The devices are characterized over full military temperature range of -55°C to +125°C.

### FUNCTION TABLE

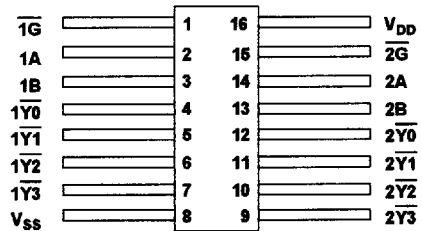
ENABLE INPUTS	SELECT INPUTS		OUTPUT			
			$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

### PINOUTS

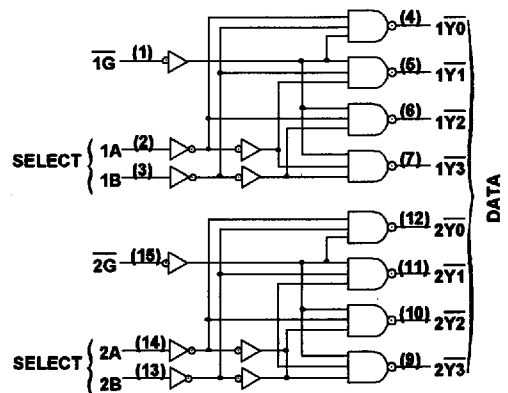
16-Pin DIP  
Top View



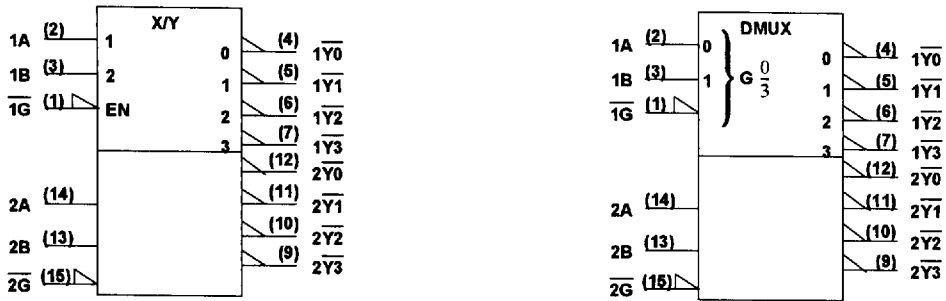
16-Lead Flatpack  
Top View



### LOGIC DIAGRAM



**LOGIC SYMBOL**



**Note:**  
 1. Logic symbols in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**RADIATION HARDNESS SPECIFICATIONS <sup>1</sup>**

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU Threshold <sup>2</sup>	80	MeV-cm <sup>2</sup> /mg
SEL Threshold	120	MeV-cm <sup>2</sup> /mg
Neutron Fluence	1.0E14	n/cm <sup>2</sup>

**Notes:**  
 1. Logic will not latchup during radiation exposure within the limits defined in the table.  
 2. Device storage elements are immune to SEU affects.

**ABSOLUTE MAXIMUM RATINGS**

SYMBOL	PARAMETER	LIMIT	UNITS
V <sub>DD</sub>	Supply voltage	-0.3 to 7.0	V
V <sub>I/O</sub>	Voltage any pin	-.3 to V <sub>DD</sub> +.3	V
T <sub>STG</sub>	Storage Temperature range	-65 to +150	°C
T <sub>J</sub>	Maximum junction temperature	+175	°C
T <sub>LS</sub>	Lead temperature (soldering 5 seconds)	+300	°C
Θ <sub>JC</sub>	Thermal resistance junction to case	20	°C/W
I <sub>I</sub>	DC input current	±10	mA
P <sub>D</sub>	Maximum power dissipation	1	W

**Note:**  
 1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

<b>SYMBOL</b>	<b>PARAMETER</b>	<b>LIMIT</b>	<b>UNITS</b>
$V_{DD}$	Supply voltage	4.5 to 5.5	V
$V_{IN}$	Input voltage any pin	0 to $V_{DD}$	V
$T_C$	Temperature range	-55 to + 125	°C

**DC ELECTRICAL CHARACTERISTICS** <sup>7</sup> $(V_{DD} = 5.0V \pm 10\%; V_{SS} = 0V^6, -55^\circ C < T_C < +125^\circ C)$ 

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
$V_{IL}$	Low-level input voltage <sup>1</sup> ACTS ACS			0.8 .3 $V_{DD}$	V
$V_{IH}$	High-level input voltage <sup>1</sup> ACTS ACS		.5 $V_{DD}$ .7 $V_{DD}$		V
$I_{IN}$	Input leakage current ACTS/ACS	$V_{IN} = V_{DD}$ or $V_{SS}$	-1	1	$\mu A$
$V_{OL}$	Low-level output voltage <sup>3</sup> ACTS ACS	$I_{OL} = 8.0mA$ $I_{OL} = 100\mu A$		0.40 0.25	V
$V_{OH}$	High-level output voltage <sup>3</sup> ACTS ACS	$I_{OH} = -8.0mA$ $I_{OH} = -100\mu A$	.7 $V_{DD}$ $V_{DD} - 0.25$		V
$I_{OL}$	Output current <sup>10</sup> (Sink)	$V_{IN} = V_{DD}$ or $V_{SS}$ $V_{OL} = 0.4V$	8		mA
$I_{OH}$	Output current <sup>10</sup> (Source)	$V_{IN} = V_{DD}$ or $V_{SS}$ $V_{OH} = V_{DD} - 0.4V$	-8		mA
$I_{OS}$	Short-circuit output current <sup>2,4</sup> ACTS/ACS	$V_O = V_{DD}$ and $V_{SS}$	-200	200	mA
$P_{total}$	Power dissipation <sup>2, 8, 9</sup>	$C_L = 50pF$		1.8	mW/ MHz
$I_{DDQ}$	Quiescent Supply Current	$V_{DD} = 5.5V$		10	$\mu A$
$\Delta I_{DDQ}$	Quiescent Supply Current Delta ACTS	For input under test $V_{IN} = V_{DD} - 2.1V$ For all other inputs $V_{IN} = V_{DD}$ or $V_{SS}$ $V_{DD} = 5.5V$		1.6	mA
$C_{IN}$	Input capacitance <sup>5</sup>	$f = 1MHz @ 0V$		15	pF
$C_{OUT}$	Output capacitance <sup>5</sup>	$f = 1MHz @ 0V$		15	pF

## UT54ACS139/UT54ACTS139

### Notes:

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions:  $V_{IH} = V_{IH(min)} + 20\%$ ,  $- 0\%$ ;  $V_{IL} = V_{IL(max)} + 0\%$ ,  $- 50\%$ , as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to  $V_{IH(min)}$  and  $V_{IL(max)}$ .
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density  $\leq 5.0E5$  amps/cm<sup>2</sup>, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3.765 pF/MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and  $V_{SS}$  at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6. Maximum allowable relative shift equals 50mV.
7. All specifications valid for radiation dose  $\leq 1E6$  rads(Si).
8. Power does not include power contribution of any TTL output sink current.
9. Power dissipation specified per switching output.
10. This value is guaranteed based on characterization data, but not tested.

**AC ELECTRICAL CHARACTERISTICS <sup>2</sup>** $(V_{DD} = 5.0V \pm 10\%; V_{SS} = 0V^1, -55^\circ C < T_C < +125^\circ C)$ 

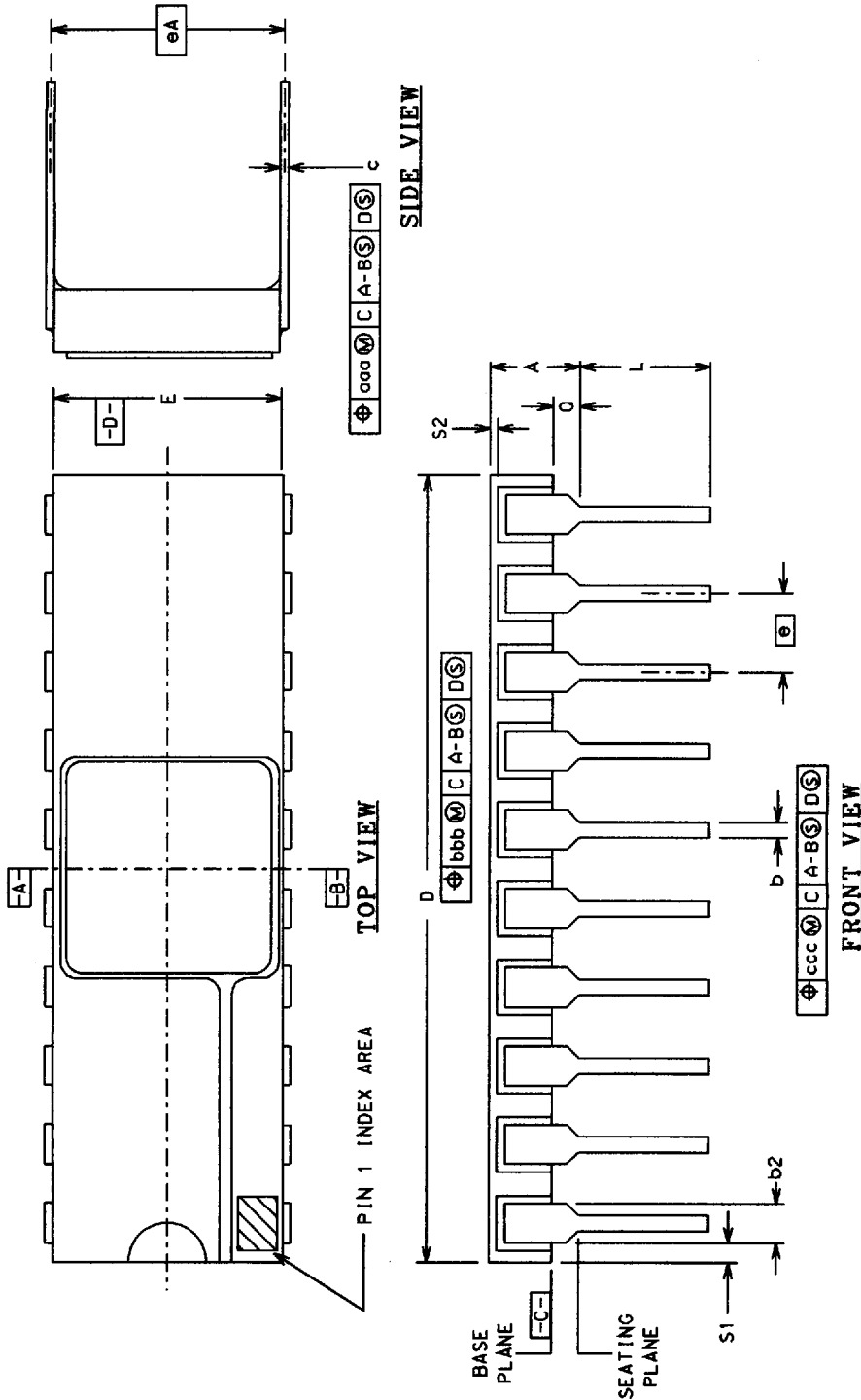
SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
$t_{PHL}$	Select to output $\overline{Y_n}$	2	14	ns
$t_{PLH}$	Select to output $\overline{Y_n}$	2	15	ns
$t_{PHL}$	Enable to output $\overline{Y_n}$	2	14	ns
$t_{PLH}$	Enable to output $\overline{Y_n}$	2	12	ns

**Notes:**

1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose  $\leq 1E6$  rads(Si).

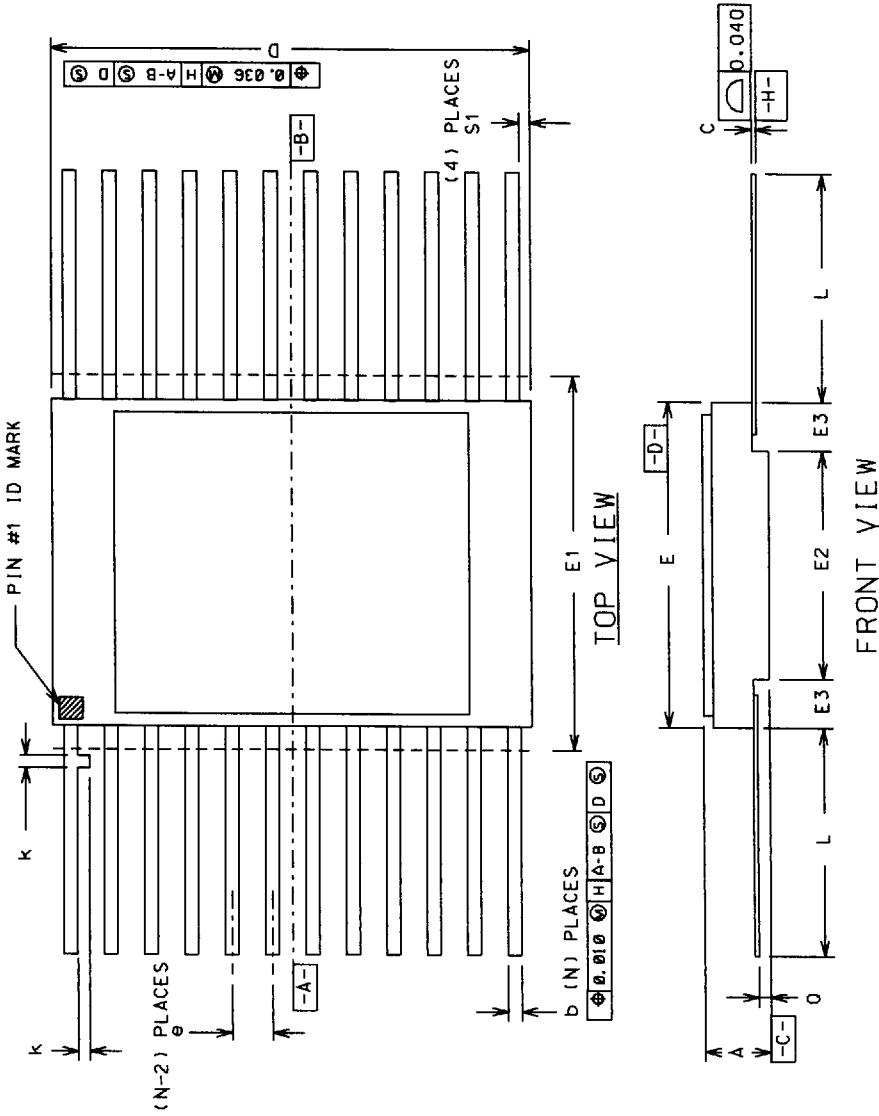
## 2.0 RADHARD MSI PACKAGES

### Side-Brazed Packages



PKG CONFIG	LEAD COUNT	MIL-STD-1835 DWG CONF C	DIMENSION SYMBOLS														
			A	b	b2	c	D	E	e	eA	L	O	S1	S2	bbb	ccc	
-01	14	D-1	0.200	0.026	0.065	0.018	0.785	0.310	0.100	0.300	0.200	0.060	---	---	0.015	0.030	ccc
-02	16	D-2	0.200	0.014	0.045	0.008	---	0.220	BSC	BSC	0.125	0.015	0.005	0.005	0.015	0.030	ccc
-03	20	D-8	0.200	0.026	0.065	0.018	0.840	0.310	0.100	0.300	0.200	0.060	---	---	0.015	0.030	ccc
			0.200	0.014	0.045	0.008	1.060	0.220	BSC	BSC	0.125	0.015	0.005	0.005	0.015	0.030	ccc
			---	0.014	0.045	0.008	---	0.310	BSC	BSC	0.125	0.015	0.005	0.005	0.015	0.030	ccc

# Flatpack Packages



PKG CONF G	LEAD COUNT	MIL-STD 1835 DMG CONF B	DIMENSION SYMBOLS													
			A	b	c	D	E	E1	E2	E3	e	k	L	Q	S1	
-03	14	F-2A	0.115 0.045	0.022 0.015	0.009 0.004	0.390 ---	0.260 0.235	0.290 ---	0.130 ---	0.030 ---	0.050 BSC	0.015 0.008	0.370 0.270	0.045 0.026	---	0.005
-04	16	F-5A	0.115 0.045	0.022 0.015	0.009 0.004	0.440 ---	0.285 0.245	0.315 ---	0.130 ---	0.030 ---	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	---	0.005
-05	20	F-9A	0.115 0.045	0.022 0.015	0.009 0.004	0.540 ---	0.300 0.245	0.330 ---	0.130 ---	0.030 ---	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	---	0.000