



L3211

ADVANCE DATA

VERY LOW VOLTAGE SPEECH CIRCUIT WITH DTMF INTERFACE

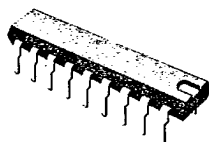
- SPEECH MODE DOWN TO 5mA/1.3V FOR PARALLEL OPERATION
- DTMF MODE DOWN TO 14mA
- A.C. BRIDGE CONFIGURATION ALLOWS ALL IMPEDANCES TO BE CONTROLLED CLOSELY
- DRIVES RECEIVERS OF 150Ω IMPEDANCE FOR REDUCED COST
- ON CHIP DTMF INTERFACE

The L3211 is a monolithic integrated circuit in 18 pin plastic DIP package suitable to replace the hybrid circuit in the telephone set. It works with magnetic capsules in receiving and with electret microphone in sending. With its very low voltage operation the L3211 is particularly suitable to work in parallel with conventional telephone sets.

In addition to speech operation, the L3211 acts as interface for the DTMF for both feeding and signaling functions.

The L3211 basic functions are the following:

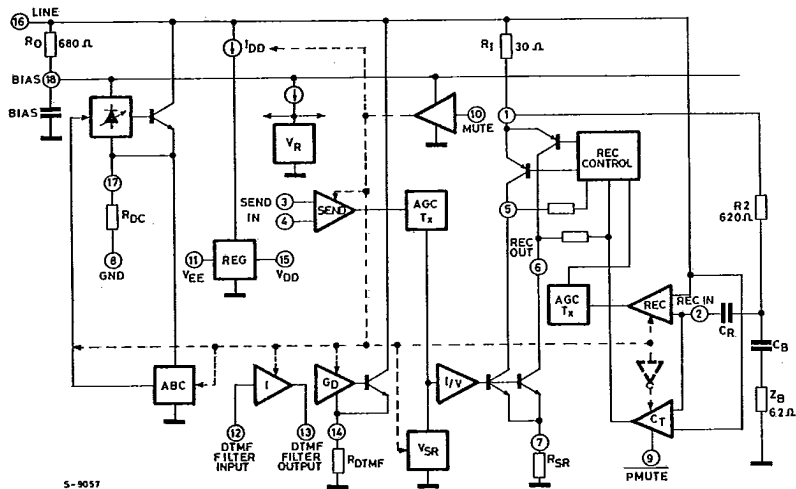
- To present the proper DC path for the line current (particular care has been paid to have very low voltage drop at low line current levels).
- To handle the voice signal, performing the 2/4 wires interface and changing the gain on both sending and receiving amplifiers to compensate for line attenuation by sensing the line current.
- To act as linear interface for the DTMF, supplying a stabilized voltage to the digital chip and delivering to the line the MF tones generated during the signaling.
- To feed with a constant voltage the electret microphone.



DIP-18 Plastic
(0.4)

ORDERING NUMBER: L3211

BLOCK DIAGRAM



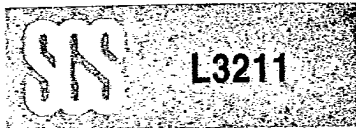
This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS

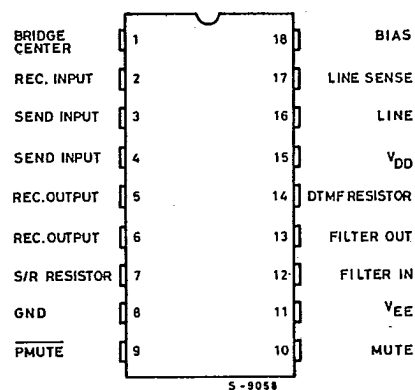
V_L	Line Voltage (3ms pulse duration)	20	V
I_L	Line Current	150	mA
P_{tot}	Total Power dissipation at $T_{amb} = 70^\circ\text{C}$	1	W
T_{op}	Operating temperature	-20 to +55	$^\circ\text{C}$
T_{stg}, T_J	Storage and Junction temperature	-60 to +150	$^\circ\text{C}$

THERMAL DATA

$R_{th J-amb}$	Thermal resistance junction-ambient	max	80	$^\circ\text{C/W}$
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CONNECTION DIAGRAM

(Top view)

Electret Bias (V_{EE})

The electret is biased through a voltage generator at Pin 11.

DC Regulator

This stage provides the path for the DC line current (DC characteristics) through the external resistor R_{DC} to pin 17.

AGC ($AGC T_X$, $AGC R_X$)

The Automatic Gain Control is internally fixed for both T_X , and R_X sections. The AGC function is built with low distortion stages.

 V_{DD}

A regulated voltage is available at Pin 15 for the bias of the DTMF generator. This stage has the following characteristics:

- When the line voltage drops lower than V_{DD} , the V_{DD} output follows the line voltage.
- The load is fed through a saturated NPN transistor. During pulse dialing when the I_C is disconnected from the line, the capacitor across the V_{DD} output is discharged only by the base-emitter leakage of the NPN transistor. This allows this capacitor to be used for "Keep Alive Memory" in pulse dialing application.



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BLOCK DESCRIPTION (continued)**Sending/Receiving Stages**

A differential input stage is available in sending. The sending/receiving gains are internally fixed. Nevertheless, sending gain can be adjusted by varying the electret bias and receiving gain can be adjusted by rearranging the external balancing network R_1 , R_2 , Z_B .

Confidence Level

A confidence level gain stage is built in parallel with the input receiving stage. During DTMF mode the C.L. gain stage is turned on and the input receiving stage is turned off. This permits a fixed amount of DTMF signal when receiving.

DTMF Amplifier and Filter

The DTMF transconductance output amplifier is available between pins 14 and 16. An external resistor at Pin 14 controls the amount of DTMF gain. A buffer stage for filtering an incoming DTMF gain. A buffer stage for filtering an incoming DTMF tone is provided between pin 12 and 13.

Mute

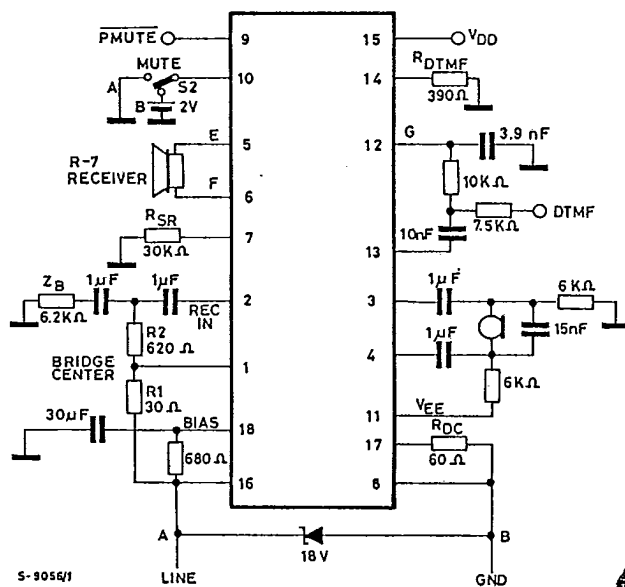
The functions performed by the mute (active high, pin 10) are:

- Mute of the sending path
- Reduction of the sending/receiving consumption.
- Increase of the source current at the regulated output V_{DD} .
- Increase of the line voltage.
- Switching of the ABC into the high current mode.
- Mute of the first stage in receiving.
- Turn on of the confidence level stage.
- Bias of the DTMF amplifier stage and filter.

Pmute

When \overline{Pmute} (Pin 9) is low the confidence level signal in receiving is muted.

Fig. 1 - Application and test circuit



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ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $f = 200$ to 3400Hz , S2 in position (a) on the test circuit, unless otherwise specified).

Parameter	Test Conditions	Min	Typ	Max	Unit	Fig.
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SPEECH OPERATION for $I_L = 20\text{mA}$ to 125mA

V_L	Line Voltage	$I_L = 20\text{mA}$ $I_L = 125\text{mA}$			5.1 12	V V	
G_S	Sending Gain	$f = 1\text{KHz}$ $V_{MI} = 3\text{mV}$ $I_L = 42\text{mA}$ $I_L = 96\text{mA}$	39 35		41 37	dB dB	2 2
	Sending Distortion	$f = 1\text{KHz}$ $I_L = 20\text{mA}$ $V_{SO} = 700\text{mV}$			2	%	2
	Sending Noise	$V_{MI} = 0\text{V}$		-70		dBmp	2
	Micro Input Impedance	$V_{MI} = 3\text{V}$	40			$\text{K}\Omega$	
G_R	Receiving gain	$V_{RI} = 0.3\text{V}$ $f = 1\text{KHz}$ $I_L = 42\text{mA}$ $I_L = 96\text{mA}$	-11 -15		-9 -13	dB dB	3 3
	Receiving Distortion	$f = 1\text{KHz}$ $I_L = 20\text{mA}$ $V_{RO} = 440\text{mV}$			2	%	3
	Receiving Noise	$V_{RI} = 0$		100		μV	3
	Receiving out impedance	$V_{RO} = 50\text{mV}$		30		Ω	
	Sidetone	$f = 1\text{KHz}$		36		dB	2
Z_{ML}	Line matching impedance	$V_{RI} = 0.3\text{V}$ $f = 1\text{KHz}$		600		Ω	3
	Return Loss	$V_{RI} = 0.3\text{V}$ $f = 1\text{KHz}$	-14			dB	3
V_{EE}	Electret Bias		2.4			V	
I_{EE}	Electret Supply Current		0.5			mA	
V_{DD}	DTMF Supply Voltage		2.4			V	
I_{DD}	DTMF Stand-by Supply Current		0.5			mA	

SPEECH OPERATION for $I_L = 5\text{mA}$ to 20mA

V_L	Line Voltage	$I_L = 5\text{mA}$			1.3	V	
V_{SO}	Sending dyn. input voltage	$I_L = 5\text{mA}$		100		mV_{rms}	
I_{RO}	Receiving dyn. output current	$I_L = 5\text{mA}$		0.8		mA	
V_{EE}	Electret bias	$I_L = 5\text{mA}$		0.7		V	

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ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	Min	Typ	Max	Unit	Fig.
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DTMF INTERFACE AND OPERATION $I_L = 20\text{mA}$ to 125mA

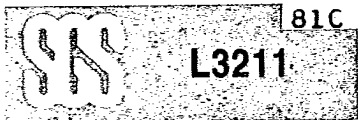
V_{DD}	DTMF Supply Voltage	S2 in (b)	2.4			V	
I_{DD}	DTMF Supply Current	S2 in (b)	2.5			mA	
V_{PI}	Sinusoidal Input pair level (Pin 12)	$V_{DD} = 2.5\text{V}$		3.4		V_{PP}	5
DTMF	Amplifier Gain	$f_{MF\text{ in}} = 1\text{KHz}$ $V_{MF\text{ in}} = 80\text{mV}$	-3.3	-2.3	-1.3	dB	4
DTMF	Transient Voltage				$V_L + 5$	V	
R_I	Input impedance	$V_{MF\text{ in}} = 80\text{mV}$	60			$K\Omega$	
	Signal Tone Dist.	$I_L = 14\text{mA}$		2		%	
	Starting Delay Time				5	ms	
V_{IL}	Mute Input Low				1.0	V	
V_{IH}	Mute Input High		2.0			V	
V_{CL}	Conf. level gain $(20 \log_{10} \frac{V_{RO}}{V_{SO}})$		-24		-30	dB	
	Sending Gain Mute	$V_{MI} = 3\text{mV}$ S2 in (b)		-60		dB	2
$I_{LEAK\ V_{DD}}$	Leakage	$V_{DD} = 2.5\text{V}$		2		nA	

DTMF INTERFACE AND OPERATION 14mA to 20mA

I_b	Boost Current (Pin 12)			100		μA	
V_{SO}	Sinusoidal Output Levels	High Low		-9 -11		dBm dBm	

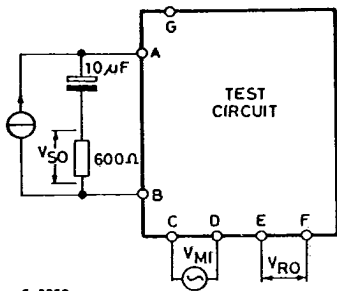
PULSE DIALING OPERATION

I_{PL}	Input Low Current $\overline{P_{mute}}$				50	μA	
I_{LEAK}	Input High Current $\overline{P_{mute}}$				-10	μA	
	Confidence Level	P_{mute} Low		-40		dB	3



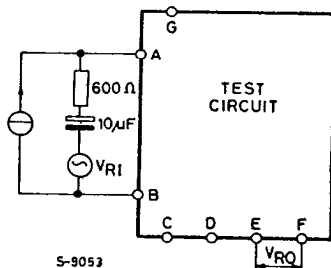
TEST CIRCUITS

Fig. 2



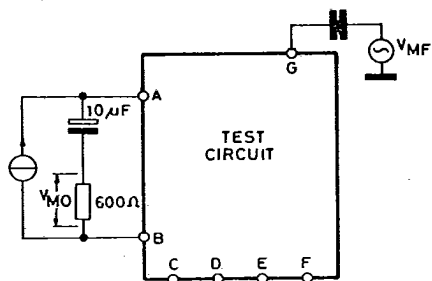
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Fig. 3



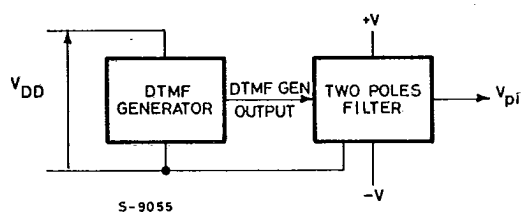
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Fig. 4



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Fig. 5



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