LogiCORE PCI32 Interface v3.0

DS 206 (v1.2) July 19, 2002 **Data Sheet, v3.0.100**

Introduction

With the Xilinx LogiCORE PCI Interface, a designer can build a customized, fully PCI 2.3-compliant core with the highest possible sustained performance, 528 Mbytes/sec.

Features

- Fully PCI 2.3-compliant core, 64/32-bit, 66/33 MHz interface
- Customizable, programmable, single-chip solution
- Predefined implementation for predictable timing
- Incorporates Xilinx Smart-IP Technology
- 3.3 V operation at 0-66 MHz
- 5.0 V operation at 0-33 MHz
- Fully verified design tested with Xilinx proprietary testbench and hardware
- Available for configuration and download on the web:
  - Web-based Configuration and Download Tool
  - Web-based User Constraint File Generator Tool
- CardBus compliant
- Supported initiator functions:
  - Configuration Read, Configuration Write
  - Memory Read, Memory Write, MRM, MRL
  - Interrupt Acknowledge, Special Cycles
  - I/O Read, I/O Write
- Supported target functions:
  - Type 0 Configuration Space Header
  - Up to 3 Base Address Registers (MEM or I/O with adjustable block size from 16 bytes to 2 Gbytes)
  - Medium Decode Speed
  - Parity Generation, Parity Error Detection
  - Configuration Read, Configuration Write
  - Memory Read, Memory Write, MRM, MRL
  - Interrupt Acknowledge
  - I/O Read, I/O Write
  - Target Abort, Target Retry, Target Disconnect

LogiCORE Facts

PCI64 Resource Utilization[1]	
Slice Four Input LUTs	724
Slice Flip Flops	732
IOB Flip Flops	176
IOBs	89
TBUFs	352
GCLKs	1[2]
PCI32 Resource Utilization[1]	
Slice Four Input LUTs	553
Slice Flip Flops	566
IOB Flip Flops	97
IOBs	50
TBUFs	288
GCLKs	1[2]
Provided with Core	
Documentation	*PCI Design Guide* *PCI Implementation Guide*
Design File Formats	Verilog/VHDL Simulation Model NGO Netlist
Constraint Files	User Constraint Files (UCF) Guide Files (NCD)
Example Design	Verilog/VHDL Example Design
Design Tool Requirements	
Xilinx Tools	v4.2i, Service Pack 3
Tested Entry and Verification Tools[3]	Synplicity Synplify Synopsys FPGA Express Exemplar Leonardo Spectrum Xilinx XST[4] Cadence Verilog XL Model Technology ModelSim

1. The resource utilization depends on configuration of the interface and the user design. Unused resources are trimmed by the Xilinx technology mapper. The utilization figures reported in this table are representative of a maximum configuration.
2. Designs running at 66 MHz in devices other than Virtex-II require one GCLKIOB and two GCLKs.
3. See the implementation guide or product release notes for current supported versions.
4. XST is command line option only. See Implementation Guide for details.

LogiCORE Facts (Cont)		
Supported Devices		
PCI32/66	Virtex V200FG256-6C	3.3v only
	Virtex-E V200EFG256-6C	3.3v only
	Virtex-E V400EFG676-6C	3.3v only
PCI32/33	Virtex V300BG432-5C	3.3v, 5.0v
	Virtex V1000FG680-5C	3.3v, 5.0v
	Virtex-E V100EBG352-6C	3.3v only
	Virtex-E V300EBG432-6C	3.3v only
	Virtex-E V1000EFG680-6C	3.3v only
	Virtex-II 2V1000FG456-4C/I/M	3.3v only
	Virtex-II Pro 2VP7FF672-6C	3.3v only
	Spartan-II 2S30PQ208-5C	3.3v, 5.0v
	Spartan-II 2S50PQ208-5C	3.3v, 5.0v
	Spartan-II 2S100PQ208-5C	3.3v, 5.0v
	Spartan-II 2S150PQ208-5C	3.3v, 5.0v
	Spartan-II 2S200PQ208-5C	3.3v, 5.0v
	Spartan-IIE 2S50EPQ208-6C	3.3v only
	Spartan-IIE 2S100EPQ208-6C	3.3v only
	Spartan-IIE 2S150EPQ208-6C	3.3v only
	Spartan-IIE 2S200EPQ208-6C	3.3v only
	Spartan-IIE 2S300EPQ208-6C	3.3v only
Xilinx provides technical support for this LogiCORE product when used as described in the Design Guide and the Implementation Guide. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices not listed, or if customized beyond that allowed in the product documentation.		

Note: Universal card implementations require two bitstreams.
Note: Virtex-E and Spartan-IIE recommended for CardBus.
Note: Commercial devices; 0 C < T_j < 85 C.
Note: For additional Part/Package combinations, see the UCF Generator in the PCI Lounge.
Note: 2V1000 is supported over Military Temp. range.

Applications

- Embedded applications in networking, industrial, and telecommunication systems
- PCI add-in boards such as frame buffers, network adapters, and data acquisition boards
- Hot swap CompactPCI boards
- CardBus compliant
- Any applications that need a PCI interface

General Description

The LogiCORE PCI Interface is a preimplemented and fully tested module for Xilinx FPGAs. The pinout for each device and the relative placement of the internal logic are predefined. Critical paths are controlled by constraint and guide files to ensure predictable timing. This significantly reduces the engineering time required to implement the PCI portion of your design. Resources can instead be focused on your unique user application logic in the FPGA and on the system-level design. As a result, LogiCORE PCI products minimize your product development time.

The core meets the setup, hold, and clock-to-timing requirements as specified in the PCI-X specification. The interface is verified through extensive simulation.

Other features that enable efficient implementation of a PCI system include:

- Block SelectRAM™ memory. Blocks of on-chip ultra-fast RAM with synchronous write and dual-port RAM capabilities. Used in PCI designs to implement FIFOs.
- SelectRAM memory. Distributed on-chip ultra-fast RAM with synchronous write option and dual-port RAM capabilities. Used in PCI designs to implement FIFOs.
- Internal three-state bus capability for data multiplexing.

The interface is carefully optimized for best possible performance and utilization in Xilinx FPGA devices.

Smart-IP Technology

Drawing on the architectural advantages of Xilinx FPGAs, Xilinx Smart-IP technology ensures the highest performance, predictability, repeatability, and flexibility in PCI designs. The Smart-IP technology is incorporated in every LogiCORE PCI interface.

Xilinx Smart-IP technology leverages the Xilinx architectural advantages, such as look-up tables and segmented routing, as well as floorplanning information, such as logic mapping and location constraints. This technology provides the best physical layout, predictability, and performance. In addition, these features allow for significantly reduced compile times over competing architectures.

To guarantee the critical setup, hold, minimum clock-to-out, and maximum clock-to-out timing, the PCI interface is delivered with Smart-IP constraint files that are unique for a device and package combination. These constraint files guide the implementation tools so that the critical paths always are within specification.

Xilinx provides Smart-IP constraint files for many device and package combinations. Constraint files for unsupported device and package combinations may be generated using the web-based constraint file generator.

Functional Description

The LogiCORE PCI Interface is partitioned into five major blocks and a user application as shown in Figure 1.

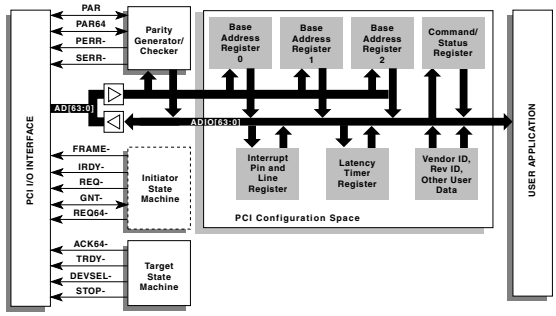

Figure 1: **LogiCORE PCI Interface Block Diagram**

PCI I/O Interface Block

The I/O interface block handles the physical connection to the PCI bus including all signaling, input and output synchronization, output three-state controls, and all request-grant handshaking for bus mastering.

User Application

The LogiCORE PCI Interface provides a simple, general-purpose interface for a wide range of applications.

PCI Configuration Space

This block provides the first 64 bytes of Type 0, version 2.3 Configuration Space Header, as shown in Table 1, to support software-driven “Plug-and-Play” initialization and configuration. This includes information for Command, Status, and three Base Address Registers (BARs).

The capability for extending configuration space has been built into the user application interface. This capability, including the ability to implement a capabilities pointer in configuration space, allows the user to implement functions such as power management and message signaled interrupts in the user application.

Parity Generator/Checker

This block generates and checks even parity across the AD bus, the CBE# lines, and the parity signals. It also reports data parity errors via PERR# and address parity errors via SERR#.

Initiator State Machine

This block controls the PCI interface initiator functions. The states implemented are a subset of those defined in Appendix B of the *PCI Local Bus Specification*. The initiator control logic uses one-hot encoding for maximum performance.

Target State Machine

This block controls the PCI interface target functions. The states implemented are a subset of those defined in Appendix B of the *PCI Local Bus Specification*. The target control logic uses one-hot encoding for maximum performance.

Table 1: **PCI Configuration Space Header**

31	16	15	0	
Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Rev ID	08h
BIST	Header Type	Latency Timer	*Cache Line Size*	0Ch
Base Address Register 0 (BAR0)				10h
Base Address Register 1 (BAR1)				14h
Base Address Register 2 (BAR2)				18h
Base Address Register 3 (BAR3)				1Ch
Base Address Register 4 (BAR5)				20h
Base Address Register 5 (BAR5)				24h
Cardbus CIS Pointer				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved			CapPtr	34h
Reserved				38h
Max Lat	Min Gnt	Int Pin	Int Line	3Ch
Reserved				40h-FFh

Note:
Shaded areas are not implemented and return zero.

Interface Configuration

The LogiCORE PCI Interface can easily be configured to fit unique system requirements by using the Xilinx Web-based Configuration and Download tool or by changing the HDL configuration file. The following customization options, among many others, are supported by the interface and are described in the product design guide.

- Base Address Registers (number, size, and type)
- Configuration Space Header ROM

Burst Transfer

The PCI bus derives its performance from its ability to support burst transfers. The performance of any PCI application depends largely on the size of the burst transfer. Buffers to support PCI burst transfer can efficiently be implemented using on-chip RAM resources.

Supported PCI Commands

Table 2 illustrates the PCI bus commands supported by the LogiCORE PCI Interface.

Bandwidth

The LogiCORE PCI Interface supports fully compliant zero wait-state burst operations for both sourcing and receiving data. This interface supports a sustained bandwidth of up to 528 MBytes/sec. The design can be configured to take advantage of the ability of the LogiCORE PCI Interface to do very long bursts.

The flexible user application interface, combined with support for many different PCI features, gives users a solution that lends itself to use in many high-performance applications. The user is not locked into one DMA engine; hence, an optimized design that fits a specific application can be designed.

Recommended Design Experience

The LogiCORE PCI Interface is preimplemented, allowing engineering focus on the unique user application functions of a PCI design. Regardless, PCI is a high-performance design that is challenging to implement in any technology. Therefore, previous experience with building high-performance, pipelined FPGA designs using Xilinx implementation software, constraint files, and guide files is recommended. The challenge to implement a complete PCI design including user application functions varies depending on configuration and functionality of your application. Contact your local Xilinx representative for a closer review and estimation for your specific requirements.

Timing Specifications

The maximum speed at which your user design is capable of running can be affected by the size and quality of the design. The following tables show the key timing parameters for the LogiCORE PCI Interface.

Table 3 lists the Timing Parameters in the 66MHz Implementations and Table 4 lists Timing Parameters in the 33MHz Implementations.

Table 2: **PCI Bus Commands**

CBE [3:0]	Command	PCI Initiator	PCI Target
0000	Interrupt Acknowledge	Yes	Yes
0001	Special Cycle	Yes	Ignore
0010	I/O Read	Yes	Yes
0011	I/O Write	Yes	Yes
0100	Reserved	Ignore	Ignore
0101	Reserved	Ignore	Ignore
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved	Ignore	Ignore
1001	Reserved	Ignore	Ignore
1010	Configuration Read	Yes	Yes
1011	Configuration Write	Yes	Yes
1100	Memory Read Multiple	Yes	Yes
1101	Dual Address Cycle	No	Ignore
1110	Memory Read Line	Yes	Yes
1111	Memory Write Invalidate	No	Yes

Table 3: **Timing Parameters, 66MHz Implementations**

Symbol	Parameter	Min	Max
T_{cyc}	CLK Cycle Time	15[1]	30
T_{high}	CLK High Time	6	-
T_{low}	CLK Low Time	6	-
T_{val}	CLK to Signal Valid Delay (bussed signals)	2[2]	6[2]
T_{val}	CLK to Signal Valid Delay (point to point signals)	2[2]	6[2]
T_{on}	Float to Active Delay	2[2]	-
T_{off}	Active to Float Delay	-	14[1]
T_{su}	Input Setup Time to CLK (bussed signals)	3[2,3]	-
T_{su}	Input Setup Time to CLK (point to point signals)	5[2,3]	-
T_{h}	Input Hold Time from CLK	0[2,3]	-
T_{rstoff}	Reset Active to Output Float	-	40

Notes:
1. Controlled by timespec constraints, included in product.
2. Controlled by SelectIO configured for PCI66_3.
3. Controlled by guide file, included in product.

Table 4: **Timing Parameters, 33MHz Implementations**

Symbol	Parameter	Min	Max
T_{cyc}	CLK Cycle Time	30[1]	-
T_{high}	CLK High Time	11	-
T_{low}	CLK Low Time	11	-
T_{val}	CLK to Signal Valid Delay (bussed signals)	2[2]	11[2]
T_{val}	CLK to Signal Valid Delay (point to point signals)	2[2]	11[2]
T_{on}	Float to Active Delay	2[2]	-
T_{off}	Active to Float Delay	-	28[1]
T_{su}	Input Setup Time to CLK (bussed signals)	7[2]	-
T_{su}	Input Setup Time to CLK (point to point signals)	10[2]	-
T_{h}	Input Hold Time from CLK	0[2]	-
T_{rstoff}	Reset Active to Output Float	-	40

Notes:
1. Controlled by timespec constraints, included in product.
2. Controlled by SelectIO configured for PCI33_3 or PCI33_5.

Ordering Information

This core may be downloaded from the Xilinx IP Center for use with the Xilinx CORE Generator System v4.1 and later. The Xilinx CORE Generator System tool is bundled with all Alliance and Foundation Series Software packages, at no additional charge.

Part Numbers

DO-DI-PCI32-IP

-Access to the V3.0 PCI32 33 MHz Spartan and 66 MHz Virtex Families

DX-DI-PCI32-SL

-Upgrade from PCI32 33 MHz Spartan only to V3.0 PCI32 33 MHz Spartan and 66 MHz Virtex Families

DO-DI-PCI32-SP

-Access to the V3.0 PCI32 Spartan Family

To order the Xilinx PCI Core, please visit the Xilinx Silicon Xpresso Cafe or contact your local Xilinx sales representative.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/27/02	1.0	New template