CYPRESS SEMICONDUCTOR

CYM1641

256K x 16 Static RAM Module

Features

- **High-density 4-megabit SRAM module**
- **High-speed CMOS SRAMs**
  — **Access time of 25 ns**
- **Customer configurable**
  — **x4, x8, x16**
- **Low active power**
  — **10W (max.)**
- **Hermetic SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  — **Max. height of .300 in.**
- **Small PCB footprint**
  — **2.2 sq. in.**

Functional Description

The CYM1641 is a high-performance 4-megabit static RAM module organized as 256K words by 16 bits. This module is constructed from sixteen 256K x 1 SRAMs in leadless chip carriers mounted on a ceramic substrate with pins. Four separate $\overline{CS}$ pins are used to control each 4-bit nibble of the 16-bit word. This feature permits the user to configure this module as either 1M x 4, 512K x 8 or 256K x 16 organization through external decoding and appropriate pairing of the outputs.

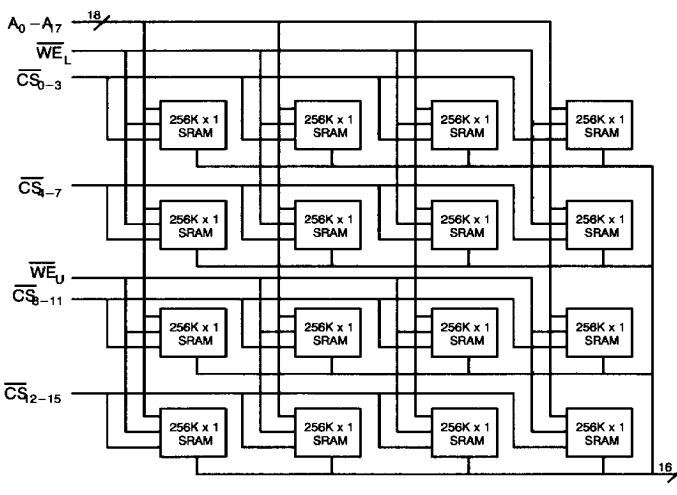
Writing to the device is accomplished when the chip select ($\overline{CS}_{XX}$) and write enable ($\overline{WE}_{U,L}$) inputs are both LOW. Data on the data lines (D_X) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking the chip select ($\overline{CS}_{XX}$) LOW, while write enable ($\overline{WE}_{U,L}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data lines (D_X).

The data output is in the high-impedance state when chip enable ($\overline{CS}_{XX}$) is HIGH or write enable ($\overline{WE}_{U,L}$) is LOW.

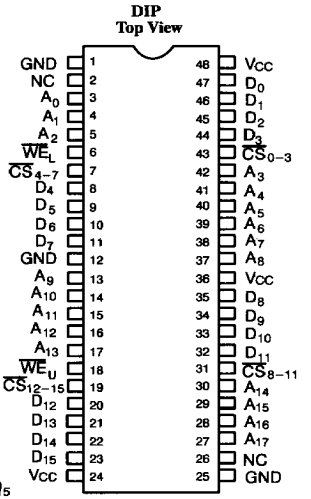
Power is consumed in each 4-bit nibble only when the appropriate $\overline{CS}$ is enabled, thus reducing power in the x4 or x8 mode.

Logic Block Diagram



1641–1

Pin Configuration



1641–2

Selection Guide

		1641-25	1641-30	1641-35	1641-45	1641-55
Maximum Access Time (ns)		25	30	35	45	55
Maximum Operating Current (mA)	Commercial	1800	1800	1800	1800	1800
	Military			1800	1800	1800
Maximum Standby Current (mA)	Commercial	560	560	560	560	560
	Military			560	560	560

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to + 7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			CYM1641 Min.	CYM1641 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA			2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 12.0 mA	Com'l		0.4	V
			I_{OL} = 8.0 mA	Mil		0.4	
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	V
V_{IL}	Input LOW Voltage				− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			− 80	+80	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			− 10	+10	µA
I_{CCx16}	V_{CC} Operating Supply Current by 16 Mode	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}_{XX}$ < V_{IL}				1800	mA
I_{CCx8}	V_{CC} Operating Supply Current by 8 Mode	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}_{XX}$ ≤ V_{IL}				950	mA
I_{CCx4}	V_{CC} Operating Supply Current by 4 Mode	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}_{XX}$ ≤ V_{IL}				720	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[2]	Max. V_{CC}, $\overline{CS}_{XX}$ ≥ V_{IH}, Min. Duty Cycle = 100%				560	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[2]	Mas. V_{CC}, $\overline{CS}_{XX}$ ≥ V_{CC} − 0.2V V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V				320	mA

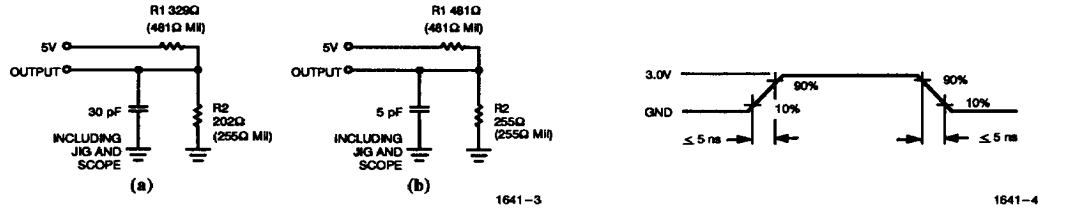
Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{INA}	Input Capacitance (A_0 − A_{17}, $\overline{CS}$, $\overline{WE}$)	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	150	pF
C_{INB}	Input Capacitance (D_0 − D_{15})		30	pF
C_{OUT}	Output Capacitance		30	pF

Notes:

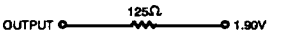
1. T_A is the "instant on" case temperature.
2. A pull-up resistor to V_{CC} on the CS input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

Military



Commercial

Switching Characteristics Over the Operating Range[4]

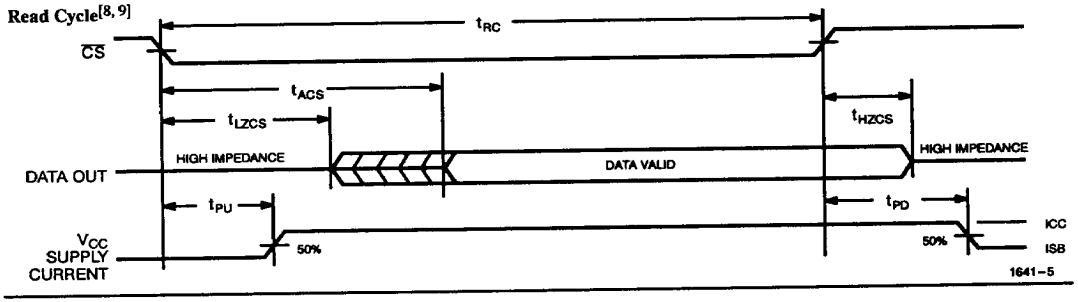
Parameters	Description	1641-25		1641-30		1641-35		1641-45		1641-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	25		30		35		45		55		ns
t_{AA}	Address to Data Valid		25		30		35		45		55	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		30		35		45		55	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	3		3		3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		15		20		20		25		25	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power Down		25		30		35		45		55	ns
WRITE CYCLE[7]												
t_{WC}	Write Cycle Time	25		30		35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		40		40		ns
t_{AW}	Address Set-Up to Write End	20		25		30		40		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		25		30		30		ns
t_{SD}	Data Set-Up to Write End	15		17		17		20		25		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[5]	3		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]	0	20	0	20	0	25	0	25	0	25	ns

Notes:

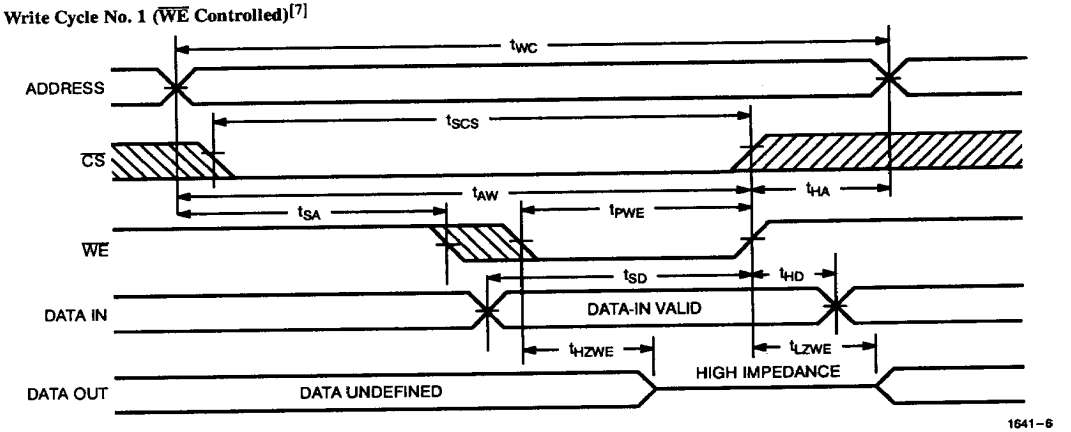
4. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.
6. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

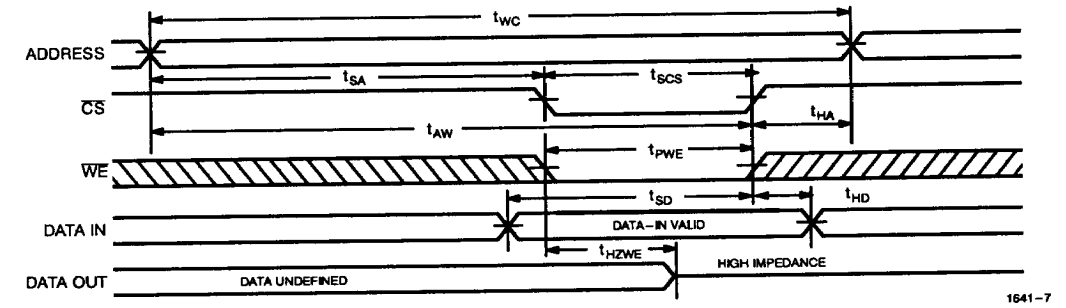
Read Cycle[8, 9]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[7]



Write Cycle No. 2 ($\overline{CS}$ Controlled)[7, 10]



Notes:
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS}$ = V_{IL}.
10. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}_{XX}$	$\overline{WE}_n$	Input/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CYM1641HD-25C	HD05	Commercial
30	CYM1641HD-30C	HD05	Commercial
35	CYM1641HD-35C	HD05	Commercial
	CYM1641HD-35MB	HD05	Military
45	CYM1641HD-45C	HD05	Commercial
	CYM1641HD-45MB	HD05	Military
55	CYM1641HD-55C	HD05	Commercial
	CYM1641HD-55MB	HD05	Military

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