REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26							
REV STATUS OF SHEETS				REV															
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
92-08-03

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, HCMOS, FLOATING POINT COPROCESSOR, MONOLITHIC SILICON

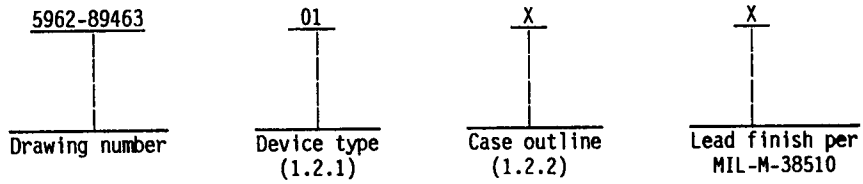
SIZE	CAGE CODE	5962-89463
A	67268	

SHEET 1

1 SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	68882-16	HCMOS floating point coprocessor
02	68882-20	HCMOS floating point coprocessor
03	68882-25	HCMOS floating point coprocessor
04	68882-33	HCMOS floating point coprocessor

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA2-PN	68	Pin grid array package
Y	See figure 1	68	Leaded chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.3 V dc to +7.0 V dc
Storage temperature range (T_{STG})	-65°C to +150°C
Case operating temperature range (T_C)	-55°C to +125°C
Maximum power dissipation (P_D)	0.75 W
Lead temperature (soldering 5 seconds)	270 °C
Junction temperature (T_J)	150 °C
Thermal resistance, junction to case (θ_{JC}):	
Case X	See MIL-STD-1835
Case Y	10°C/W

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage (logic inputs)(V_{IH})	2.0 V dc to V_{CC}
Low level input voltage (logic inputs)(V_{IL})	GND -0.3 V to 0.8 V
Minimum high level output voltage (V_{OH})	2.4 V dc
Maximum low level output Voltage (V_{OL})	0.5 V dc
Frequency of operation:	
Device type 01	12.5 to 16.67 MHz
Device type 02	12.5 to 20.0 MHz
Device type 03	12.5 to 25 MHz
Device type 04	16.67 to 33.33 MHz

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input high voltage	V_{IH}		1, 2, 3	All	2.0	V_{CC}	V
Input low voltage	V_{IL}				-0.3	0.8	
Input leakage current CLK, RESET, R/W, A0-A4, CS, DS, AS, SIZE	I_{IN}	V_{CC} = 5.5 V			-	10	µA
High-impedance(off-state) DSACK0, DSACK1, D0 - D31	I_{TSI}	V_{IN} = 2.4 V / 0.4 V			-	20	
Supply current 2/	I_{CC}	V_{CC} = 5.5 V			-	150	mA
Output low current 3/ (V_{OL} = GND) SENSE	I_{OL}				-	500	µA
High-level output voltage DSACK0, DSACK1, D0 - D31	V_{OH}	I_{OH} = -400 µA			2.4	-	V
Low-level output voltage DSACK0, DSACK1, D0 - D31	V_{OL}	I_{OL} = 5.3 mA			-	0.5	
Input capacitance	C_{IN}	V_{IN} = 0.0 V f = 1MHz, see 4.3.1c	4		-	20	pF
Functional testing		See 4.3.1d, V_{CC} = 4.5 V	7, 8	All			
Frequency of operation 4/	f_{MAX}	GND = 0.0 V		01 02 03 04	12.5 12.5 12.5 16.67	16.7 20.0 25.0 33.33	MHz
Cycle time	1	See figure 4	9, 10, 11	01 02 03 04	60 50 40 30	125 80 80 60	ns
Clock pulse width (Measured from 1.5 V to 1.5 V for 33 MHz)	2, 3			01 02 03 04	24 20 15 14	95 54 59 42	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock fall time	4	See figure 4	9, 10, 11	01		5	ns
				02		5	
				03		4	
				04		3	
Clock rise time	5			01		5	
				02		5	
				03		4	
				04		3	
Address valid to AS asserted 5/	6			01	15		
				02	10		
				03	5		
				04	5		
Address valid to DS asserted (read) 5/	6A			01	15		
				02	10		
				03	5		
				04	5		
Address valid to DS asserted (write) 5/	6B			01	50		
				02	50		
				03	35		
				04	26		
AS negated to address invalid 6/	7			01	10		
				02	10		
				03	5		
				04	5		
DS negated to address invalid 6/	7A			01	10		
				02	10		
				03	5		
				04	5		
CS negated to AS asserted 7/	8			01	0		
				02	0		
				03	0		
				04	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CS negated to DS asserted (read) 7/	8A	See figure 4	9, 10, 11	01 02 03 04	0 0 0 0		ns
CS asserted to DS asserted (write)	8B			01 02 03 04	30 25 20 15		
AS negated to CS negated	9			01 02 03 04	10 10 5 5		
DS negated to CS negated	9A			01 02 03 04	10 10 5 5		
R/W high to AS asserted (read)	10			01 02 03 04	15 10 5 5		
R/W high to DS asserted (read)	10A			01 02 03 04	15 10 5 5		
R/W low to DS asserted (write)	10B			01 02 03 04	35 30 25 25		
AS negated to R/W low (read) or AS negated to R/W high (write)	11			01 02 03 04	10 10 5 5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DS negated to R/W low (read) or DS negated to R/W high (write)	11A	See figure 4	9, 10, 11	01 02 03 04	10 10 5 5		ns
DS width asserted (write)	12			01 02 03 04	40 38 30 23		
DS width negated 3/	13			01 02 03 04	40 38 30 23		
DS negated to AS asserted 3/ 8/	13A			01 02 03 04	30 30 25 18		
CS, DS asserted to data out valid (read) 9/	14			01 02 03 04		80 45 45 30	
DS negated to data out invalid (read)	15			01 02 03 04	0 0 0 0		
DS negated to data out high impedance (read) 3/	16			01 02 03 04		50 30 30 30	
Data in valid to DS asserted (write)	17			01 02 03 04	15 10 5 5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DS negated to data in invalid (write)	18	See figure 4	9, 10, 11	01	15		ns
				02	10		
				03	5		
				04	5		
START true to DSACK0 and DSACK1 asserted 9/	19			01		50	
				02		35	
				03		25	
				04		20	
DSACK0 asserted to DSACK1 asserted (skew) 10/	19A			01	-15	15	
				02	-10	10	
				03	-10	10	
				04		5	
DSACK0 or DSACK1 asserted to data out valid	20			01		50	
				02		43	
				03		32	
				04		17	
START false to DSACK0 and DSACK1 negated 11/	21			01		50	
				02		40	
				03		30	
				04		30	
START false to DSACK0 and DSACK1 high impedance 3/ 11/	22			01		70	
				02		55	
				03		55	
				04		40	
START true to clock high (synchronous read) 11/ 12/	23			01	0		
				02	0		
				03	0		
				04	0		
Clock low to data out valid (synchronous read) 12/	24			01		105	
				02		80	
				03		60	
				04		45	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
START true to data out valid (synchronous read) 11/ 12/ 13/	25	See figure 4	9, 10, 11	01	1.5	105+	ns
						2.5	clks
				02	1.5	80+	ns
						2.5	clks
				03	1.5	60+	ns
						2.5	clks
				04	1.5	45+	ns
						2.5	clks
Clock low to DSACK0 and DSACK1 asserted (synchronous read) 12/	26			01		75	ns
				02		55	
				03		45	
				04		30	
START true to DSACK0 and DSACK1 asserted (synchronous read) 11/ 12/ 13/	27			01	1.5	75+	ns
						2.5	clks
				02	1.5	55+	ns
						2.5	clks
				03	1.5	45+	ns
						2.5	clks
				04	1.5	30+	ns
						2.5	clks

1/ The following pins are active low: $\overline{AS}$, $\overline{CS}$, $\overline{DS}$, $\overline{DSACK0}$, $\overline{DSACK1}$, $\overline{RESET}$, $\overline{W}$ of R/$\overline{W}$, $\overline{SENSE}$, $\overline{SIZE}$. Unless otherwise specified, test conditions shall be at worst case condition.

2/ All outputs unloaded except for load capacitance. Clock at f_{Max}. Part in reset.

3/ Tested initially and at process and design changes. Thereafter guaranteed, if not tested, to the limits specified in table I.

4/ $-55°C \le TC \le +125°C$ in a power-off condition under thermal soak for 4 minutes minimum or until thermal equilibrium. Electrical parameters are tested instant on 100 ms after power is applied.

5/ If the SIZE pin is not strapped to either V_{CC} or GND, it must have same setup times as do address.

6/ If the SIZE pin is not strapped to either V_{CC} or GND, it must have same hold times as do address.

7/ If a subsequent access is not a FPCP access, CS must be negated before the assertion of AS and or DS on the non-FPCP

8/ This specification only applies to systems in which back-to-back accesses (read-write or write-write) of the coprocessor interface operand can occur. When the device is used as a coprocessor to the main processor, this can occur when the addressing mode is immediate.

9/ These specifications only apply if the device had completed all operations initiated by the termination of the previous bus cycle when DS was negated. Bus cycles which initiate operations in this manner are:
- Write to coprocessor interface control register LSB.
- Write to coprocessor interface restore register LSB.
- Last write to coprocessor interface operand register LSB during restore with "busy" state size.
- First read to coprocessor interface operand register LSB during save "idle" or "busy" state size.

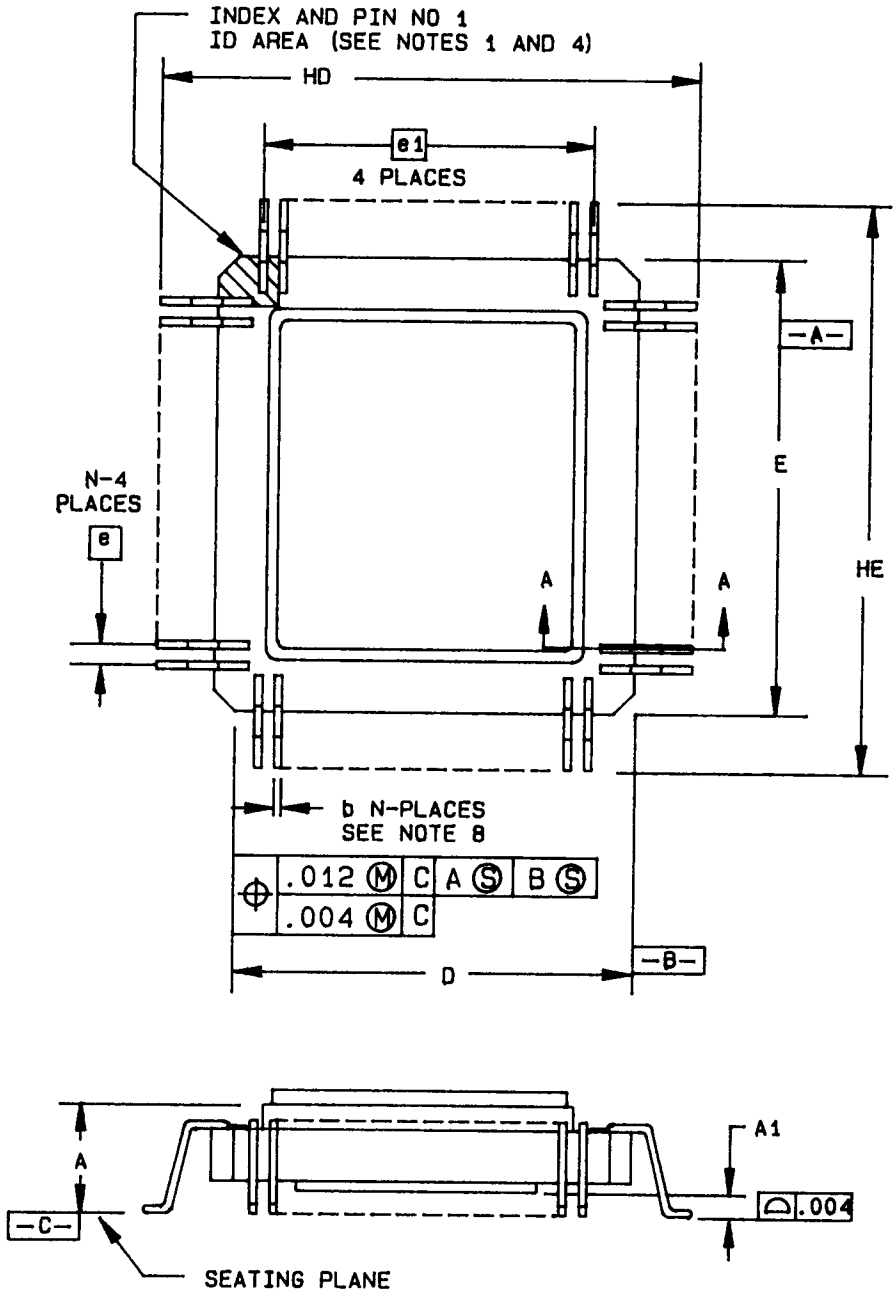
Following one of these bus cycles, all operations are completed within four clocks after DS is negated. If an asynchronous read/write bus cycle is attempted prior to the completion of these operations, the new bus cycle is postponed by DSACK0-DSACK1 (and data for reads) being withheld. DSACK0-DSACK1 (and data for reads) are also withheld on asynchronous reads/writes of the coprocessor interface operand register and register selector register when the MPU overturns the device. Since the device clock may be much slower than the MPU's clock, these registers cold be empty/full when the MPU attempts to read/write.

10/ This number can be reduced to 5 ns if DSACK0 and DSACK1 have equal loads.

11/ START is not an external signal, rather it is logical condition that indicates the start of an access. The logical equation for this condition is: START = CS+AS + (R/W.DS).

12/ Synchronous reads occur only when the coprocessor interface save register or response register locations are read.

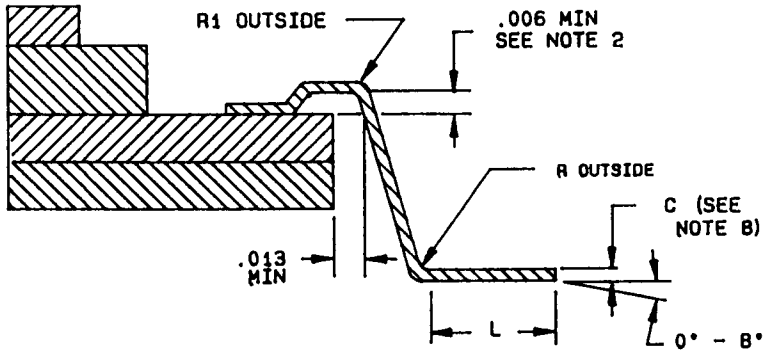
13/ Value depends on actual clock input waveform used and not clock input specifications.



Case Y

FIGURE 1. Case outlines.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89463
		REVISION LEVEL	SHEET 12



SECTION A-A

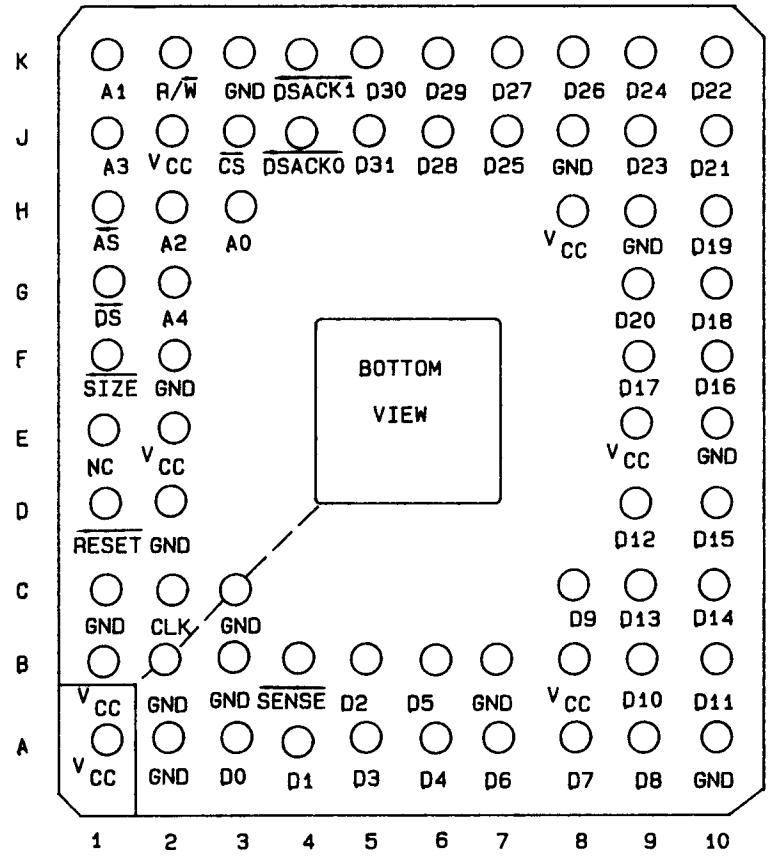
Case Y				
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.125	---	3.18
A1	.018	.035	0.16	0.89
b	.018	.030	0.16	0.76
c	.005	.010	0.13	0.25
D/E	.940	.960	23.88	24.38
e	.050 BSC		1.28 BSC	
e1	.800 BSC		20.32 BSC	
HD/HE	1.133	1.147	28.78	29.13
L	.024	.040	0.61	1.02
N	68		68	
R	.011	.034	0.28	0.87
R1	.009	---	0.23	---

NOTES:
1. A terminal 1 identification mark shall be located at the index corner in the shaded area shown. Terminal 1 is located immediately adjacent to and counterclockwise from the index corner. Terminal numbers increase in a counterclockwise direction when viewed as shown.
2. Generic lead attach dogleg depiction.
3. Dimension N: Number of terminals.
4. Corner shapes (square, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
5. Metric equivalents are given for general information only.
6. Controlling dimension: Inch.
7. Datums X and Y to be determined where center leads exit the body.
8. Dimension b and c include lead finish

FIGURE 1. Case outlines - Continued.

All device types

Case X



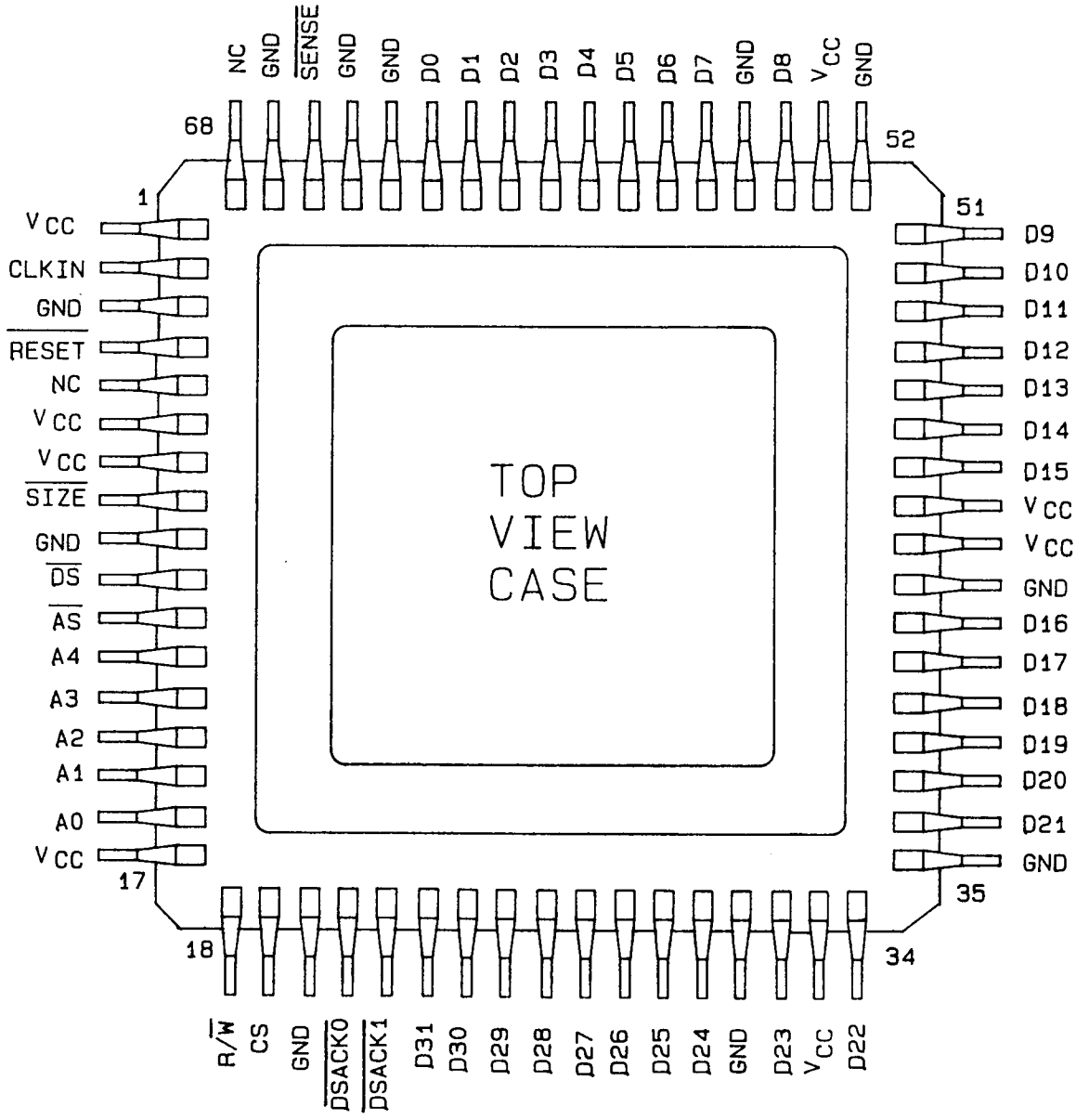
Bottom view

FIGURE 2. Terminal connections.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89463
		REVISION LEVEL	SHEET 14

All device types

Case Y



NC = No connection

FIGURE 2. Terminal connections - Continued.

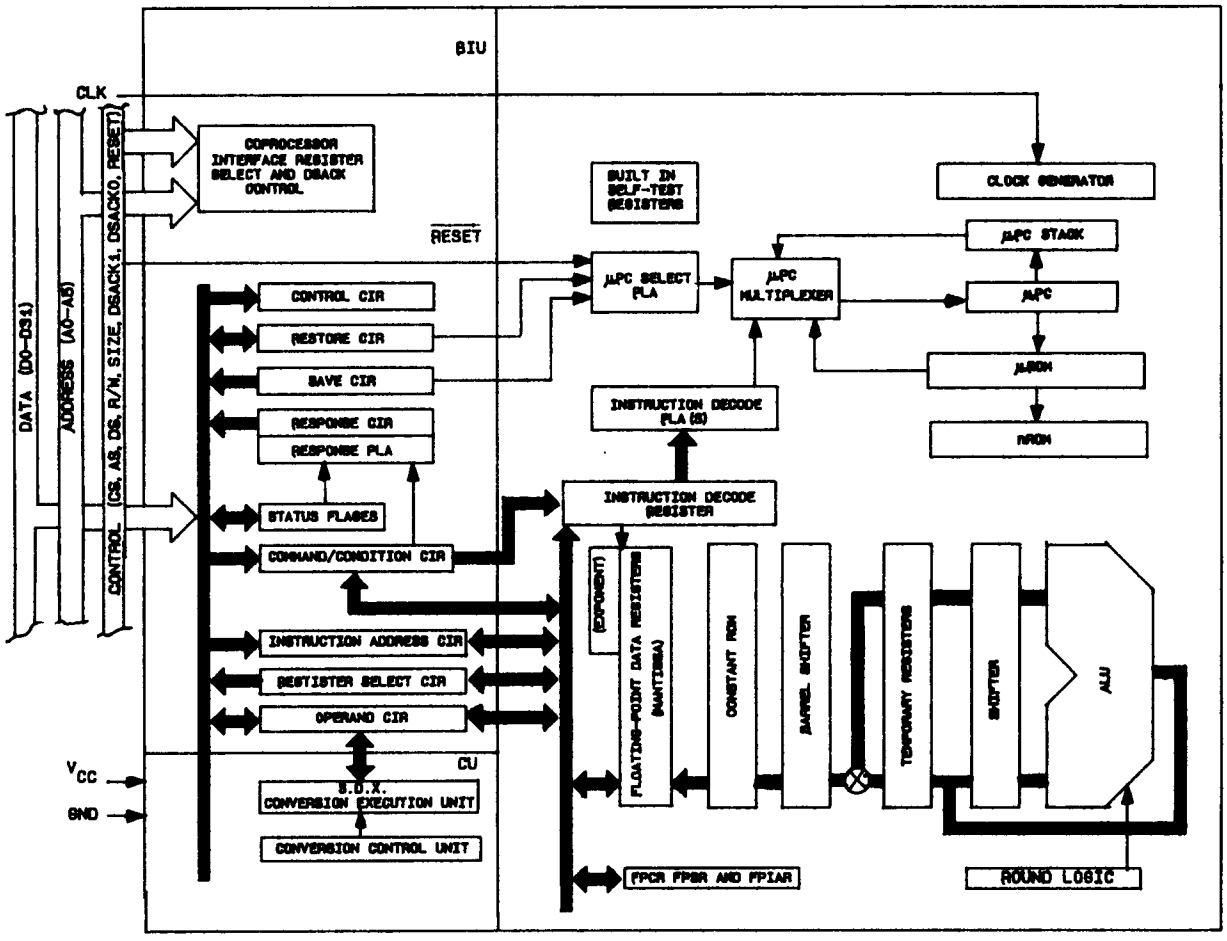
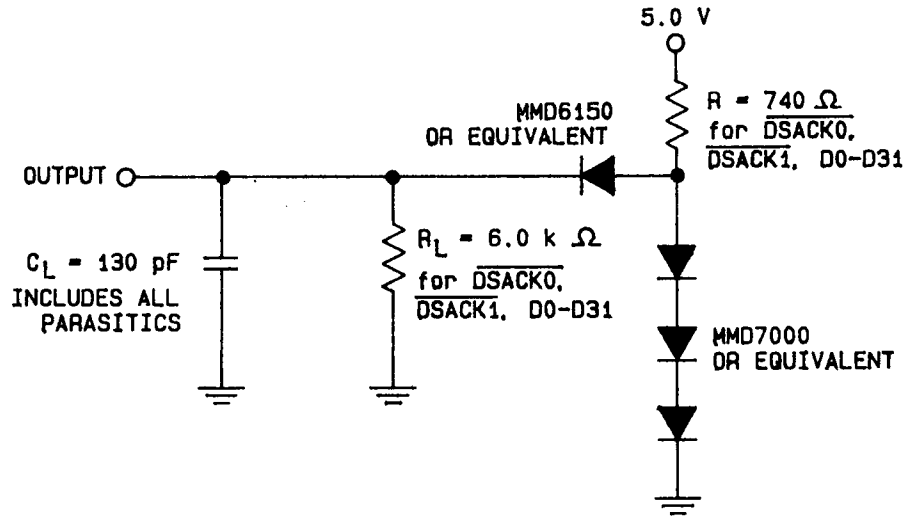


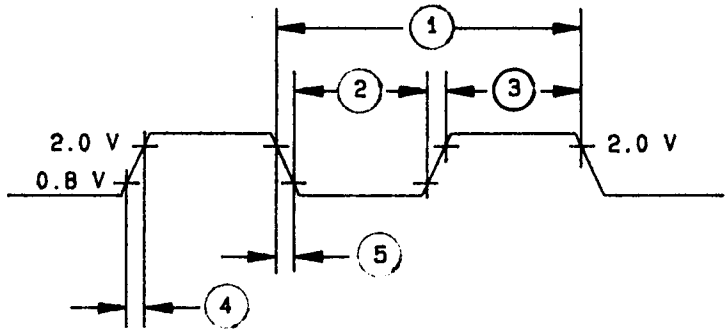
FIGURE 3. Functional block diagram.

Test circuit



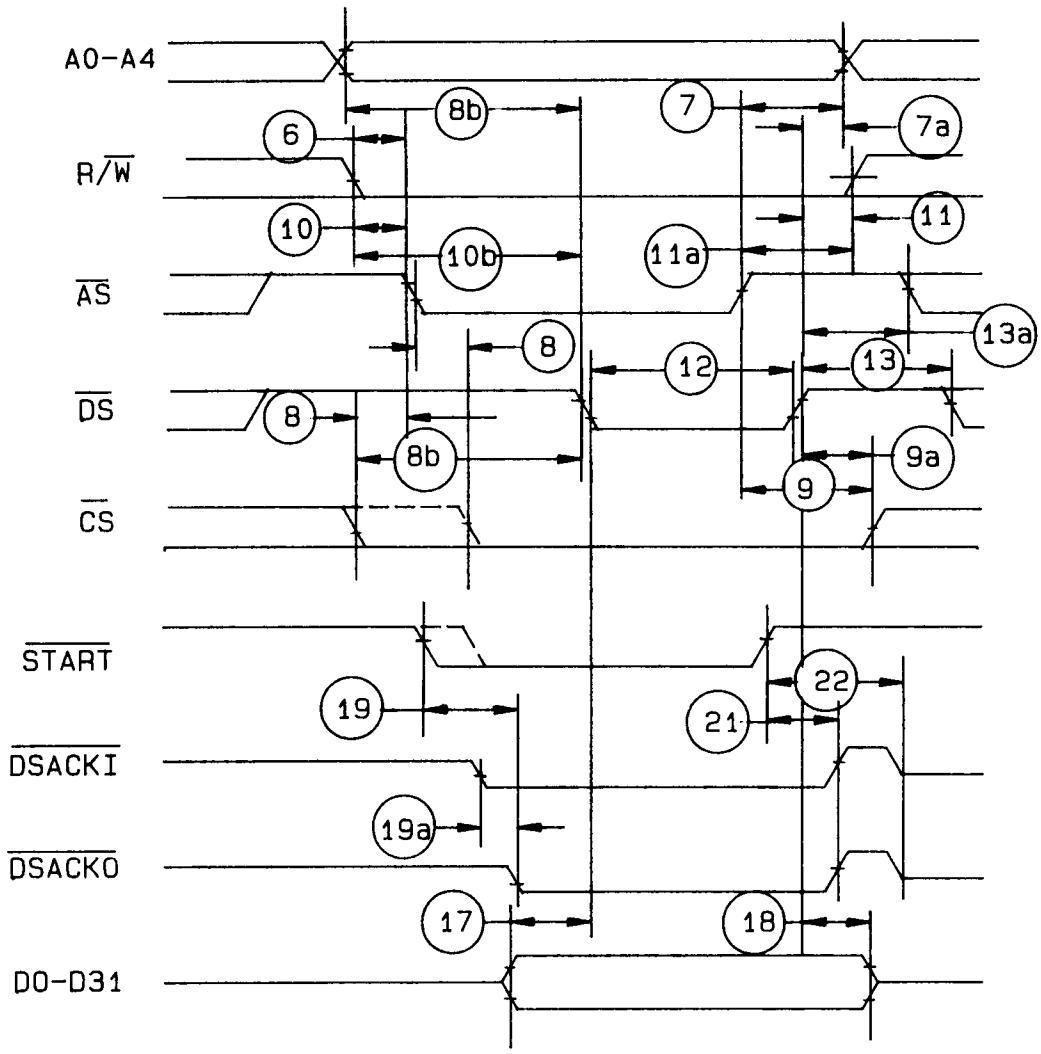
NOTE: Equivalent loading may be simulated by the tester.

Clock input AC timing diagram



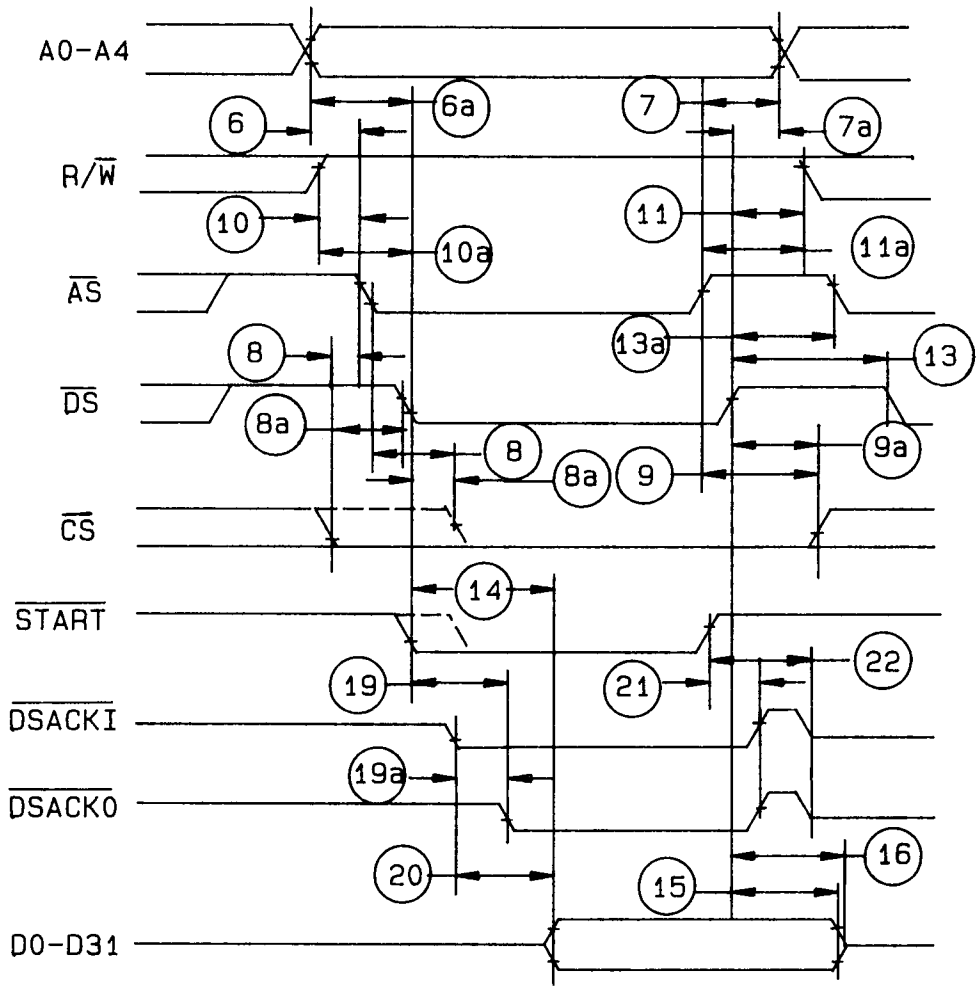
NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise and fall will be linear between 0.8 and 2.0 volts.

FIGURE 4. Switching waveforms and test circuit



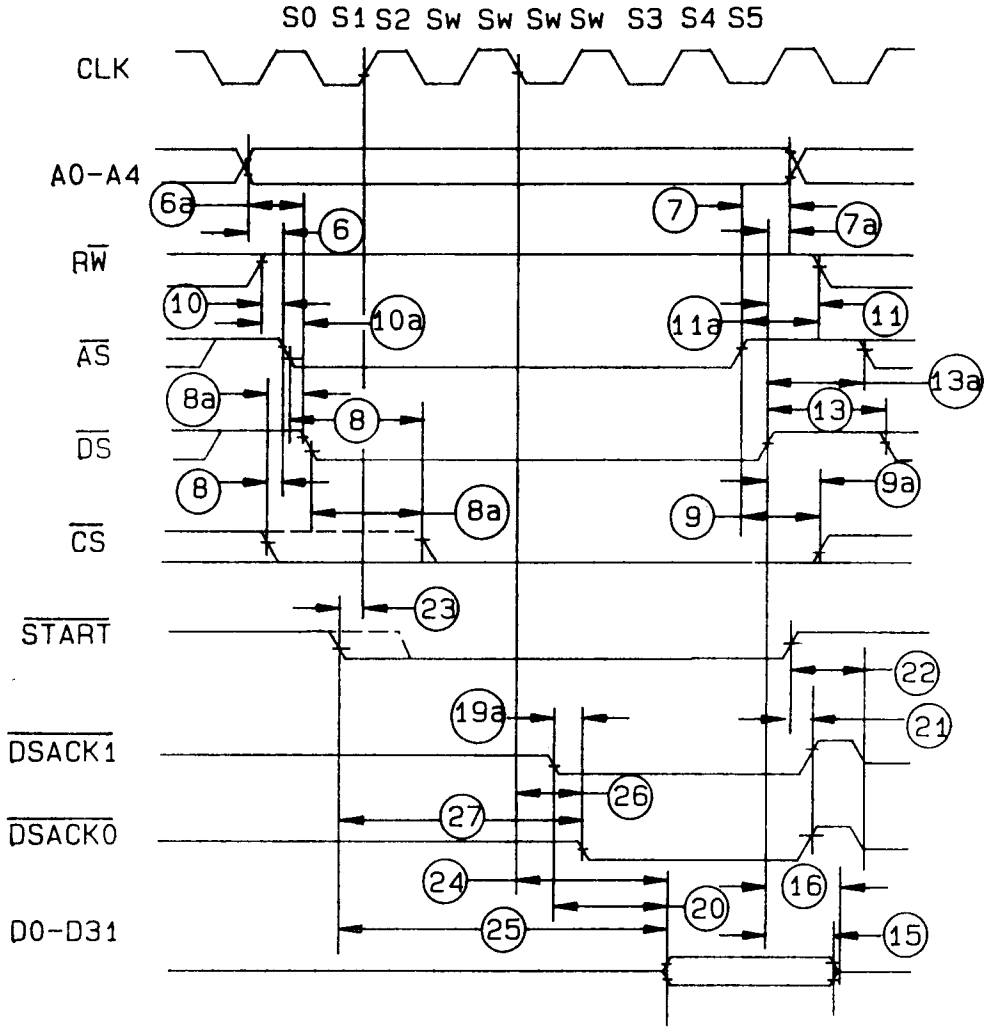
ASYNCHRONOUS WRITE CYCLE TIMING DIAGRAM

FIGURE 4. Switching waveforms and test circuit - Continued.



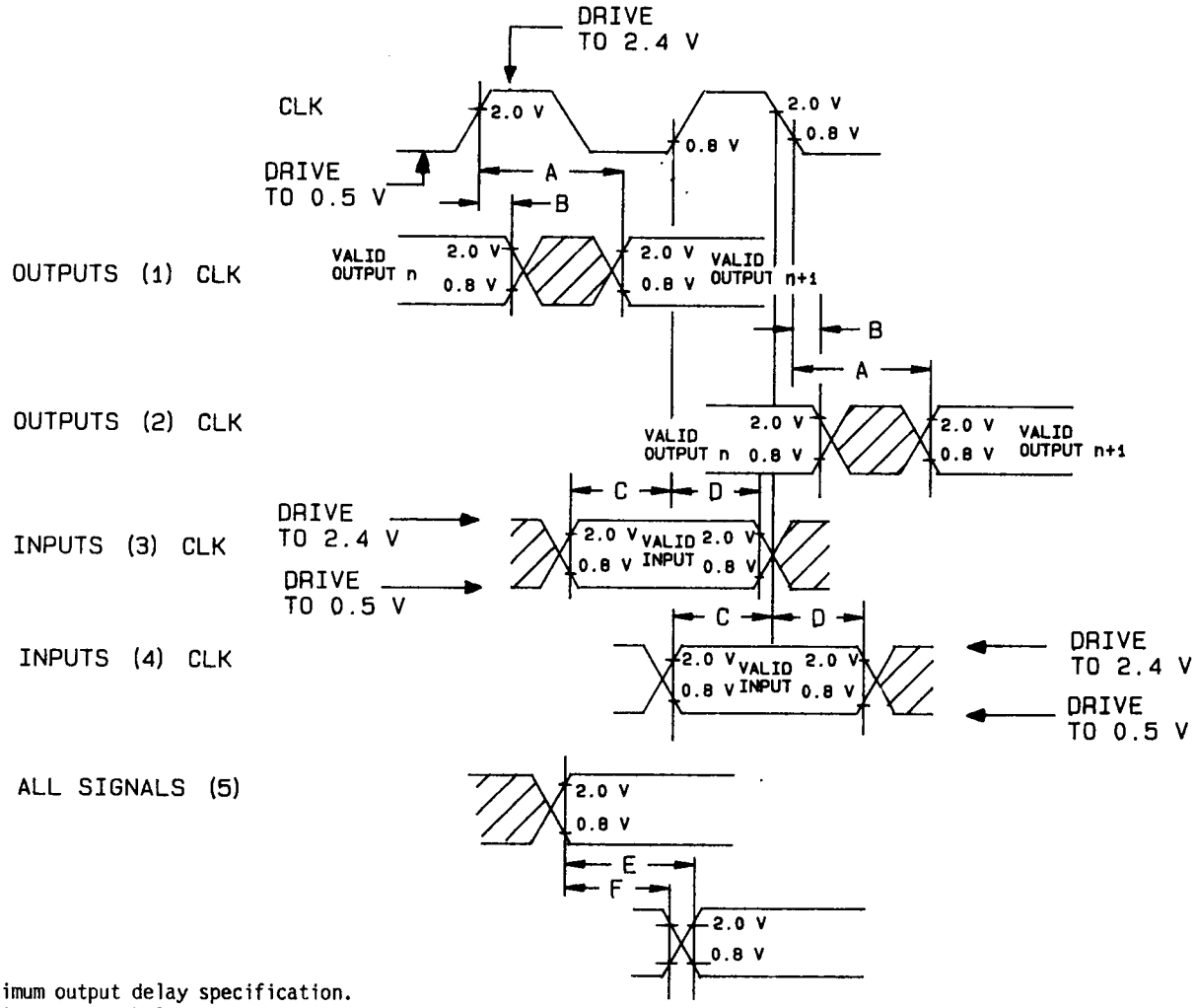
ASYNCHRONOUS READ CYCLE TIMING DIAGRAM

FIGURE 4. Switching waveforms and test circuit - Continued.



SYNCHRONOUS READ CYCLE TIMING DIAGRAM

FIGURE 4. Switching waveforms and test circuit - Continued.



LEGEND:
A - Maximum output delay specification.
B - Minimum output hold time.
C - Minimum input setup time specification.
D - Minimum input hold time specification.
E - Signal valid to signal valid specification (maximum or minimum).
F - Signal valid to signal invalid specification (maximum or minimum).

DRIVE LEVELS AND TEST POINTS FOR AC SPECIFICATION

NOTES:
1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This output timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the rising edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

FIGURE 4. Switching waveforms and test circuit - Continued.

A0	SIZE'	DATA BUS
-	LOW	8 - BIT
LOW	HIGH	16 - BIT
HIGH	HIGH	32 - BIT

SYSTEM BUS SIZE CONFIGURATIONS

DATA BUS	A4	DSACK1'	DSACK0'	COMMENTS
32 - BIT	1	LOW	LOW	VALID DATA ON D31-D0
32 - BIT	0	LOW	HIGH	VALID DATA ON D31-D16
16 - BIT	X	LOW	HIGH	VALID DATA ON D31-D16 OR D15-D0
8 - BIT	X	HIGH	LOW	VALID DATA ON D31-D24, D23-D16, D15-D8, D7-D0
ALL	X	HIGH	HIGH	INSERT WAIT STATES IN CURRENT BUS CYCLE

DSACK ASSERTIONS

NOTE: ' = Asserted LOW

SYSTEM BUS SIZE CONFIGURATIONS AND DSACK ASSERTIONS

FIGURE 4. Switching waveforms and test circuit - Continued.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1,7,9
Final electrical test parameters (method 5004)	1*,2,3,7*, 8a,9,10,11
Group A test requirements (method 5005)	1,2,3,4,7, 8a,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,7,8a, 9,10

* PDA applies to subgroup 1 and 7.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

d. Subgroups 7 and 8 shall include verification of the instruction set. The instruction set forms a part of the vendors test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.6 Symbols, definitions, and functional descriptions.

A0 - A4 (Address bus)

These active-high address line inputs are used by the main processor to select the coprocessor interface register locations located in the CPU address space. When the device is configured to operate over an 8-bit system data bus, the A0 pin is used as an address lead for byte accesses of the coprocessor interface registers. When the device configured to operate over a 16- or 32-bit system data bus, both the A0 and $\overline{SIZE}$ pins are strapped high and/or low as listed in Table 1A.

D0 - D31 (Data bus)

This 32-bit, bidirectional, three-state bus serves as the general-purpose data path between the main processor and the device. Regardless of whether the device is operated as a coprocessor or a peripheral processor, all interprocessor transfers of instruction information, operand data, status information, and requests for service occur as standard similar family bus cycles.
The device may be configured to operate over an 8-, 16-, or 32-bit system data bus. Depending upon the system data bus configuration, both the A0 and $\overline{SIZE}$ pins are configured specifically for the applicable bus configuration. (Refer to address bus (A0 through A5) and $\overline{SIZE}$ for further information.

$\overline{SIZE}$

This active low input signal is used in conjunction with the A0 pin to configure the device for operation over an 8-, 16-, or 32-bit system data bus. When the device is configured to operate over a 16-, or 32-bit system data bus, both the $\overline{SIZE}$ and A0 pins are strapped high and/or low as listed at the end of figure 4.

6.6 Symbols, definitions, and functional descriptions - Continued.

$\overline{AS}$ (Address strobe)

This active low input signal indicates that there is a valid address on the bus, and both the chip select $\overline{CS}$ and Read/Write (R/$\overline{W}$) signal lines are valid.

$\overline{CS}$ (Chip select)

This active low input signal enables the main processor access to the device coprocessor interface registers. When operating the device as a peripheral processor the Chip Select decode is system dependent (i.e., like the Chip Select on any peripheral). The ($\overline{CS}$) signal must be valid as ($\overline{AS}$) is asserted.

R/$\overline{W}$ (Read/Write)

This active low input signal indicates the direction of a bus transaction (read/write) by the main processor. A logic high (1) indicates a read from device and a low (0) indicates a write to the device. The R/$\overline{W}$ signal must be valid when $\overline{AS}$ is asserted.

$\overline{DS}$ (Data strobe)

This active low input signal indicates that there is a valid data on the data bus during a write bus cycle.

$\overline{RESET}$

This active-low input signal causes the device to initialize the floating-point data registers to nonsignaling not-a-numbers (NANs) and clears the floating-point control, status, and instruction address registers.When performing a power-up reset, the external circuitry should keep the $\overline{RESET}$ line asserted for a minimum of four clock cycles after V_{CC} is within tolerance. This assures correct initialization of the device when power is applied. For compatibility with all family devices, 100ms should be used at the minimum. When performing a reset after the device V_{CC} has been within tolerance for more than the initial power-up time, the $\overline{RESET}$ line must have an asserted pulse width which is greater than two clock cycles. For compatibility with all similar family devices, 10-clock cycles should be used as the minimum.

CLK (Clock)

The device clock input is a TTL-compatible signal that is internally buffered for development of the internal clock signals. The clock input must be a constant frequency square wave.

6.6 Symbols, definitions, and functional descriptions - continued.

$\overline{\text{DSACK0}}$, $\overline{\text{DSACK1}}$ (Data transfer and size acknowledge)

These active-low, three-state output signals indicate the completion of bus cycle to the main processor. The device assert either one or both of the ($\overline{\text{DSACK0}}$) and ($\overline{\text{DSACK1}}$) signals upon receipt of a CS assertion. If the bus cycle is a main processor read, the device asserts $\overline{\text{DSACK0}}$ and $\overline{\text{DSACK1}}$ signals to indicate that the information on the data bus is valid. (Both the $\overline{\text{DSACK}}$ signals may be asserted in advance of the valid data being placed on the bus.) If the bus cycle is a main processor write to the device, $\overline{\text{DSACK0}}$ and $\overline{\text{DSACK1}}$ are used to acknowledge acceptance of the data by the device.

The device also uses $\overline{\text{DSACK0}}$ and $\overline{\text{DSACK1}}$ signals to dynamically indicate to the main processor to "port" size (system data bus width) on a cycle-by cycle basis. Depending upon which of the two $\overline{\text{DSACK}}$ pins are asserted in a given busccle, the main processor will assume data has been transferred to/from an 8-, 16-, or 32-bit wide data port. Table 1 lists the $\overline{\text{DSACK}}$ assertions that are used by the device for the various bus cycles over the various system data bus configurations. Figure 4 indicates that all accesses where A4 equals zero are to be 16-bit registers. The device implements all 16-bit coprocessor interface registers on data lines D16-D31; the main processor expects 16-bit registers that are located in a 32-bit port at odd word addresses (A1=1) to be implemented on data lines D0-D15. For accesses to these registers when configured for 32-bit bus operation, the device generates $\overline{\text{DSACK}}$ signals as listed in Table 1 to inform the main processor of valid data on D16-D31 instead of D0-D15. An external holding register is required to maintain both $\overline{\text{DSACK0}}$ and $\overline{\text{DSACK1}}$ high between bus cycles. The $\overline{\text{DSACK0}}$ and $\overline{\text{DSACK1}}$ lines are actively pulled up (negated) by the device following the rising edge of the $\overline{\text{AS}}$ and both $\overline{\text{DSACK}}$ lines are then three-stated (high-impedance state) to avoid interference with the next bus cycle.

$\overline{\text{SENSE}}$

This pin may optionally be used as an additional GND pin, or as an indicator to external hardware that the device is present in the system. This signal is internally connected to the GND of the die, but it is not necessary to connect it to the external ground for correct device operation. If a pull-up resistor is connected to this pin, external hardware may sense the presense of the device in a system. If the pin floats high, the coprocessor is not installed; while the pin will be pulled low if the device is installed in the system.

V_{CC} and GND (Power and ground)

These pins provide the supply voltage and system reference level for the internal circuitry of the device. Care should be taken to reduce the noise level on these pins with appropriate capacitive decoupling.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.