QAM demodulator | TDA8045

FEATURES

- Different modulation schemes: 4, 16, 32 and 64-QAM
- Digital demodulator and Square-Root Raised-Cosine Nyquist filter with roll-off of 20%
- High performance adaptive equalizer (no training sequence needed)
- Digital detectors for generation of required control voltages for carrier recovery, clock recovery and AGC
- Digital-to-Analog Converters (DACs) and operational amplifiers allowing high flexibility for selection of the (PLL) loop time constants
- High maximum symbol frequency: 7 Msymbols/s
- Input format: straight binary or twos complement (up to 9 bits, TTL compatible)
- Output format: 7-bit wide bus (CMOS compatible)
- I²C-bus interface to initialize and monitor the demodulator. When no I²C usage: 64-QAM in default mode, soft or hard decision output for FEC (pin SHND)
- 5 V supply voltage
- Boundary Scan Test.

APPLICATION

Demodulation for digital cable TV.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	–	4.75	5.00	5.25	V
I_{DD}	total supply current at 7 Msymbols/s	V_{DD} = 5 V	–	260	–	mA
f_{sym}	symbol frequency	–	–	–	7	Msymbols/s
IL	implementation loss	notes 1 and 2	–	–	1	dB
α	Nyquist roll-off	–	–	20	–	%
SNR_{lock}	SNR for locking a 64-QAM constellation	–	21	–	–	dB

Notes

1. The implementation loss, IL, of the demodulator is defined as the distance between the measured and theoretical BER curve as function of S/N at a BER = 10^{-6} for a back-to-back measurement at the IF frequency. Of course, this performance depends on the chosen loop parameters (see *"Application Note AN95088"*).
2. The demodulator should be able to acquire lock for a BER $\geq 2 \times 10^{-3}$, because the FEC can still handle this input error rate (see Fig.27).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8045H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

BLOCK DIAGRAM

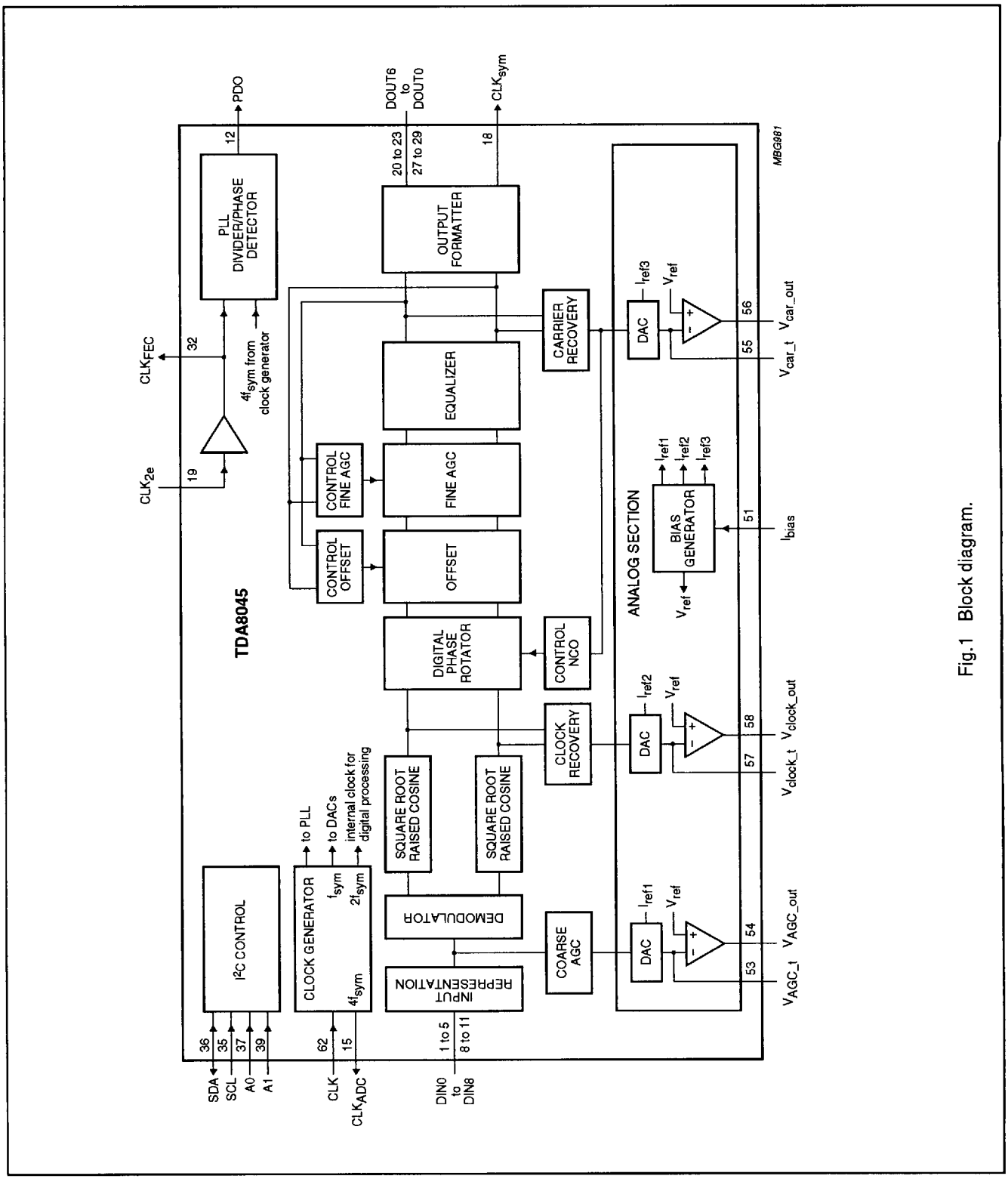


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
DIN0	1	I	digital input bit 0 (LSB)
DIN1	2	I	digital input bit 1
DIN2	3	I	digital input bit 2
DIN3	4	I	digital input bit 3
DIN4	5	I	digital input bit 4
V_{DD}	6	supply	positive supply voltage
V_{SS}	7	supply	negative supply voltage
DIN5	8	I	digital input bit 5
DIN6	9	I	digital input bit 6
DIN7	10	I	digital input bit 7
DIN8	11	I	digital input bit 8 (MSB)
PDO	12	O	PLL phase detector output
V_{DD}	13	supply	positive supply voltage
V_{SS}	14	supply	negative supply voltage
CLK_{ADC}	15	O	clock output to Analog-to-Digital Converter (ADC); $4f_{sym}$
V_{DD}	16	supply	positive supply voltage
V_{SS}	17	supply	negative supply voltage
CLK_{sym}	18	O	symbol clock output (f_{sym})
CLK_{2e}	19	I	clock input for CLK_{FEC} PLL and for test purposes
DOUT6	20	O	parallel data output (bit 6)
DOUT5	21	O	parallel data output (bit 5)
DOUT4	22	O	parallel data output (bit 4)
DOUT3	23	O	parallel data output (bit 3)
V_{SS}	24	supply	negative supply voltage
V_{DD}	25	supply	positive supply voltage
V_{SS}	26	supply	negative supply voltage
DOUT2	27	O	parallel data output (bit 2)
DOUT1	28	O	parallel data output (bit 1)
DOUT0	29	O	parallel data output (bit 0)
CLK_{out}	30	O	clock output to FEC ($2f_{sym}$)
V_{SS}	31	supply	negative supply voltage
CLK_{FEC}	32	O	clock output to FEC ($^{16}/_{3}f_{sym}$)
V_{DD}	33	supply	positive supply voltage
V_{SS}	34	supply	negative supply voltage
SCL	35	I	serial clock of I^2C-bus
SDA	36	I/O	serial data of I^2C-bus
A0	37	I	I^2C hardware address
V_{DD}	38	supply	positive supply voltage
A1	39	I	I^2C hardware address
SHND	40	I	soft hard not decision (sets output mode)

SYMBOL	PIN	I/O	DESCRIPTION
TEST	41	I	test pin (normally connected to ground)
TRST	42	I	optional asynchronous reset
TCK	43	I	dedicated test clock
TMS	44	I	input control signal
V_{DD}	45	supply	positive supply voltage
V_{SS}	46	supply	negative supply voltage
TDO	47	O	serial test data out
TDI	48	I	serial test data in
V_{DD}	49	supply	positive supply voltage
V_{SS}	50	supply	negative supply voltage
I_{bias}	51	I	bias current for DAC
PRESET	52	I	set device into default mode
V_{AGC_t}	53	O	AGC time constant connection
V_{AGC_out}	54	O	analog output for AGC
V_{car_t}	55	O	carrier recovery time constant connection
V_{car_out}	56	O	analog output for carrier recovery
V_{clock_t}	57	O	clock recovery time constant connection
V_{clock_out}	58	O	analog output for clock recovery
V_{SS}	59	supply	negative supply voltage
V_{DD}	60	supply	positive supply voltage
V_{SS}	61	supply	negative supply voltage
CLK	62	I	clock ($4f_{sym}$) input
V_{DD}	63	supply	positive supply voltage
V_{SS}	64	supply	negative supply voltage

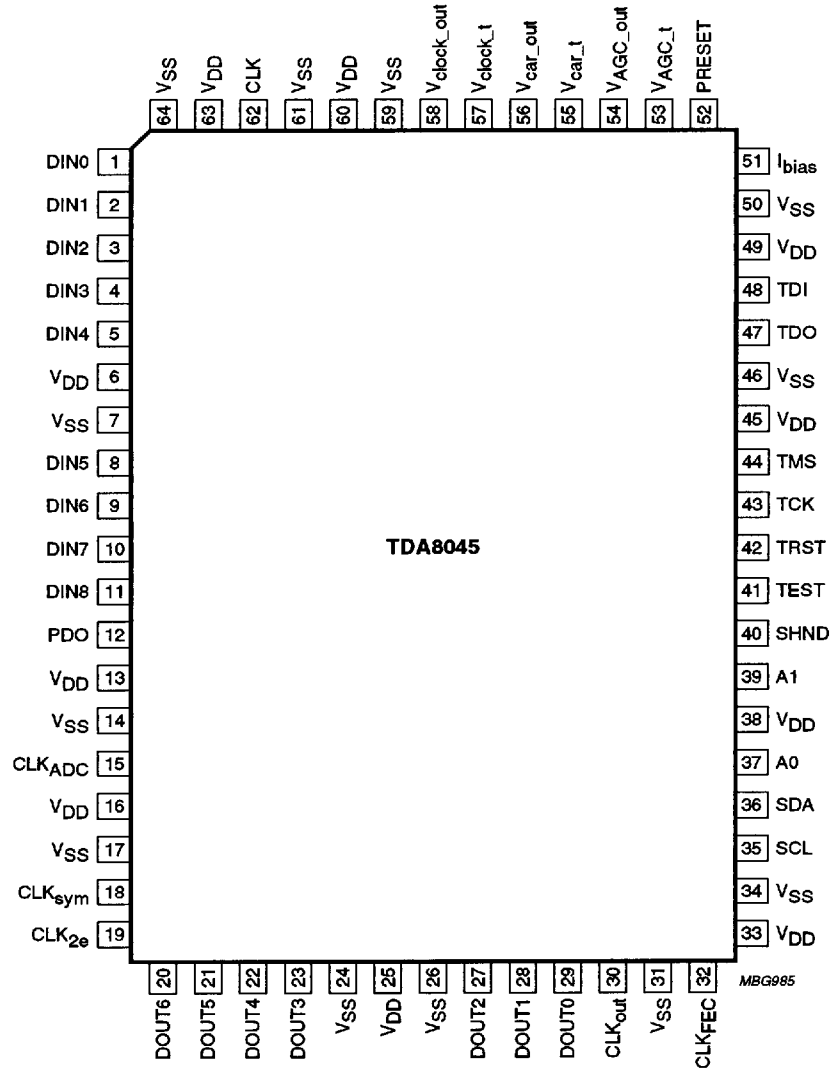


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Figure 3 shows the application of the TDA8045 QAM demodulator. The frequency of the IF signal, IF_{QAM}, is down converted to the symbol frequency f_{sym} by a mixer which is driven from a local oscillator with a frequency of $f_{car} = f_{IF} + f_{sym}$. After low pass filtering this baseband signal is applied to an external 8 or 9-bit ADC. Under normal operating conditions, it is sufficient to use an 8-bit ADC. To avoid additional performance degradation due to adjacent interferences, a 9-bit ADC can be used.

The QAM demodulator generates in a digital way the control values for AGC, Carrier Recovery, and Clock Recovery. The on-chip DACs translate these digital values to analog control currents which are integrated afterwards by a loop filter.

To perform this loop filtering, after each DAC an operational amplifier is integrated.

The carrier recovery consists of a two loop system. The outer loop is shown in the diagram of Fig.3 and controls both phase and frequency at a low speed. The inner loop controls the carrier phase at a high speed (wide loop bandwidth).

Also the AGC consists of two loops; one outer loop called the coarse AGC and one inner loop called the fine AGC.

The recovered symbols are converted into bits according to a demapping scheme and represented at the output in a 7-bit parallel output format. The demodulator can be initialized and monitored by the I²C-bus interface.

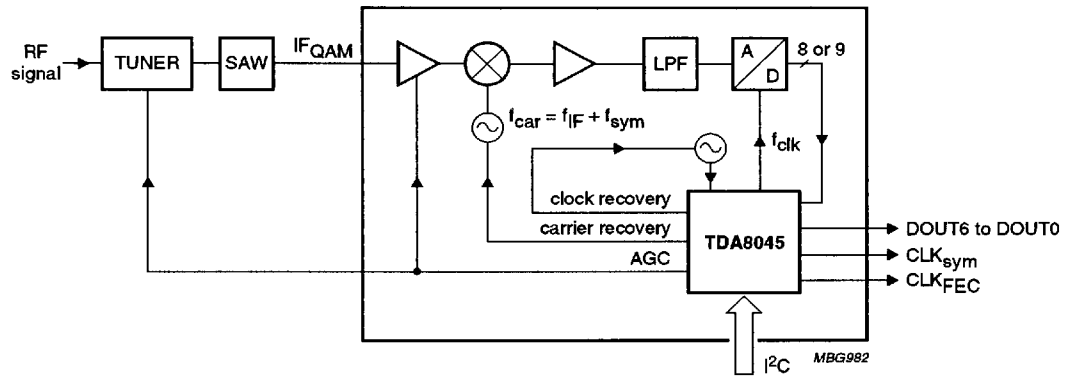


Fig.3 Application circuit.

Functional description of the individual blocks

The functional block diagram of the QAM demodulator is shown in Fig.1. In this section the individual blocks in the demodulator are described. After adaptation for the used input format (twos complement or binary), the input signal is demodulated in the I and Q baseband signals which are applied to the inputs of the Half Nyquist filter (Square-Root Raised-Cosine). To avoid overloading of the ADC, an AGC detector is placed after the adaptation for the input format. After Half Nyquist filtering, the control value for the clock recovery is generated. In the equalizer, the echos created in the cable network are reduced significantly.

After the equalizer, a 'clean' constellation diagram is present from which the information for carrier recovery is derived. This constellation is also applied to the output formatter which demaps the transmitted symbols in corresponding bits. The Carrier Recovery and Lock Detection function are based on the equalizer output. The output of the equalizer is applied to an output formatter, which translates the symbol bits to a FEC input format. The digital outputs of the Clock Recovery, AGC, and Carrier Recovery section are converted into currents which are integrated by the loop filters. To make these active loop filters, operational amplifiers are integrated on the chip.

The TDA8045 can handle four different digital modulation schemes; 4, 16, 32 and 64-QAM. These schemes are selectable by the I^2C interface.

Demodulator and Half Nyquist Filter

After selection of the appropriate input format by the I^2C-bus, demodulation is accomplished. The in-phase and quadrature components are both applied to a Half Nyquist filter. Under normal operation this filter gives a 20% roll-off Half Nyquist shaping. The basic schematic of the demodulator followed by the Half Nyquist filter is shown in Fig.4. The signs of the multiplication factors in the Q branch can be inverted. This can be done by using I^2C.

When using an 8-bit ADC the LSB of the 9-bit input word should be connected to the supply. This is to ensure a symmetrical twos complement representation which can be multiplied by −1 in a correct (twos complement) way. The characteristics of the demodulator and the Half Nyquist filter are listed in Table 1. The overall transfer function of the Square-Root Raised-Cosine filter is shown in Fig.5.

Table 1 Demodulator and Half Nyquist filter characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Half Nyquist filter						
α	roll-off		–	20	–	%
PBR	passband ripple	$f \leq 0.4f_{sym}$	–	0.05	–	dB
SBR	stopband ripple	$f \leq 0.6f_{sym}$	see Fig.5			
ISI_{power}	power intersymbol interference	note 1	–	−44	–	dB

Note

1. Definition of peak intersymbol interference:

$$ISI_{power}\,(dB) = 10 \log \left[\frac{2 \times \sum_{k=1}^{(N_{conv}-1)/2} |C_{conv}(4k)|^2}{|C_{conv}(0)|^2} \right]$$

   a) where N_{conv} is the number of coefficients C_{conv}. $C_{conv(k)}$ represents the coefficient resulting from the convolution of the transmission and reception filters (k indicates the k^{th} coefficient).

   b) the power ISI specified in Table 1 has been calculated on a filter resulting from the convolution of the TDA8045 filter and a truncated Half Nyquist filter with 41 T/4 taps.

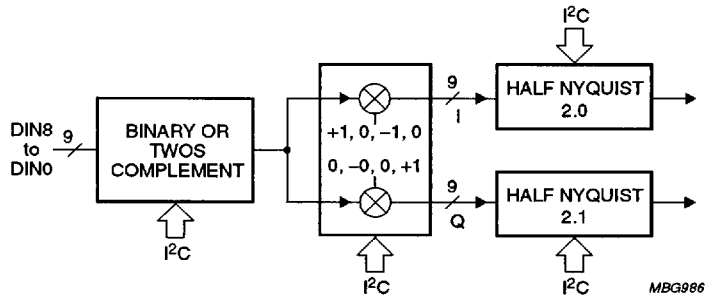
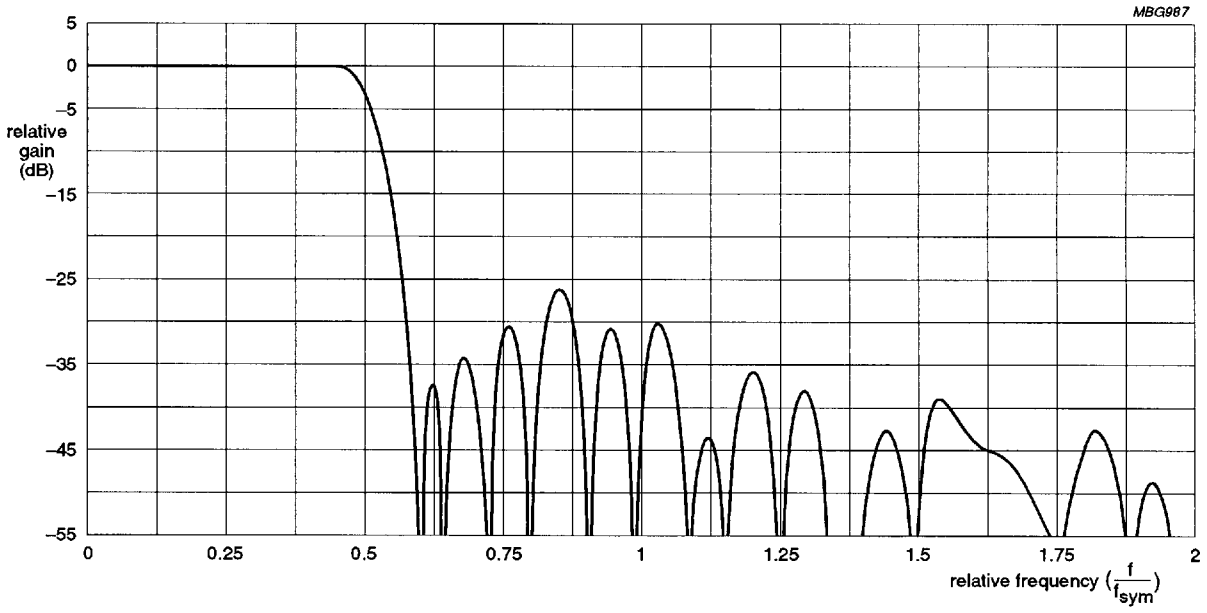


Fig.4 Functional block diagram of the demodulator.



Half Nyquist receiver filter (20% roll-off).
Average passband gain = 1.08.

Fig.5 Transfer function.

EQUALIZER

The equalizer function is realized with four 'T' spaced adaptive filters based on Zero-Forcing algorithm; no training sequence is required. The block schematic of the total equalizer is shown in Fig.7. The main tap of the II and QQ filter is adjustable for fine AGC function (6 dB AGC range). By means of the I²C bus, one can read the settings of the equalizer taps. Only one set of tap values is needed for the two direct filters and one set for the two cross filters.

Besides reading the equalizer tap values, the main tap of the direct filters in the equalizer can also be programmed. After setting the main tap, the other coefficients can be set to zero. Furthermore in the equalizer one can freeze the equalizer settings also by I²C.

The equalizer has been simulated with the echo profile as given in Table 2. From the total system simulations it is concluded that all loops (including equalizer) converges at a SNR of 21 dB for a 64-QAM modulation format.

Table 2 Channel Echo Profile

DELAY	AMPLITUDE	PHASE
$\frac{3}{8}T_{sym}$	0.08	130°
$1\frac{1}{8}T_{sym}$	0.20	60°
$2T_{sym}$	0.05	310°
$4\frac{5}{8}T_{sym}$	0.10	200°
$6\frac{7}{8}T_{sym}$	0.03	200°

Figure 6 represents the QAM spectrum seen by the equalizer. It corresponds (in the frequency domain) to the multiplication of a full Nyquist spectrum by the impulse response of the channel specified by Table 2.

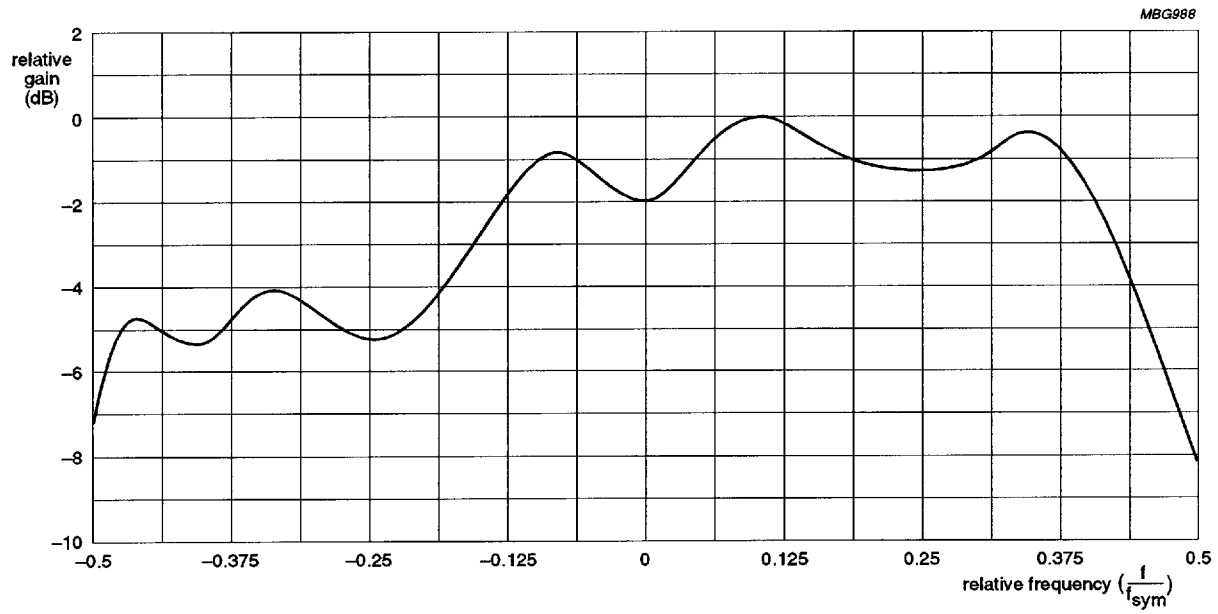


Fig.6 QAM spectrum with echo profile seen by the equalizer.

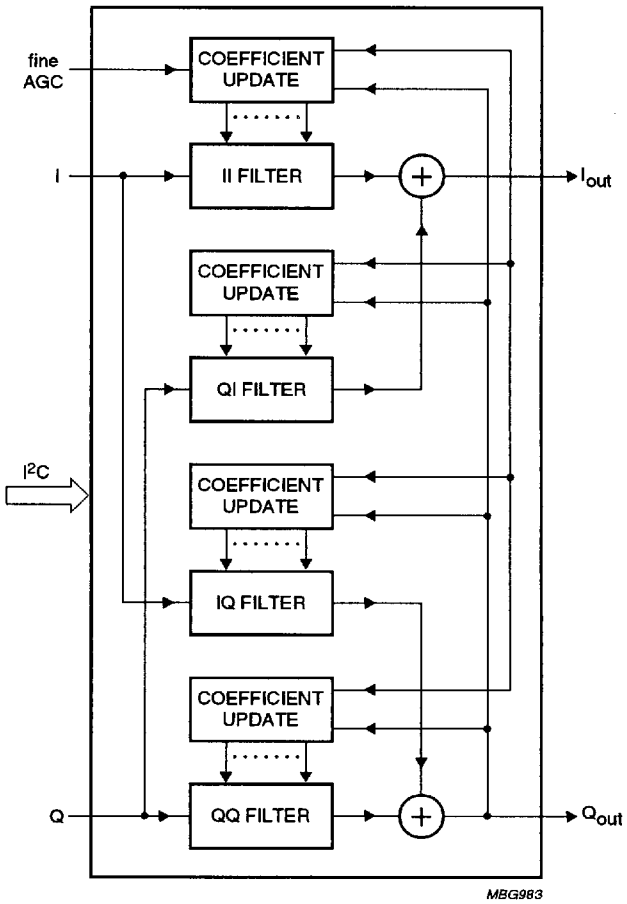


Fig.7 Equalizer block diagram.

LOCK DETECTOR

The lock detector indicates whether all algorithms in the demodulator are converged or not. For a symbol error rate (at the input of the demodulator) smaller than 2×10^{-2}, the detector will give the indication 'LOCK'; I^2C bit LK = 1. For larger symbol error rates, the detector will generate the 'UNLOCK' signal; I^2C bit LK = 0. Note that this 'UNLOCK' signal is generated before any other part of the demodulator loses lock. The lock detector is part of the carrier recovery loop, see Fig.8. The Lock Detector Threshold (LDT) can be changed with the help of I^2C. The nominal LDT values for given S/N ratios are given in Table 3. The estimation algorithm used in the lock detector provides also information about the SER ratio which can be read out by the I^2C-bus interface.

Table 3 Lock detector characteristics

SYMBOL	PARAMETER	CONSTELLATION FORMAT	MIN.	TYP.	MAX.	UNIT
SNR_{lock}	SNR for lock	4-QAM	8	–	–	dB
		16-QAM	15	–	–	dB
		32-QAM	18	–	–	dB
		64-QAM	21	–	–	dB

CARRIER RECOVERY

The carrier recovery detector consists of a Phase-Frequency Detector (PFD) and Phase Detector (PD). Depending on the mode of operation, the carrier recovery is switched either between the phase-frequency detector (no lock) or the phase detector (lock). The carrier recovery consists of the following two loops:

1. The outer loop; this loop is controlling the phase and frequency of the incoming QAM signal at the IF frequency in such a way that the constellation is optimally positioned for detection.
2. The inner loop; the bandwidth of this loop can be large (up to 50 kHz) and can therefore reduce the influence of large bandwidth phase noise.

Four different maximum DAC output currents can be selected with the I²C-bus. The characteristics of the carrier recovery detector are listed in Table 4. The output currents of the DAC are defined in such a way that a VCO with a behaviour as shown in Fig.8 can be connected directly to the output of the integrated operational amplifier. In case the VCO slope is negative the sign of the current can be inverted by I²C. Figure 9 defines also the DAC output currents.

Table 4 Characteristics of the carrier recovery detector
Bias current for DACs is set to 37.5 μA.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Carrier recovery						
K_d	detector constant	SNR = 21 dB for 64-QAM constellation	–	$^6/_2 I_{CAR}$	–	μA/rad
Δf_{car}	frequency range		0.017	–	–	f_{sym}
$f_{n\ in}$	loop bandwidth of inner loop		10	–	50	kHz
$f_{n\ out}$	loop bandwidth of outer loop		–	–	$0.3 f_{n\ in}$	kHz
I_Z	zero current of DAC		–25	–	+25	nA
I_{CAR}	DAC output current range (programmable)		50	–	200	μA
f_{DAC}	DAC sampling rate		–	f_{sym}	–	MHz
Carrier recovery DAC output currents during lock						
$I_{O\text{-}car\text{-}lock}$	mean output current		–	$^1/_2 I_{CAR}$	–	μA
$\Delta I_{O\text{-}car\text{-}lock}$	matching of output currents		–5	–	+5	%
Carrier recovery DAC output currents during unlock						
$I_{O\text{-}car\text{-}unlock}$	mean output current		–	I_{CAR}	–	μA
$\Delta I_{O\text{-}car\text{-}unlock}$	matching of output current		–5	–	+5	%

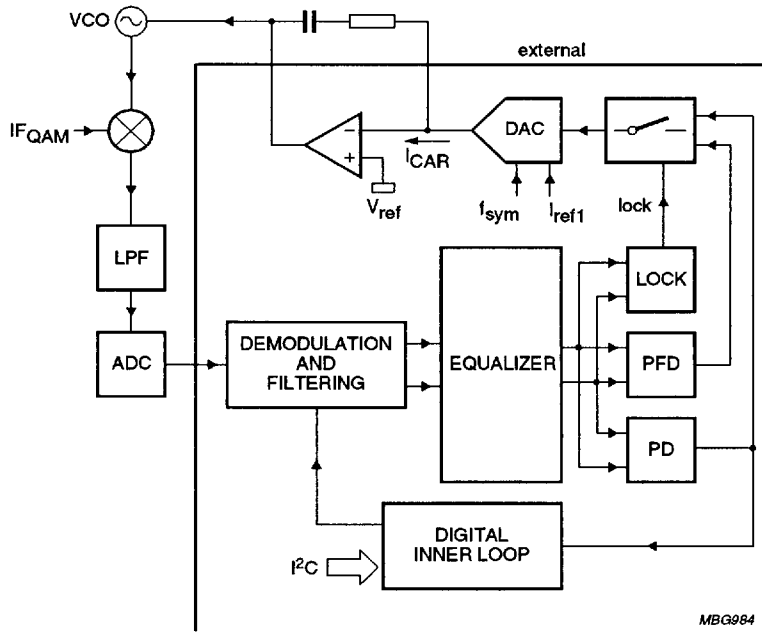


Fig.8 The carrier recovery.

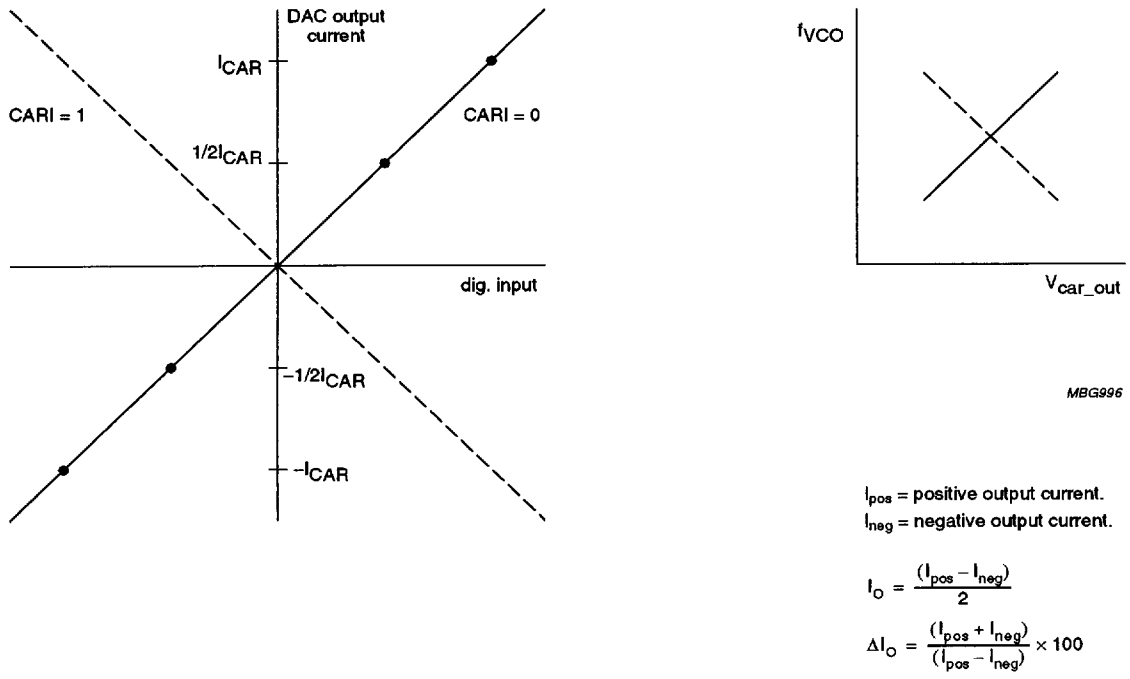


Fig.9 The definition of the DAC currents and the expected frequency behaviour of the VCO.

CLOCK RECOVERY

The clock recovery function uses the unequalized I and Q signals, i.e. the Half Nyquist filter outputs; see Fig.2. The clock recovery section generates a control value each symbol period. As this algorithm is based on the energy maximization, both main and mid symbols are required at the input. So, the input data rate is twice the symbol rate ($2/T_{sym}$). To reduce the data jitter, a prefilter, IIR, in front of the clock recovery detector is included. The functional schematic of this detector is shown in Fig.10.

The clock generator generates from the VCXO clock signal at $4f_{sym}$ the required internal clocks. The input stage amplifier of this generator enables the designer to supply a low amplitude oscillator signal to the TDA8045. The DAC output current range, I_{CLK}, can be varied by means of the I^2C-bus. Also here the sign of the output current can be inverted to adjust for the proper sign of the VCXO slope.

The characteristics of the clock recovery detector are listed in Table 5.

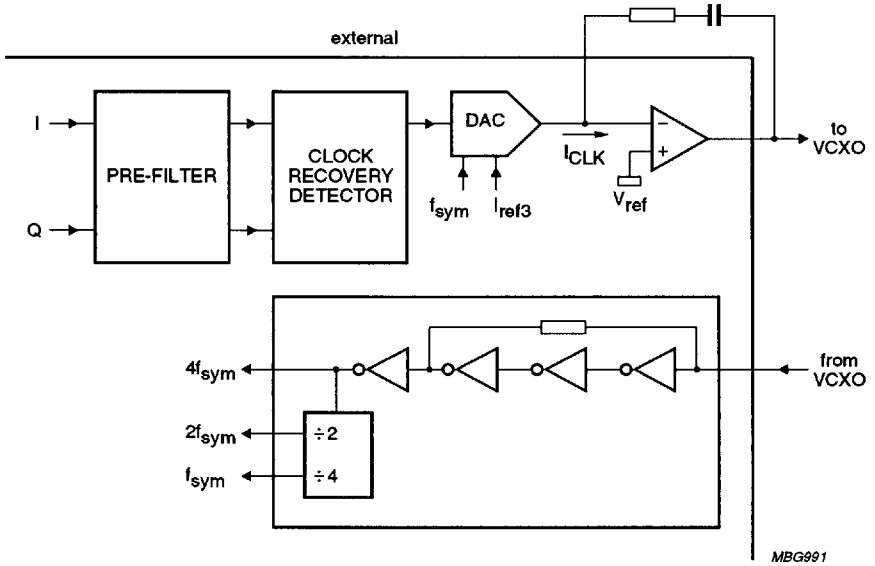


Fig.10 Clock recovery function diagram.

Table 5 Characteristics of the clock recovery detector

Bias current for DACs is set to 37.5 µA.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
K_d	detector constant	SNR = 21 dB for 64-QAM constellation	–	$0.4I_{CLK}$	–	µA/rad
Δf_{CLK}	frequency range		±100	–	–	ppm
f_n	natural frequency		–	400	–	Hz
I_{CLK}	DAC output current range (programmable)		50	–	200	µA
f_{DAC}	DAC sample rate		–	f_{sym}	–	MHz
Clock recovery DAC output currents						
$I_{O\text{-}clk\text{-}lock}$	mean output current		–	I_{CLK}	–	µA
$\Delta I_{O\text{-}clk\text{-}lock}$	matching of output currents		–5	–	+5	%

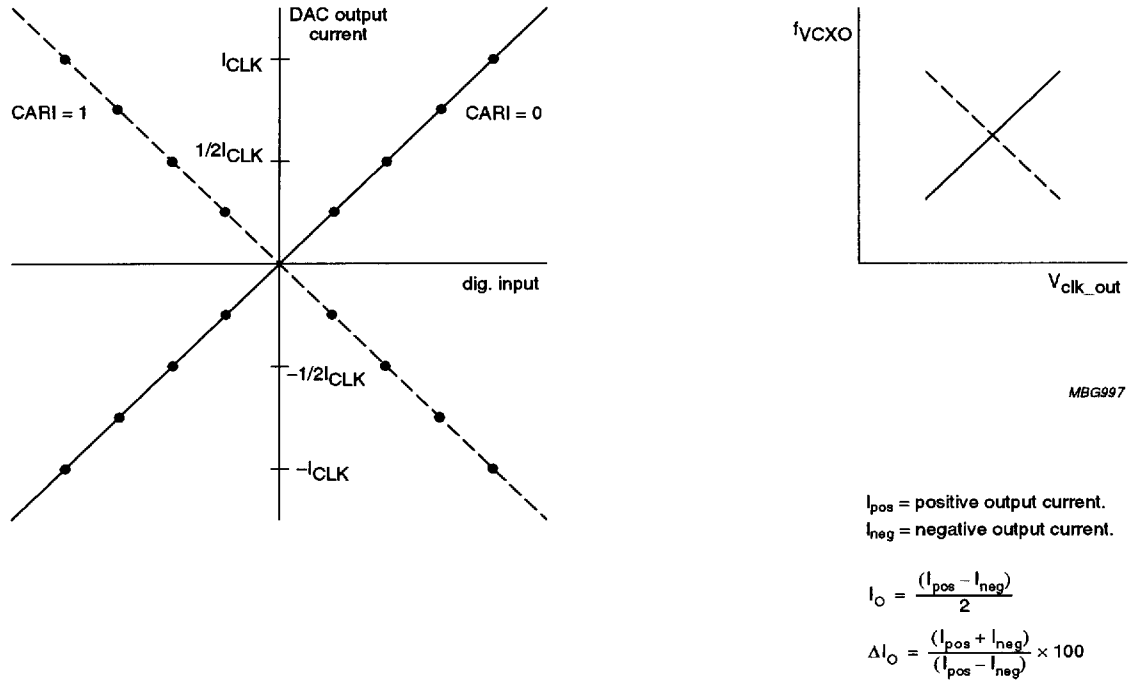


Fig.11 The definition of the DAC currents and the expected frequency behaviour of the VCXO for clock recovery.

AGC

The AGC estimates the mean power based on the digital input signal and relates this to a peak value for a given constellation. To avoid overloading of the ADC, this estimation of the peak signals is used to control the AGC loop. The implemented AGC covers a range of ±20 dB in gain variance.

In case the SAW filter has not sufficient adjacent channel attenuation, the AGC threshold can be varied to avoid clipping of the ADC. To do this, the threshold is made programmable by the I²C-bus (byte ATH).

Table 6 shows that for each mode, a new ATH value (on address 08) must be set with the help of I²C. The I²C data on address 08 is a factor 16 smaller than the used AGC threshold ATH.

The DAC output current range can be varied with the I²C-bus interface (bits AGCA and AGCB) and sign of the current can be inverted (bit AGCI). The output of the AGC amplifier can be monitored and read by the I²C-bus interface (I²C bits AGO).

Table 6 AGC Threshold values

MODE	ATH (AGC THRESHOLD)	I²C DATA FOR ADDRESS 08
4-QAM	496	1F
16-QAM	992	3E
32-QAM	1408	58
64-QAM	1984	7C

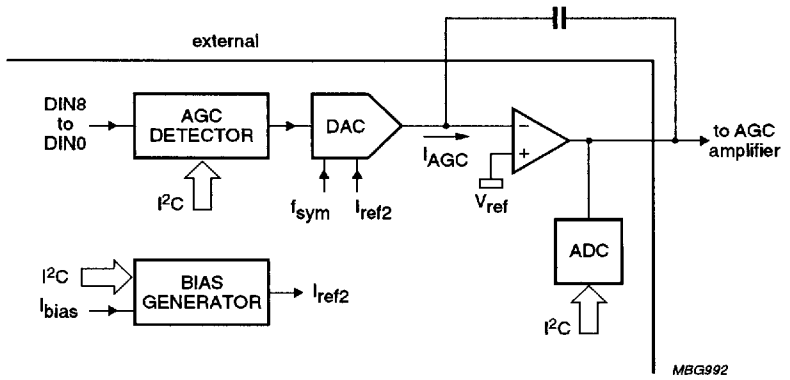


Fig.12 AGC schematic.

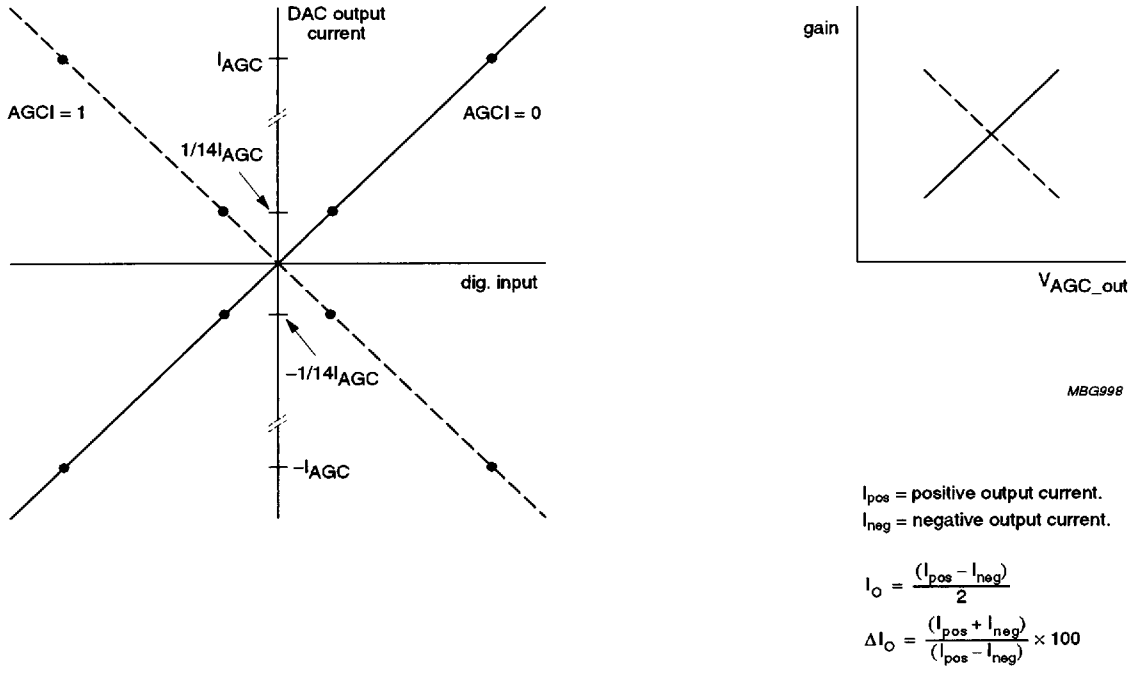


Fig.13 The definition of the DAC currents and the expected behaviour of the AGC.

Table 7 Characteristics of the AGC detector

Bias current for DACs set to 37.5 µA.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
ΔR_{AGC}	AGC range of detector	±20	–	–	dB
I_Z	zero current	−25	–	+25	nA
I_{AGC}	DACs output current range (programmable)	50	–	200	µA
f_{DAC}	DACs sample rate	–	f_{sym}	–	MHz
AGC DAC output currents					
$I_{O\text{-}AGC}$	mean output current (in lock)	–	$^1/_{14}I_{AGC}$	–	µA
	mean output current (unlock)	–	I_{AGC}	–	µA
$\Delta I_{O\text{-}AGC}$	matching of output current	−5	–	+5	%

OFFSET CONTROL

To compensate offsets in the I and Q branch due to spurious signals at the symbol frequency at the ADC input, an offset compensation loop in each of the I and Q branches is included. This loop forces the constellation to be symmetrically distributed over its four quadrants. This function can be switched **off** by I²C (bit OFFS; see Table 14).

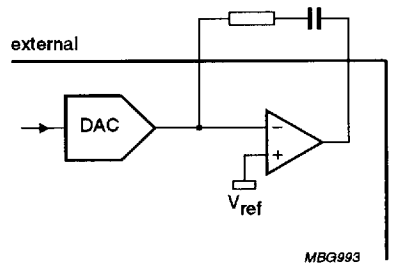


Fig.14 Loop amplifier.

LOOP AMPLIFIERS

The characteristics of the loop amplifiers to enable loop filtering in the loops are listed in Table 8.

Table 8 Characteristics of integrated loop amplifiers

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
G_o	open loop gain	–	60	–	dB
G_{BW}	gain bandwidth product	–	1	–	MHz
V_{ref}	reference voltage	–	2.5	–	V
V_{out}	output voltage range	$0.1V_{DD}$	–	$0.9V_{DD}$	V
$R_{L\ VSS}$	load to ground	5	–	–	kΩ
$R_{L\ VDD}$	load to supply	6.5	–	–	kΩ

OUTPUT FORMATTER

The output formatter transforms the detected I and Q values into bits according to the selected mapping. The TDA8045 has four possible mapping formats which can be selected by the I²C-bus interface (OUTA and OUTB). The demapping procedure and the corresponding bits are defined in Fig.15.

After demapping the bits are allocated to the output. Output format is controlled by I²C-bus interface (TSEL2, TSEL1 and TSEL0). Two main modes are used: 7-bit parallel detected symbol or 7-bit I and Q value (twos complement). The output allocation for the detected symbols corresponds to one of the selected demapping schemes.

The implemented demapping formats and output bit allocation are listed below.

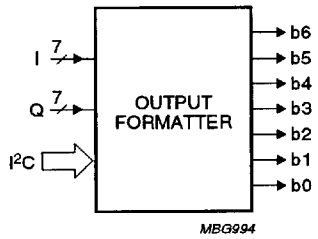
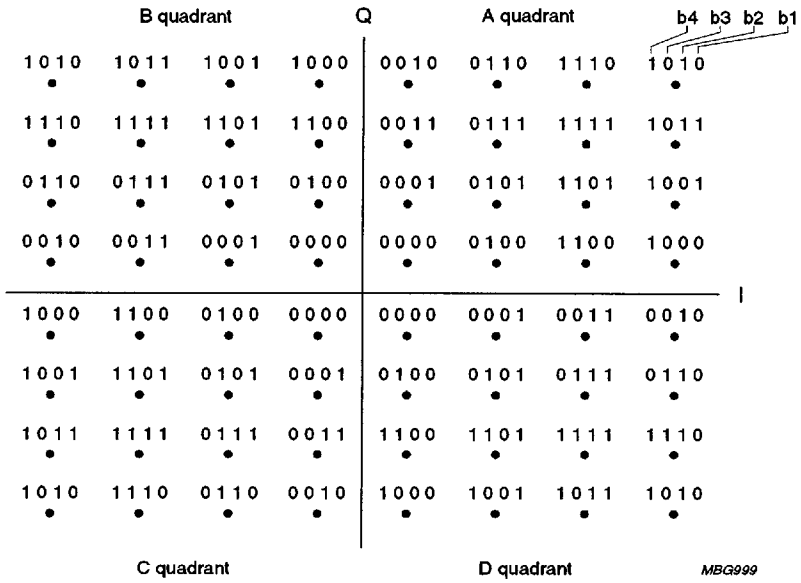


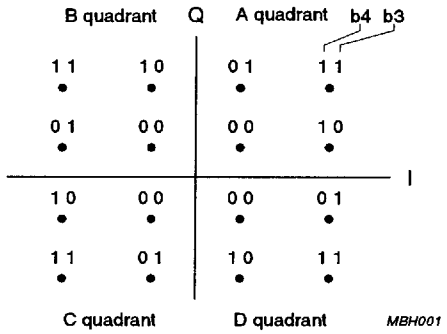
Fig.15 The output formatter.

Demapping scheme 1; differential decoding



Bit allocation for **4-QAM**: b4 = b3 = b2 = b1 = b0 = 0; b6 and b5 differentially decoded (see Table 9).
Bit allocation for **64-QAM**: b4, b3, b2 and b1; b0 = 0; b6 and b5 differentially decoded (see Table 9).

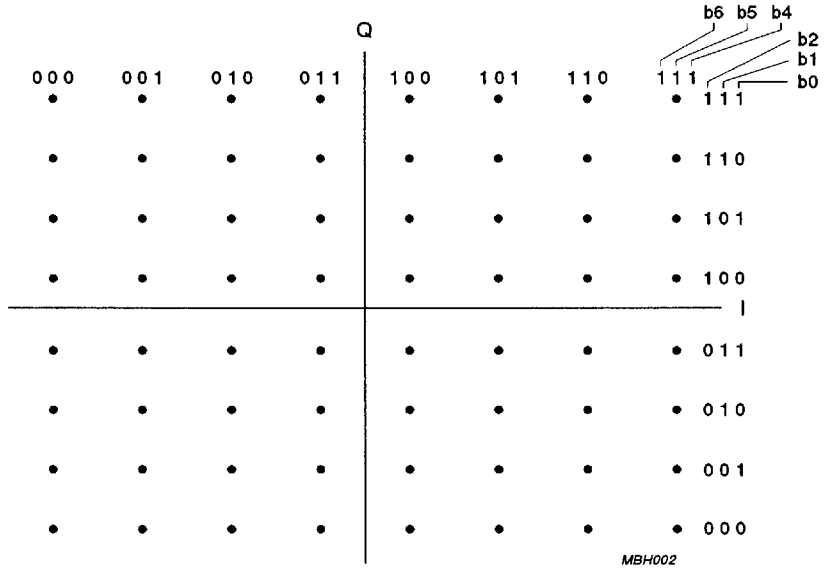
Fig.16 Demapping scheme 1; bit allocation: 4-QAM; 64-QAM.



Bit allocation for **16-QAM**: b4 and b3; b2 = b1 = b0 = 0; b6 and b5 differentially decoded (see Table 9).
Bit allocation for **32-QAM**: not implemented.

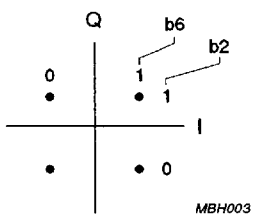
Fig.17 Demapping scheme 1; bit allocation: 16-QAM; 32-QAM.

Demapping scheme 2; direct translation

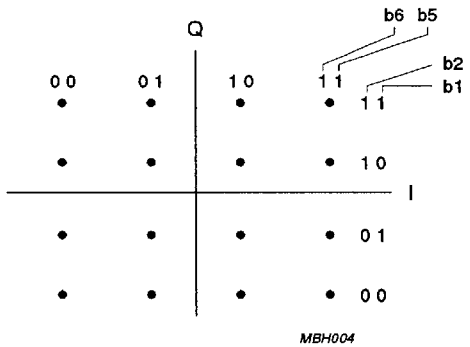


Bit allocation for **64-QAM**: b6, b5, b4, b2, b1, b0; b3 = 0.
Bit allocation for **32-QAM**: not implemented.

Fig.18 Demapping scheme 2; bit allocation: 64-QAM; 32-QAM.



a.

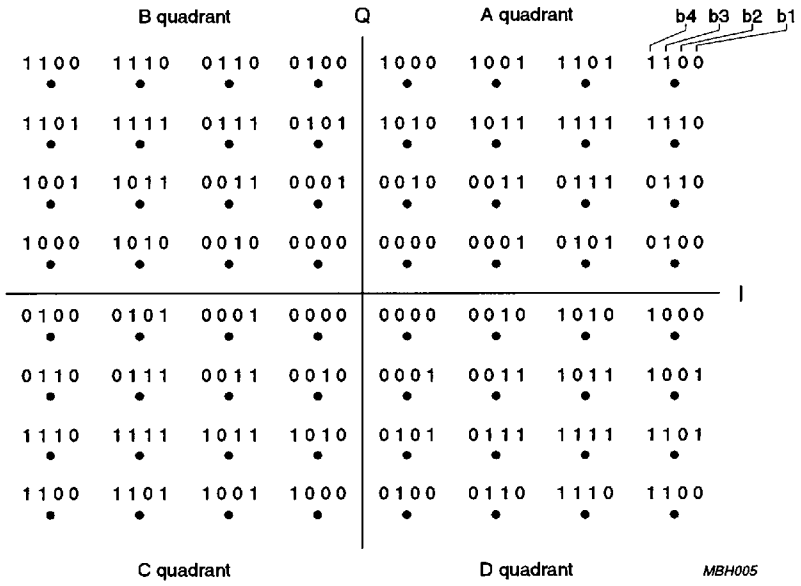


b.

a. Bit allocation for **4-QAM**: b6 and b2; b5 = b4 = b3 = b1 = b0 = 0.
b. Bit allocation for **16-QAM**: b6, b5, b2 and b1; b4 = b3 = b0 = 0.

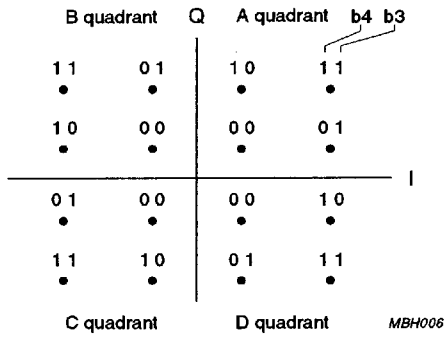
Fig.19 Demapping scheme 2; bit allocation: 4-QAM; 16-QAM.

Demapping scheme 3; differential decoding: Draft prETS 429: 1994



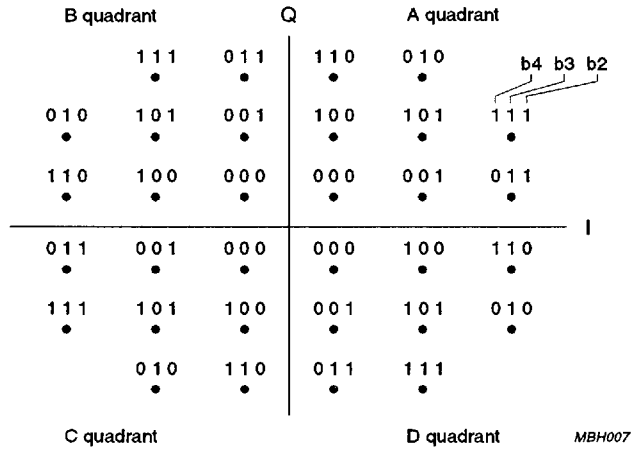
Bit allocation for **4-QAM**: b4 = b3 = b2 = b1 = b0 = 0; b6 and b5 differentially decoded (see Table 9).
Bit allocation for **64-QAM**: b4, b3, b2 and b1; b0 = 0; b6 and b5 differentially decoded (see Table 9).

Fig.20 Demapping scheme 3; bit allocation: 4-QAM; 64-QAM.



Bit allocation for **16-QAM**: b4 and b3; b2 = b1 = b0 = 0; b6 and b5 differentially decoded (see Table 9).

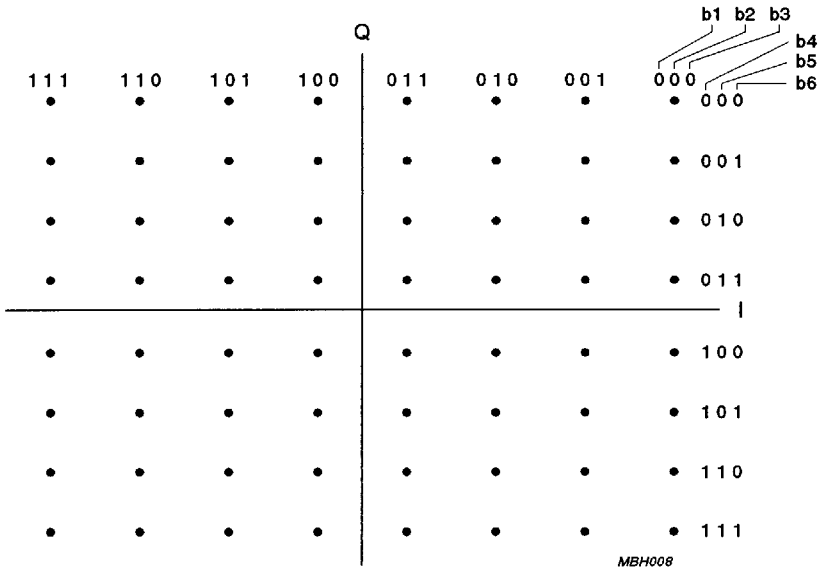
Fig.21 Demapping scheme 3; bit allocation: 16-QAM.



Bit allocation for **32-QAM**: b4, b3 and b2; b1 = b0 = 0; b6 and b5 differentially decoded (see Table 9).

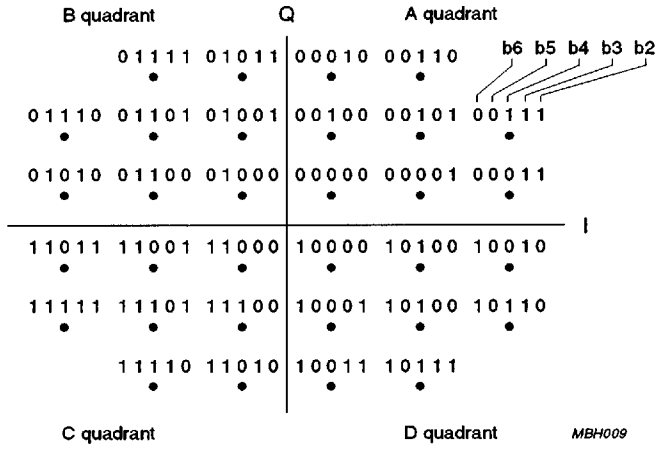
Fig.22 Demapping scheme 3; bit allocation: 32-QAM.

Demapping scheme 4; direct translation: HP8782B/K03



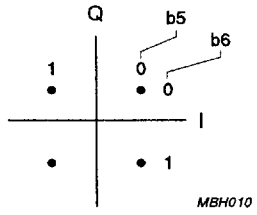
Bit allocation for **64-QAM**: b6, b5, b4, b3, b2 and b1; b0 = 0.

Fig.23 Demapping scheme 4; bit allocation: 64-QAM.

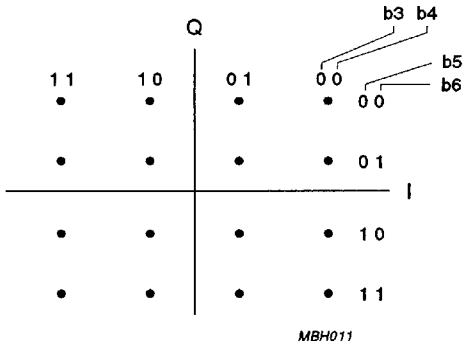


Bit allocation for **32-QAM**: b6, b5, b4, b3 and b2; b1 = b0 = 0.

Fig.24 Demapping scheme 4; bit allocation: 32-QAM.



a.



b.

a. Bit allocation for **4-QAM**: b6 and b5; b4 = b3 = b2 = b1 = b0 = 0.
b. Bit allocation for **16-QAM**: b6, b5, b4 and b3; b2 = b1 = b0 = 0.

Fig.25 Demapping scheme 4; bit allocation: 4-QAM; 16-QAM.

Table 9 Definition of two MSBs in modulation schemes 1 and 3

QUADRANT OF CURRENTLY RECEIVED SYMBOL	QUADRANT OF PREVIOUSLY RECEIVED SYMBOL	PHASE CHANGE (DEGREES)	CURRENT OUTPUT BITS			
			SCHEME 1		SCHEME 3	
			b6	b5	b6	b5
A	A	0	0	0	0	0
A	B	270	1	0	0	1
A	C	180	1	1	1	1
A	D	90	0	1	1	0
B	A	90	0	1	1	0
B	B	0	0	0	0	0
B	C	270	1	0	0	1
B	D	180	1	1	1	1
C	A	180	1	1	1	1
C	B	90	0	1	1	0
C	C	0	0	0	0	0
C	D	270	1	0	0	1
D	A	270	1	0	0	1
D	B	180	1	1	1	1
D	C	90	0	1	1	0
D	D	0	0	0	0	0

PLL DIVIDER AND PHASE DETECTOR

A phase detector with two dividers is included in order to generate a control signal for an external VCO which has to be phase locked on the symbol frequency.

An extra VCO and a passive low pass filter are placed outside the TDA8045. The VCO is running at $^{16}/_{3}f_{sym}$.

The LPF is fed by a phase frequency detector which is implemented on chip. It is comparing the '$^{4}/_{96}f_{sym}$ signal' and the 'squared and by 128 divided $^{16}/_{3}f_{sym}$ signal'. An additional $^{16}/_{3}f_{sym}$ output buffer is available to provide a digital clock signal to the FEC IC.

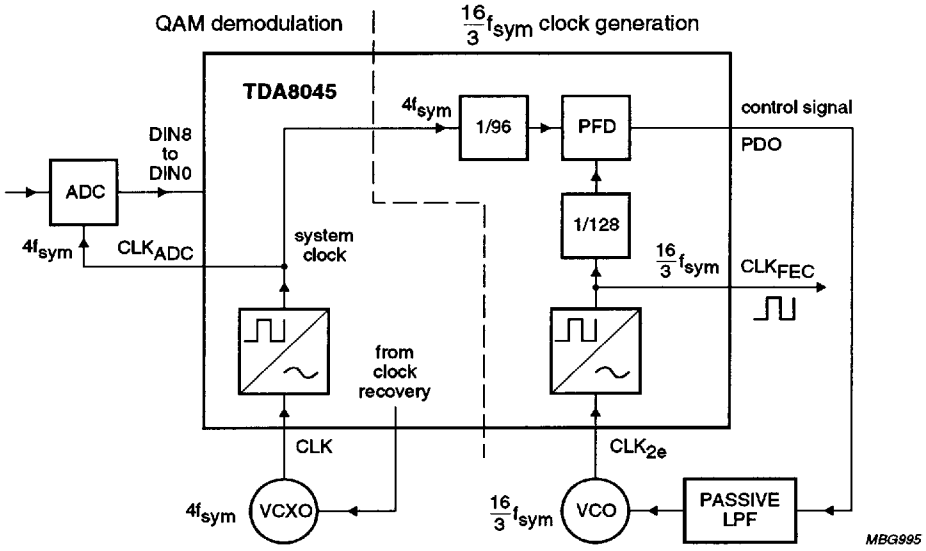


Fig.26 PLL block diagram.

I²C-BUS INTERFACE

The TDA8045 is controlled by an I²C-bus.
For programming, there is one 7-bit module address and the R/W bit for selecting READ or WRITE mode. Note that the TDA8045 starts up according to the settings as defined in Tables 11, 12 and 13.

Table 10 Slave address

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
0	0	0	1	1	A1	A0	X

Table 11 WRITE (R/$\overline{W}$ = 0)

FUNCTION	ADD	D7	D6	D5	D4	D3	D2	D1	D0
General	00	–	–	–	–	OFFS	NYQ	DPHR	RST
Demodulator	01	INP	–	OUTB	OUTA	DEM	–	CONB	CONA
DAC select	02	–	–	AGCB	AGCA	CLKB	CLKA	CARB	CARA
DAC current inversion	03	–	–	–	–	–	AGCI	CLKI	CARI
Digital test mode	04	–	–	–	–	–	TSEL2	TSEL1	TSEL0
Carrier recovery BW	05	DCA7	DCA6	DCA5	DCA4	DCA3	DCA2	DCA1	DCA0
Carrier recovery BW	06	FSOL	DCB2	DCB1	DCB0	–	–	–	DCA8
Lock detector threshold	07	LDT7	LDT6	LDT5	LDT4	LDT3	LDT2	LDT1	LDT0
AGC detector threshold	08	ATH7	ATH6	ATH5	ATH4	ATH3	ATH2	ATH1	ATH0
Equalizer mode	09	–	–	EAR	–	EFCR	EFDI	EFC	PRESET
Equalizer tap TDC	0A	TDC7	TDC6	TDC5	TDC4	TDC3	TDC2	TDC1	TDC0

Table 12 Default settings after reset

FUNCTION	ADD	D7	D6	D5	D4	D3	D2	D1	D0
General	00	–	–	–	–	1	1	1	0
Demodulator	01	1	–	0	1	0	–	1	1
DAC select	02	–	–	0	1	0	0	0	1
DAC current inversion	03	–	–	–	–	–	0	1	0
Digital test mode	04	–	–	–	–	–	0	0	0
Carrier recovery BW	05	0	1	0	0	1	1	1	0
Carrier recovery BW	06	1	0	1	1	–	–	–	0
Lock detector threshold	07	0	0	0	1	1	0	0	1
AGC detector threshold	08	0	1	1	1	1	1	0	0
Equalizer mode	09	–	–	1	–	0	0	0	0
Equalizer tap TDC	0A	0	1	1	1	0	1	1	1

Table 13 READ ($R/\overline{W}$ = 1)

FUNCTION	ADD	D7	D6	D5	D4	D3	D2	D1	D0
V_{car_out} (4 bits)	00	–	–	–	–	CR03	CR02	CR01	CR00
V_{clock_out} (4 bits)	01	–	–	–	–	CL03	CL02	CL01	CL00
V_{AGC_out} (4 bits)	02	–	–	–	–	AG03	AG02	AG01	AG00
Lock detector	03	–	–	–	ALEQ	–	–	–	LK
SER estimation	04	LE7	LE6	LE5	LE4	LE3	LE2	LE1	LE0

I²C WRITE PARAMETERS

Table 14 I²C write parameters; 1-bit values

PARAMETER	BIT	VALUE	DESCRIPTION
Input format	INP	0	twos complement
		1	straight binary
Inversion demodulator	DEM	0	Q-branch = 0,–1, 0, +1
		1	Q-branch = 0,+1, 0, –1
Half Nyquist filter	NYQ	0	filter in bypass mode (only for test purposes)
		1	Half Nyquist filter
Digital phase rotator	DPHR	1	**on**
		0	**off**
Digital filter select	FSOL	0	first order loop (test mode)
		1	second order loop (normal mode)
General reset	RST	0	normal operation
		1	reset (with automatic return to normal operation)
Offset	OFFS	0	switch **off**
		1	switch **on**
DAC current inversion	CARI	0	no inversion
		1	inversion
	CLKI	0	no inversion
		1	inversion
	AGCI	0	no inversion
		1	inversion
Equalizer	PRESET	0	normal operation
		1	coefficient to zero (main tap to '01110111')
	EFCR (Equalizer Freeze Cross) FIR	0	normal operation
		1	freeze coefficients
	EFDI (Equalizer Freeze Direct FIR)	0	normal operation
		1	freeze coefficients
	EFC (Fine AGC (Equalizer Freeze Center tap))	0	normal operation
		1	freeze center tap, no fine AGC
	EAR (Equalizer Auto Reset)	0	**off**
		1	**on**

Table 15 I²C write parameter: constellation; 2-bit values

BITS		DESCRIPTION
CONB	CONA	
0	0	4-QAM
0	1	16-QAM
1	0	32-QAM
1	1	64-QAM

Table 16 I²C write parameter: output format; 2-bit values

BITS		DESCRIPTION
OUTB	OUTA	
0	0	scheme 1
0	1	scheme 2
1	0	scheme 3
1	1	scheme 4

Table 17 I²C write parameter: DAC carrier recovery (maximum current); 2-bit values

BITS		DESCRIPTION
CARB	CARA	
0	0	50 μA
0	1	100 μA
1	0	150 μA
1	1	200 μA

Table 18 I²C write parameter: DAC clock recovery (maximum current); 2-bit values

BITS		DESCRIPTION
CLKB	CLKA	
0	0	50 μA
0	1	100 μA
1	0	150 μA
1	1	200 μA

Table 19 I²C write parameter: DAC AGC (maximum current); 2-bit values

BITS		DESCRIPTION
AGCB	AGCA	
0	0	50 μA
0	1	100 μA
1	0	150 μA
1	1	200 μA

Table 20 I²C write parameters; 3-bit values

PARAMETER	BITS			DOUT6 TO DOUT0
	TSEL2	TSEL1	TSEL0	
Functional Test	0	0	0	default mode SHND = 0: scheme 1 to 4 SHND = 1: multiplexed I/Q
	0	0	1	scheme 1 to 4
	0	1	0	multiplexed I/Q
	0	1	1	test mode 1
	1	0	0	test mode 2
	1	0	1	test mode 3
	1	1	0	test mode 4
	1	1	1	test mode 5

I²C READ PARAMETERS

Table 21 I²C read parameters; 1-bit values

PARAMETER	BIT	VALUE	DESCRIPTION
Lock detect	LK	0	no lock
		1	lock
Alarm equalizer	ALEQ	0	normal operation (alarm **off**)
		1	divergence detected (alarm **on**)

Table 22 I²C read parameter: ADC carrier recovery; 4-bit values

BITS				DESCRIPTION
CR03	CR02	CR01	CR00	
b3	b2	b1	b0	Carrier recovery: $V_{car\_out} = 0.25 + {}^{VDD}/_{16}(8b3 + 4b2 + 2b1 + b0)$ V

Table 23 I²C read parameter: ADC clock recovery; 4-bit values

BITS				DESCRIPTION
CL03	CL02	CL01	CL00	
b3	b2	b1	b0	Clock recovery: $V_{clock\_out} = 0.25 + {}^{VDD}/_{16}(8b3 + 4b2 + 2b1 + b0)$ V

Table 24 I²C read parameter: ADC AGC; 4-bit values

BITS				DESCRIPTION
AG03	AG02	AG01	AG00	
b3	b2	b1	b0	AGC: $V_{AGC\_out} = 0.25 + {}^{VDD}/_{16}(8b3 + 4b2 + 2b1 + b0)$ V

Table 25 I²C read parameter; 8-bit values

PARAMETER	BITS[1]								DESCRIPTION
	LE7	LE6	LE5	LE4	LE3	LE2	LE1	LE0	
SER[2]	b7	b6	b5	b4	b3	b2	b1	b0	SER = f(b7, b6, b5, b4, b3, b2, b1, b0)

Notes

1. The bits LE7 to LE0 give the number of symbols falling inside the lock detector active areas. The count is made during an observation period (256 to 2048 symbols).
2. To get more details about the SER estimation, refer to the *"Application Note AN95088"*.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.3	6.0	V
V_{max}	maximum voltage on all pins		0	V_{DD}	V
P_{tot}	total power dissipation	T_{amb} = 70 °C	−	1.5	W
		T_{amb} = 60 °C	−	1.8	W
		T_{amb} = 50 °C	−	2.0	W
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	45	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

ELECTRICAL CHARACTERISTICS OF DIGITAL INPUTS AND OUTPUTS

V_{DD} = 5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital outputs: DOUT6 to DOUT0						
V_{OL}	LOW level output voltage		0	−	$0.1V_{DD}$	V
V_{OH}	HIGH level output voltage		$0.9V_{DD}$	−	V_{DD}	V
t_{od}	delay time		−	−	22	ns
t_{oh}	hold time		−	−	22	ns
C_L	load capacitance		−	−	30	pF
Digital inputs: DIN8 to DIN0						
V_{IL}	LOW level input voltage		0	−	0.8	V
V_{IH}	HIGH level input voltage		2	−	V_{DD}	V
t_{su}	set-up time		−	−	15	ns
t_{ih}	hold time		−	−	0	ns
C_i	input capacitance		−	−	10	pF
Clock inputs: CLK and CLK_{2e}						
$V_{in(rms)}$	input level	sine wave	100	−	−	mV
T_{cy}	cycle time		35	−	−	ns
t_w	pulse width	40 : 60 duty factor	14	−	−	ns
R_{source}	source resistance		−	−	50	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock outputs: CLK_{ADC} and CLK_{FEC}						
V_{OL}	LOW level output voltage		0	–	$0.1V_{DD}$	V
V_{OH}	HIGH level output voltage		$0.9V_{DD}$	–	V_{DD}	V
T_{cy}	cycle time		35	–	–	ns
t_w	pulse width	40 : 60 duty factor	14	–	–	ns
t_r	rise time	C_L = 30 pF	–	–	6	ns
t_f	fall time	C_L = 30 pF	–	–	6	ns
R_L	load		1	–	–	kΩ
Clock outputs: CLK_{sym} and CLK_{out}						
V_{OL}	LOW level output voltage		0	–	$0.1V_{DD}$	V
V_{OH}	HIGH level output voltage		$0.9V_{DD}$	–	V_{DD}	V
t_r	rise time	C_L = 30 pF	–	–	6	ns
t_f	fall time	C_L = 30 pF	–	–	6	ns
Loop amplifiers						
V_o	output range		$0.1V_{DD}$	–	$0.9V_{DD}$	V
G_o	DC voltage gain (open loop)		–	60	–	dB
G_B	gain bandwidth product		–	1	–	MHz
R_L	load resistance		5	–	–	kΩ

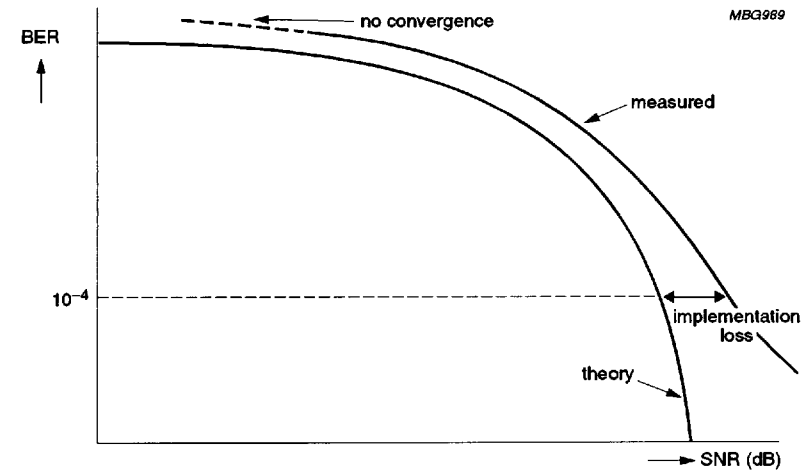


Fig.27 Implementation loss.

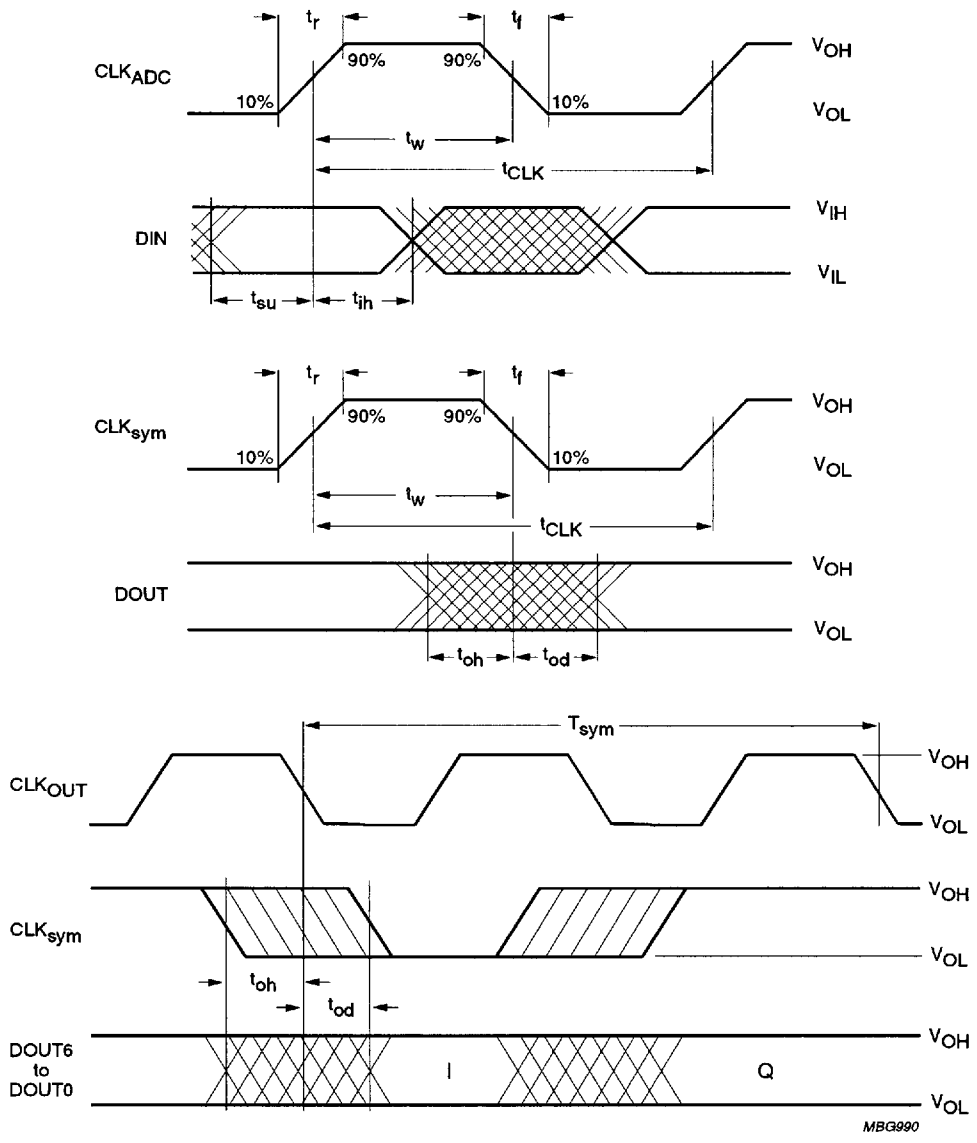
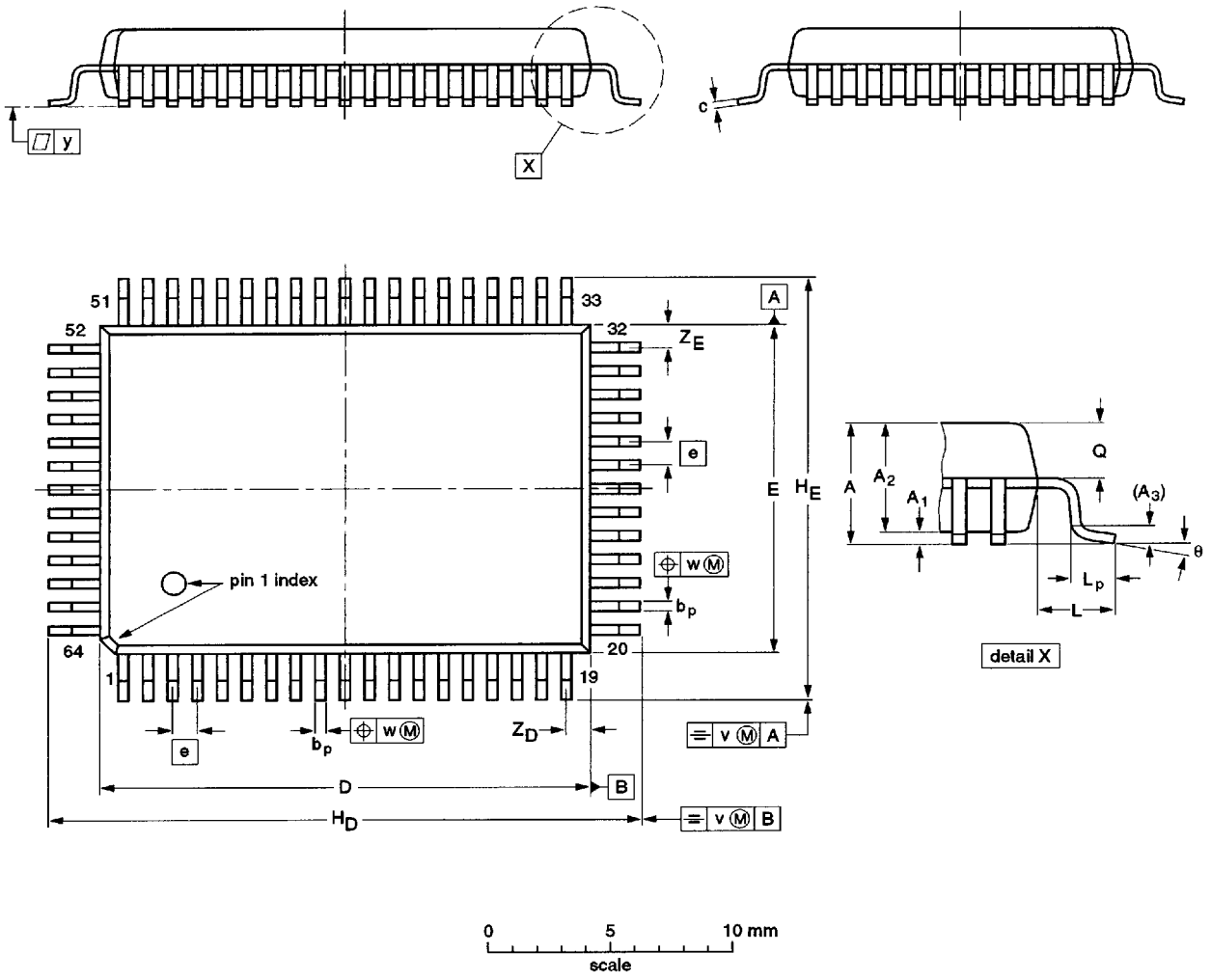


Fig.28 CMOS input and output general interface definition.

PACKAGE OUTLINES

QFP64: plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT319-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.50 0.35	0.25 0.14	20.1 19.9	14.1 13.9	1	24.2 23.6	18.2 17.6	1.95	1.0 0.6	1.4 1.2	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-2						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9398 510 63011).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.