PI74FCT322501T
PI74FCT322Q501T

Fast CMOS 36-Bit Registered Transceiver with 3-State Outputs

Product Features

Common Features

- V_{CC} = 5V ±10%
- Hysteresis on all inputs
- Bus Hold retains last active bus state during 3-state
- Internal resistors eliminates the need for external pullup resistors
- Packages available:
  – 100-pin TQFP (F100)

PI74FCT322501T Features

- Balanced output drivers: ±24mA

PI74FCT322Q501T Features

- Balanced output drivers: ±12mA
- Output impedance 35Ω (typical)

Truth Table[1,4]

Inputs				Outputs
xOEAB	xLEAB	xCLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B[2]
H	L	L	X	B[3]

Notes:

1. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{\text{xOEBA}}$, xLEBA, and xCLKBA.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that xCLKAB was LOW before xLEAB went LOW.
4. H = High Voltage Level
   L = Low Voltage Level
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

Product Description

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT322501T and PI74FCT322Q501T are 36-bit registered bus transceivers designed with D-type latches and flip-flops to allow data flow in transparent, latched, and clocked modes. The Output Enable (xOEAB and $\overline{\text{xOEBA}}$), Latch Enable (xLEAB and xLEBA) and Clock (xCLKAB and xCLKBA) inputs control the data flow in each direction.

When xLEAB is HIGH, the device operates in transparent mode for A-to-B data flow. When xLEAB is LOW, the A data is latched if xCLKAB is held at a HIGH or LOW logic level. When xLEAB is LOW, the A bus data is stored in the latch/flip-flop on the transition of xCLKAB. Data flow from B port to A port is similar to that of A port to B port but uses $\overline{\text{xOEBA}}$, xLEBA and xCLKBA.

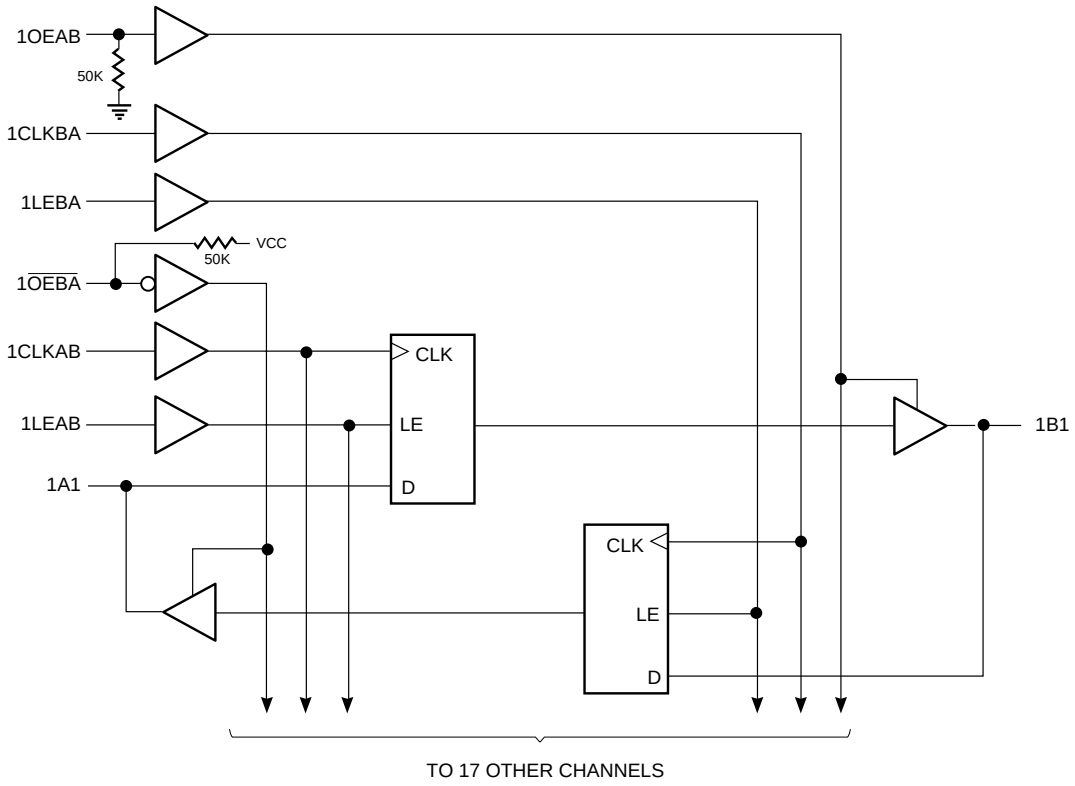
Internal 50KΩ pullup and pulldown resistors are provided for the two Output Enable inputs. xOEAB should be tied to GND through a pulldown resistor. Its minimum value is determined by the current-sourcing capability of the driver. The Output Enables are complementary (xOEAB is active HIGH and $\overline{\text{xOEBA}}$ is active LOW).

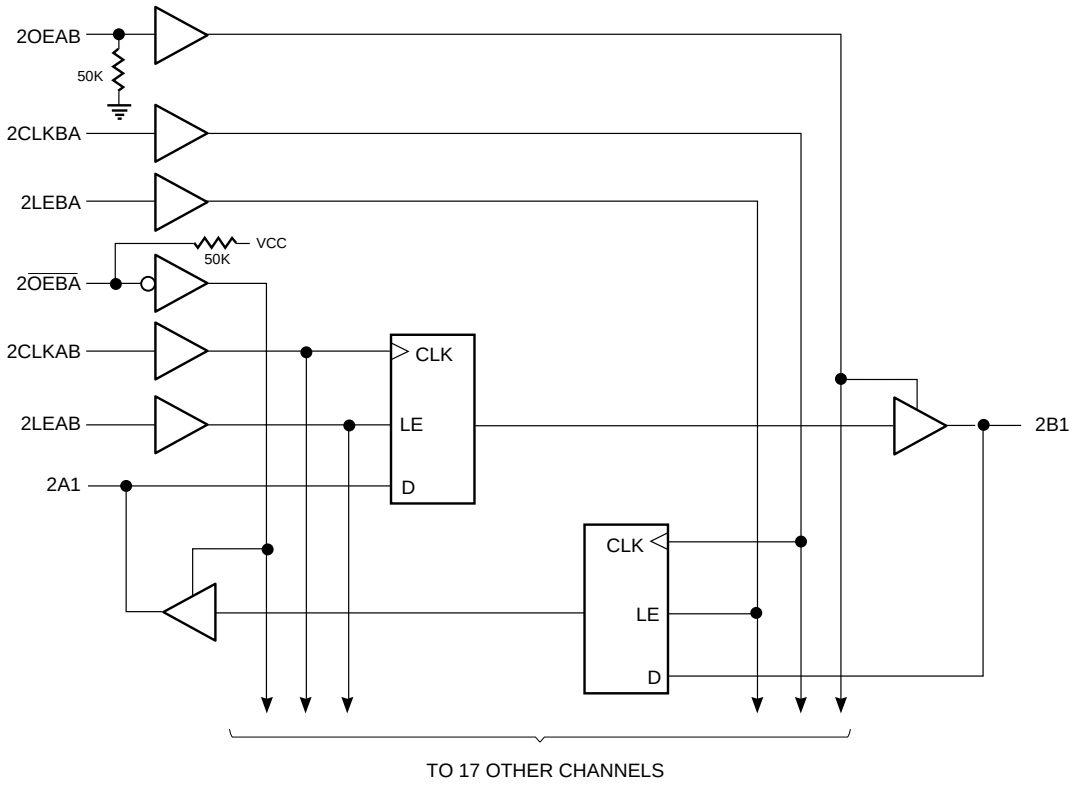
The PI74FCT322501T and PI74FCT322Q501T have "Bus Hold" which retains the input's last state whenever the input goes to high-impedance preventing "floating" inputs and eliminating the need for pullup/down resistors.

The PI74FCT322501T and PI74FCT322Q501T are designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot.

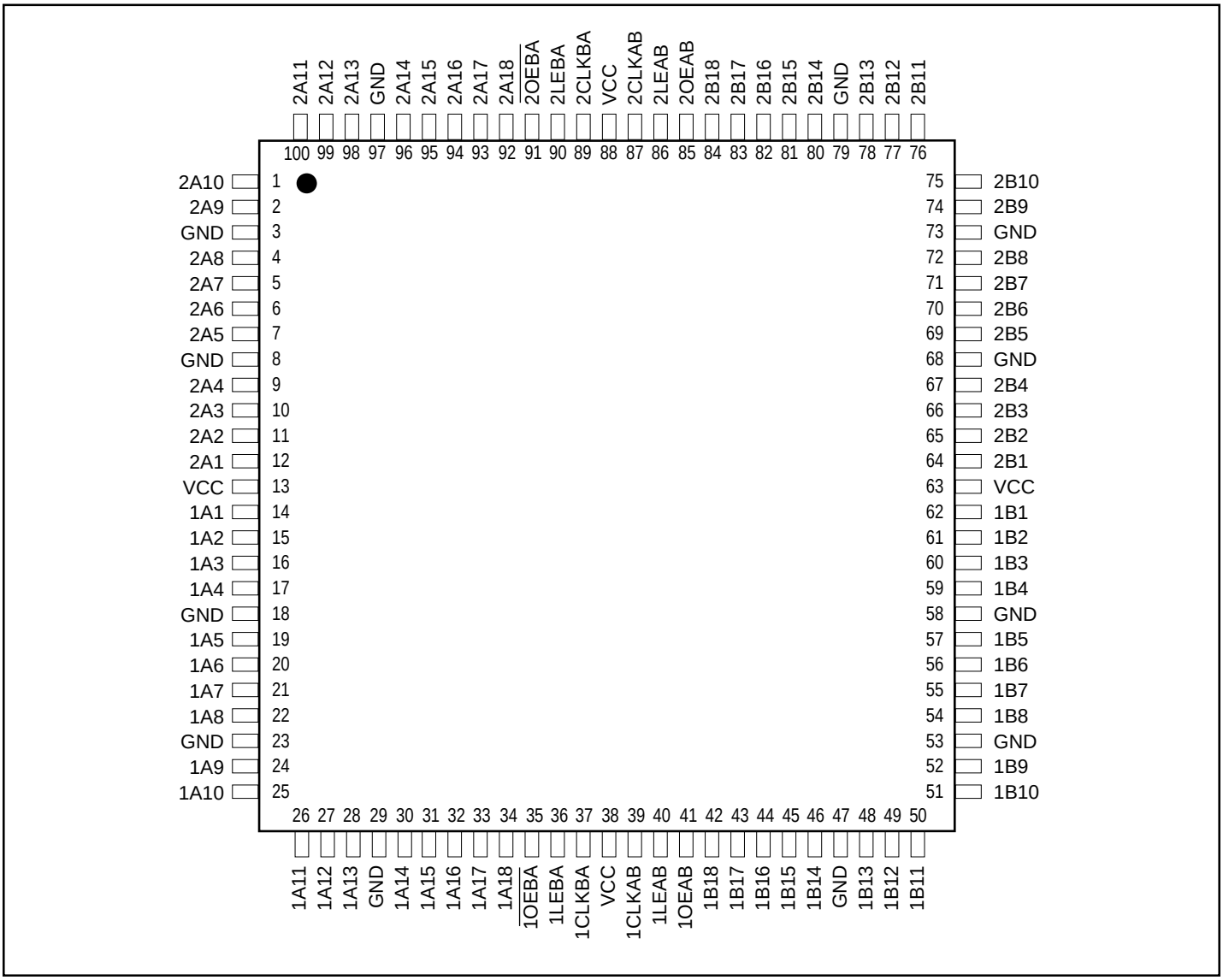
The PI74FCT322Q501T also features an additional internal series resistor which further minimizes noise. This virtually eliminates the need for any external terminating resistors for most low noise bus interface applications. This noise suppression benefit is designated by the letter "Q" (for quiet) in the part number.

Logic Block Diagram





Product Pin Configuration



Product Pin Description

Pin Name	Description
xOEAB	A-to-B Output Enable Inputs (Active HIGH)
x$\overline{\text{OEBA}}$	B-to-A Output Enable Inputs (Active LOW)
xLEAB	A-to-B Latch Enable Inputs
xLEBA	B-to-A Latch Enable Inputs
xCLKAB	A-to-B Clock Inputs
xCLKBA	B-to-A Clock Inputs
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs
GND	Ground
V_{CC}	Power

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–55°C to +125°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.2W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	Standard Input, V_{CC} = Max.	V_{IN} = V_{CC}			1	µA
I_{IH}	Input HIGH Current	Standard I/O, V_{CC} = Max.	V_{IN} = V_{CC}			1	µA
I_{IH}	Input HIGH Current	Bus Hold Input[4], V_{CC} = Max.	V_{IN} = V_{CC}			±100	µA
I_{IH}	Input HIGH Current	Bus Hold I/O[4], V_{CC} = Max.	V_{IN} = V_{CC}			±100	µA
I_{IL}	Input LOW Current	Standard Input, V_{CC} = Min.	V_{IN} = GND			–1	µA
I_{IL}	Input LOW Current	Standard I/O, V_{CC} = Min.	V_{IN} = GND			–1	µA
I_{IL}	Input LOW Current	Bus Hold Input[4], V_{CC} = Min.	V_{IN} = GND			±100	µA
I_{IL}	Input LOW Current	Bus Hold I/O[4], V_{CC} = Min.	V_{IN} = GND			±100	µA
I_{BHH}	Bus Hold	Bus Hold Input[4], V_{CC} = Min.	V_{IN} = 2.0V	–50			µA
I_{BHL}	Sustain Current		V_{IN} = 0.8V	+50			
I_{BHHO}	Bus Hold	Bus Hold Input[4], V_{CC} = Max.	V_{IN} = 1.5V			TBD	mA
I_{BHLO}	Overdrive Current						
I_{OZH}	High-Impedance	V_{CC} = Max.	V_{OUT} = 2.7V			1	µA
I_{OZL}	Output Current (3-State Outputs)	V_{CC} = Max.	V_{OUT} = 0.5V			–1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max.[3], V_{OUT} = 2.5V		–50		–180	mA
V_H	Input Hysteresis				100		mV

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Pins with Bus Hold are identified in the pin description.

PI74FCT322501T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –24.0 mA	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA	—	0.3	0.55	V
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–150	mA

PI74FCT322Q501T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12.0 mA	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA	—	0.3	0.55	V
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		—	TBD	—	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		—	TBD	—	mA

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8	pF

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.2	20	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.4V[3]		1.0	6.0	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open OEAB = $\overline{OEBA}$ = V_{CC} or GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		150	240	µA/ MHz

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

PI74FCT322501/322Q501T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	322501/Q501AT Com. Min	322501/Q501AT Com. Max	322501/Q501CT Com. Min	322501/Q501CT Com. Max	322501/Q501DT Com. Min	322501/Q501DT Com. Max	322501/Q501ET Com. Min	322501/Q501ET Com. Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Ax to Bx or Ax to Bx	C_L = 50 pF R_L = 500Ω	1.5	5.1	1.5	4.6	1.5	4.1	1.5	3.8	ns
t_{PLH} t_{PHL}	Propagation Delay xLEBA to Ax, xLEAB to Bx		1.5	5.6	1.5	5.3	1.5	4.6	1.5	4.2	ns
t_{PLH} t_{PHL}	Propagation Delay xCLKBA to Ax, CLKAB to Bx		1.5	5.6	1.5	5.3	1.5	4.6	1.5	4.2	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OEBA}$ to Ax, xOEAB to Bx		1.5	6.0	1.5	5.6	1.5	5.2	1.5	4.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] x$\overline{OEBA}$ to Ax, xOEAB to Bx		1.5	5.6	1.5	5.2	1.5	5.2	1.5	5.2	ns
t_{SU}	Setup Time HIGH or LOW Ax to xCLKAB, Bx to xCLKBA		3.0	—	3.0	—	3.0	—	2.4	—	ns
t_H	Hold Time HIGH or LOW Ax to xCLKAB, Bx to xCLKBA		0	—	0	—	0	—	0	—	ns
t_{SU}	Setup Time HIGH or LOW Ax to xLEAB, Bx to xLEBA — Clock HIGH		3.0	—	3.0	—	3.0	—	2.0	—	ns
	Setup Time HIGH or LOW Ax to xLEAB, Bx to xLEBA — Clock LOW		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_H	Hold Time HIGH or LOW Ax to xLEAB, Bx to xLEBA		1.5	—	1.5	—	1.5	—	0.5	—	ns
t_W	xLEAB or xLEBA Pulse Width HIGH[3]		3.0	—	3.0	—	3.0	—	3.0	—	ns
t_W	xCLKAB or xCLKBA Pulse Width HIGH or LOW[3]		3.0	—	3.0	—	3.0	—	3.0	—	ns
$t_{SK(O)}$	Output Skew[4]		—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.