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CMOS 300 MHz Complete-DDS Synthesizer

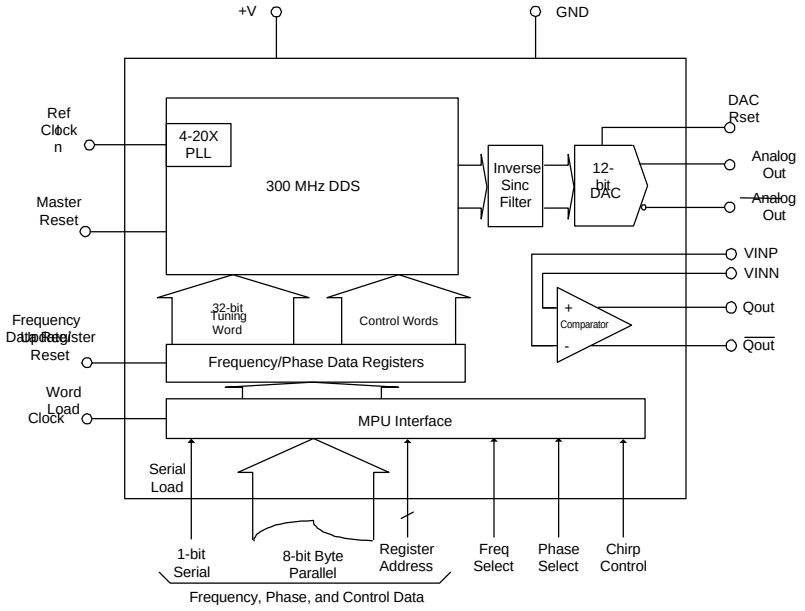
PRODUCT CONCEPT ADI Proprietary and Confidential **AD9852**

FEATURES

300 MHz Internal Clock Rate
On-chip 12-bit DAC
& High-speed Comparator
Excellent Dynamic Performance:
84 dB SFDR @ 100 MHz (±1 MHz) Aout
4-20X PLL Reference Clock Multiplier
32-bit Frequency/14-bit Phase Tuning Words
Two Programmable Frequency/Phase Registers
FM Chirp Function
SIN X/X Correction
Simplified Control Interface: Serial & Parallel
+3 V Single Supply
Low Power: 500 mW @ 300 MHz
Power-down Function
Ultra-Small 44-pin TQFP Packaging

APPLICATIONS

Agile L.O. Frequency Synthesis in Amateur Radio Tuners
Cellular/DCS/GSM Basestation
Programmable Clock Generator
FM Chirp Source for Acousto-optic Laser Scanning System



AD9852 FUNCTIONAL BLOCK DIAGRAM

GENERAL DESCRIPTION

The AD9852 digital synthesizer is a highly integrated device that uses advanced DDS technology, coupled with an internal high-speed, high performance D/A converter and comparator to form a digitally-programmable synthesizer function.When referenced to an accurate clock source, the AD9852 generates a highly stable, frequency/phase-programmable output sinewave that can be used as an agile L.O. in communications, radar, and many other applications. The AD9852's innovative high-speed DDS core provides a 32-bit frequency tuning word, which results in an output tuning resolution of .07 Hz, for a 300 MHz internal reference clock input. The AD9852's circuit architecture allows the generation of an output sinewave at up to one-third the clock frequency, or 100 MHz, which can be digitally changed up to a rate of 25 million new frequencies per second. The device also provides 14-bits of digitally-controlled phase modulation. The on-board 12-bit DAC, coupled with the innovative DDS architecture, provides excellent output wideband and narrowband SFDR. The AD9852's programmable 4-20X reference clock PLL generates the 300 MHz clock internally, from an external reference clock. This saves the user the expense and difficulty of implementing a 300 MHz clock source. The AD9850 uses advanced CMOS technology to provide this high level of functionality on <500 mW of power dissipation, at a maximum internal clock rate of 300 MHz.

The AD9852 is available in a space-saving 44-pin TQFP surface mount package. It is specified to operate over the extended industrial temperature range of -40° to +85°C.

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AD9852 PRODUCT CONCEPT

ABSOLUTE MAXIMUM RATINGS[1]

Maximum Junction Temp. .....+165°C
Vs ..... +6V
Digital Inputs ..... -0.7V to +Vs
Digital Output Current 5mA
Storage Temperature ..... -65°C to +150°C
Operating Temp. ..... -40°C to +85°C
Lead Temp. (10 sec. soldering) ..... +300°C

AD9852 GOAL ELECTRICAL SPECIFICATIONS (Vs=+3 V ±5%, Rset=3.9 kΩ)

Parameter	Temp	Test Level	AD9852 Min	AD9852 Typ	AD9852 Max	Units
CLOCK INPUT CHARACTERISTICS[2]						
Internal clock Frequency Range	FULL	VI	10		300	MHz
Duty Cycle	+25°C	I		50		%
Input Capacitance	+25°C	IV		3		pF
Input Impedance	+25°C	IV		100		MΩ
DAC OUTPUT CHARACTERISTICS						
Full Scale Output Current	+25°C	V			10	mA
Gain error	+25°C	I		TBD		%FS
Output Offset	+25°C	I		TBD		uA
Differential Non-linearity	+25°C	I		.5		lsb
Integral Non-linearity	+25°C	I		1		lsb
Output Slew Rate	+25°C	IV		TBD		V/nS
Output Impedance	+25°C	I		100		kΩ
Voltage Compliance Range	+25°C	I			1	V
Wideband SFDR:						
1 MHz Aout	+25°C	V		75		dBC
20 MHz Aout	+25°C	V		65		dBC
40 MHz Aout	+25°C	V		62		dBC
100 MHz Aout	+25°C	V		50		dBC
Narrowband SFDR[3]:						
100 MHz Aout (± 15 MHz)	+25°C	V		75		dBC
100 MHz Aout (± 1 MHz)	+25°C	V		84		dBC
100 MHz Aout (± 50 kHz)	+25°C	V		90		dBC
COMPARATOR INPUT CHARACTERISTICS						
Input Capacitance	+25°C	V		3		pF
Input Resistance	+25°C	IV		500		kΩ
Input Bias Current	+25°C	I		±12		nA
Input Voltage Range	+25°C	IV	0		V_{DD}	V
COMPARATOR OUTPUT CHARACTERISITICS						
Logic "1" voltage	FULL	VI	+4.95			V
Logic "0" voltage	FULL	VI			+0.4	V
Propagation Delay	+25°C	IV,		7		ns
CLOCK OUTPUT AC CHARACTERISTICS[4]						
Clock Output Duty Cycle	FULL	VI		50		%
Rise/Fall Time	+25°C	IV		1		ns
Output Jitter (RMS)	+25°C	IV			20	ps
CMOS LOGIC INPUTS						
Logic "1" Voltage	+25°C	I	2.7			V
Logic "0" Voltage	+25°C	I			0.4	V
Logic "1" Current	+25°C	IV			12	uA
Logic "0" Current	+25°C	IV			12	uA
Input Capacitance	+25°C	V		3		pF

AD9852 PRODUCT CONCEPT

AD9852 GOAL ELECTRICAL SPECIFICATIONS (Vs=+3 V ±5 %, Rset=3.9 kΩ)

Parameter	Temp	Test Level	AD9852 Min	AD9852 Typ	AD9852 Max	Units
POWER SUPPLY						
+Vs Current @:						
50 MHz External Clock (PLL enabled)	+25°C	I		166		mA
$P_{DISS@:}$						
50 MHz External Clock	+25°C	I		500		mW
P_{DISS} Power-down Mode	+25°C	I		10		mW

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

[2]The reference clock input is configured to accept a sine wave input or a TTL-level pulse input.

[3]Reference clock frequency is selected to insure second harmonic is out of the bandwidth of interest.

[4]Reference clock input=50 MHz; output frequency=40MHz; external filter=5-pole low-pass.

EXPLANATION OF TEST LEVELS

Test Level

I - 100% Production Tested.

III - Sample Tested Only.

IV - Parameter is guaranteed by design and characterization testing.

V - Parameter is a typical value only.

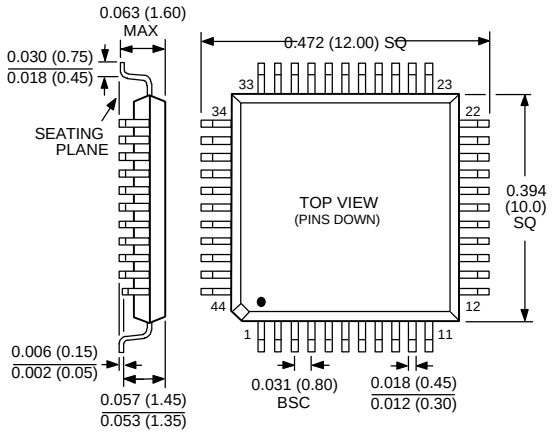
VI - All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for military temperature devices; guaranteed by design and characterization testing for industrial devices.

Table I. AD9852 PIN-FUNCTION DESCRIPTIONS

CLKIN	Reference clock input. This may be a sine input or continuous TTL/CMOS-level pulse train.
Rset	This is the DAC's external Rset connection. This resistor value sets the DAC fullscale output current.
AGND	Analog Ground. These pins are the ground return for the analog circuitry (DAC and comparator).
VDD	Supply voltage pins for digital circuitry.
AVCC	Supply voltage for the analog circuitry (DAC and comparator).
W_CLK	Word load clock. This clock is used to load each of the (up to) five iterations of the 8-bit
FQ_UD	Frequency Update. When this pin is set high, the DDS will update to the frequency
D0-D7	8-bit Data Input. This is the 8-bit data port for iteratively loading the 32-bit
RESET	Reset. This is the master reset pin; when set high it clears all registers and the DAC
IOUT	The true output of the differential DAC.
IOUTB	The complementary output of the differential DAC.
DACBL	DAC Baseline. This is the DAC baseline reference; it should normally be left as a no connect.
VINP	Voltage input positive. This is the comparator's positive input pin.
VINN	Voltage input negative. This is the comparator's negative input pin.
QOUTB	Output complement. This is the comparator's complementary output pin.
QOUT	Ouput true. This is the comparator's positive output pin.
FSELECT	Frequency select input. Controls which frequency register, F0 or F1, is added to the phase accumulator
PSELECT	Phase select input. Controls which phase register, P0 or P1, is added to the phase accumulator
A0-A2	Address bits. These address bits are used to select the destination register for freq/phase/control input data

AD9852 PRODUCT CONCEPT

Mechanical Outline
44-Lead Thin-Quad Flatpack IC Package (TQFP)



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