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Am186™CC Microcontroller ISDN TA Reference Design

User's Manual

Order #22033B

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Am186™CC Microcontroller ISDN TA Reference Design User's Manual

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About the Am186™CC Microcontroller ISDN TA Reference Design

The Am186CC microcontroller ISDN terminal adapter (TA) reference design is a small, cost-effective ISDN solution for embedded communications applications. This design is intended to reduce the time to market for ISDN designers using the Am186CC microcontroller. Figure 0-1 shows a block diagram of the ISDN TA reference design.

The ISDN TA reference design is a functional ISDN TA that illustrates the benefits of using the Am186CC microcontroller. The Am186CC microcontroller has a number of integrated features required in many communication applications. These features include four high-level data link control (HDLC) channels and a universal serial bus (USB) peripheral controller with an internal transceiver. The HDLC channels support GCI/IOM-2, PCM, and DCE interfaces. Other integrated features include four general-purpose DMA channels, eight SmartDMA™ channels, four time-slot assigners (TSAs), one UART, one High-Speed UART with autobaud, and an integrated DRAM controller.

The ISDN TA reference design illustrates how to use many of the integrated peripherals to provide a small, low-cost ISDN TA. The reference design supports either an ISDN 2B+D U or S/T network interface by a component population option. You can interface to a PC using either the High-Speed UART connection at up to 230 Kbit/s, or by using a full-speed USB connection at 12 Mbit/s.

Note that the ISDN data rate is 128 Kbit/s, so the reference design's UART transceiver is only 230 Kbit/s. This limits the High-Speed UART, which is actually capable of 460 Kbit/s. The PCs that the ISDN TA would connect are also a limiting factor because most are only capable of speeds up to 115 Kbit/s or 230 Kbit/s.

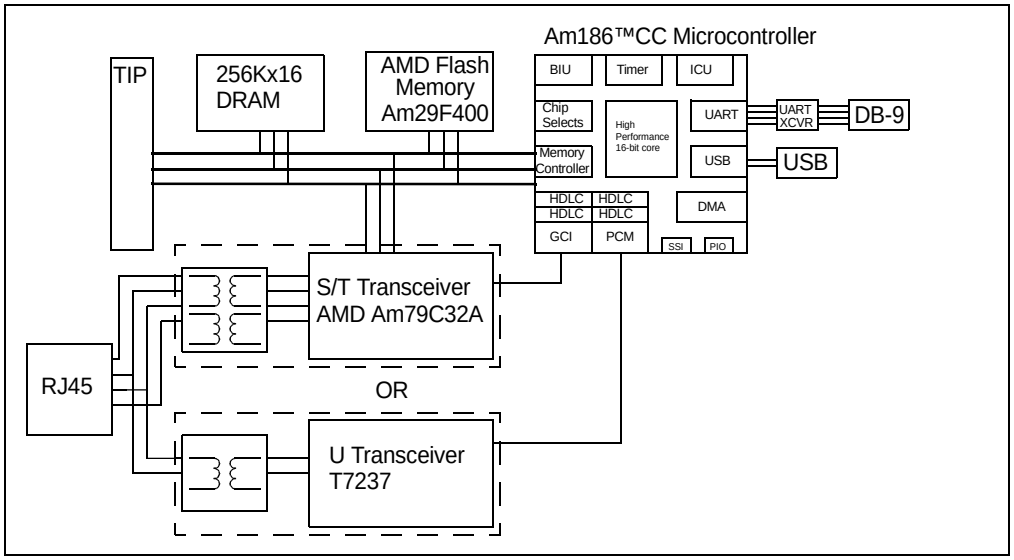

Figure 0-1. ISDN TA Reference Design Block Diagram

Theory of Operation

The ISDN TA reference design demonstrates the processor's functionality in an ISDN application. You can use this design as a reference to create your own ISDN designs. The small size and simplicity of this design highlight the benefits of the Am186CC microcontroller's many integrated peripherals.

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Features

The ISDN TA reference design provides the following features:

- 2B+D ISDN network interface (for more information about ISDN, see “ISDN Background” on page xii)
  - ISDN U interface available by population option
  - ISDN S/T interface available by population option
- High-Speed, 230-Kbit/s, serial PC interface
- 12-Mbit/s, USB PC interface
- Single, +5V AC/DC wall-adapter power supply
- Very small form factor
- Four-layer printed circuit board (two signal: V_{CC}, GND)

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ISDN Background

ISDN (integrated services digital network) is an alternative to analog phone lines. ISDN provides greater performance than analog and is still affordable to consumers. There are many different variations of ISDN available, but the most common variation is 128-Kbit/s data transfer rate over two B (bearer) channels, plus 16 Kbit/s of signaling data over the D channel; this is the 2B+D configuration, the configuration used by the ISDN TA reference design discussed in this manual. Another configuration uses a single B channel and transfers data at 64 Kbit/s. Broadband ISDN is available and can achieve data rates in the 100-Mbit/s range.

There are a number of reference points in an ISDN system. Figure 0-2 shows a graphical representation of the ISDN reference points. For more information about Figure 0-2, refer to *Digital Telephony, Second Edition*, ISBN 0-471-62056-4.

The U reference point is the local loop between the LE (local exchange) and the NT (network termination) device. The U interface is a two-wire interface, which in North America and Asia is typically supplied by a telecommunications service provider. The U interface operates in 2B1Q (two binary, one quaternary) format, and can travel for miles without repeaters. The T reference point is used only with customer premises switching equipment (NT2). The S/T reference point is the four-wire interface between the network termination device (NT1) and the terminal equipment (TE1) or terminal adapter (TA). The S/T interface is offered in Europe, and is also used with stand-alone NT1 devices.

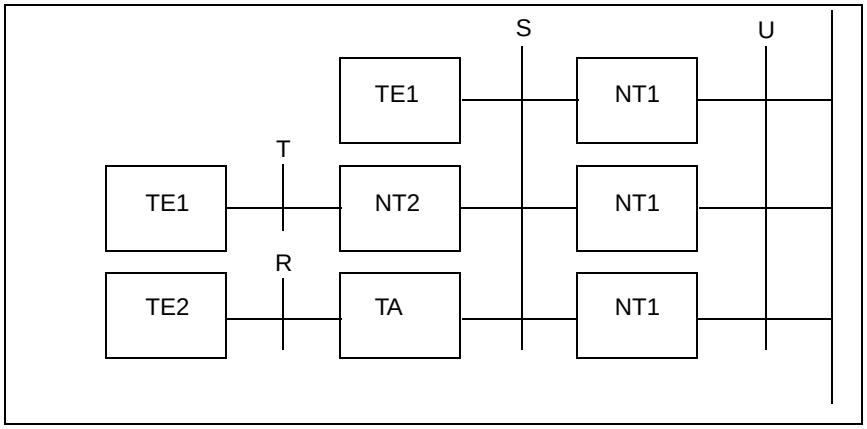

Figure 0-2. ISDN Reference Point Diagram

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Documentation

The *Am186™CC Microcontroller ISDN TA Reference Design User's Manual* provides information on the system and board features, functionality, and ISDN interfaces. Additional information can be found in the documentation listed on page xiv.

About This Manual

Chapter 1, "Quick Start" provides installation information for the ISDN TA reference design.

Chapter 2, "System Features and Components" contains descriptions of the reference design features and components, ISDN interfaces, power supply, test interface port, and ISDN TA pin usage.

Appendix A, "Bill of Materials (BOM)" shows the bill of materials for the reference design.

Appendix B, "Glossary" contains definitions of terms used in this manual.

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Suggested Reference Material

The following AMD documentation may be of interest to you:

- *Am186™CC/CH/CU Microcontrollers User's Manual*
  Advanced Micro Devices, order #21914
- *Am186™CC Communications Controller Data Sheet*
  Advanced Micro Devices, order #21915
- *Am186™CC/CH/CU Microcontrollers Register Set Manual*
  Advanced Micro Devices, order #21916
- *Am186™ and Am188™ Family Instruction Set Manual*
  Advanced Micro Devices, order #21076
- *E86™ Family Products and Development Tools CD*
  Advanced Micro Devices, order #21508
- *AMD Test Interface Port Board User's Manual*
  Advanced Micro Devices, order #22505

For current application notes and technical bulletins, see our World Wide Web page at **www.amd.com**.

The following non-AMD documentation may also be of interest to you:

- *ISDN Concepts, Facilities, and Services*
  Gary C. Kessler, ISBN: 0-07-034242-3
- *ISDN For Dummies®, 2nd Edition*
  David Angell, ISBN: 0-7645-0064-3
- *ISDN Implementor's Guide: Standards, Protocols, Services*
  Charles K. Summers, ISBN: 0-07-069416-8
- *Digital Telephony, Second Edition*
  John Bellamy, ISBN: 0-471-62056-4
- Lucent T7237 device data sheet at www.lucent.com
- International Telecommunication Union Standards at www.itu.ch

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Chapter 1

Quick Start

This chapter provides information that helps you quickly set up and install the ISDN TA reference design.

- For information on how to connect the ISDN TA reference design to a PC (high-speed serial connection or full-speed USB connection), see page 1-2.
- For information on how to locate other sources of information, see page 1-3.
- For information on invoking the software supported by the reference design, refer to the Software Quick Start information included in your kit.

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Connecting to a PC

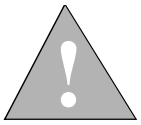
The procedure in this section describes how to connect the ISDN TA reference design to a PC using either a USB or serial port. Follow the steps below to connect the ISDN TA reference design to your PC. For information on how to invoke the software, see the Software Quick Start document included in your kit.

Installation Requirements

The items listed below are necessary to install and run the ISDN TA:

- PC with an available COM port
- Terminal emulation software (such as Microsoft®Windows® Terminal or ProComm Plus) that supports ASCII file transfers, software flow control (Xon/Xoff), and send break capability
- Dial-up networking configured per your ISP's recommendations
- Power source for universal power supply (47–63 Hz, 100–250 VAC)

Board Installation



CAUTION: As with all computer equipment, the ISDN TA may be damaged by electrostatic discharge (ESD). Please take proper ESD precautions when handling any board.

1. Remove the board from the shipping carton. Visually inspect the board to verify that it was not damaged during shipment.
2. Connect the ISDN TA board's DB-9 serial port to an available COM port. Use the serial cable included in the ISDN TA kit and note that a DB-9 to DB-25 serial connector adapter is provided if your host system requires it. If using your own cable, use a straight through cable, *not* a null modem cable.
3. Plug the AC adapter into a power source. Connect the 5 V_{DC} from the AC adapter to the ISDN TA through the barrel connector.
4. If you are using a USB PC interface, connect the USB cable into the USB Type-B connector on the ISDN TA.

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5. When all of the power and PC connections have been made, apply power by toggling the switch located at the back of the ISDN TA. The power LED (PWR LED) turns on when power is correctly applied.

For More Information...

If you need more information about:

- The ISDN TA reference design hardware, see Chapter 2.
- Problems with the reference design, see page iii.
- The ISDN TA reference design board layout, see Chapter 2.
- The ISDN TA reference design schematics, see the schematics document included in your kit.
- The Am186CC microcontroller, see the *Am186™CC Communications Controller Data Sheet* and the *Am186™CC/CH/CU Microcontroller User's Manual* included in your kit.
- The latest release and updates, see Demo Board Updates at www.amd.com.

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Chapter 2

System Features and Components

The ISDN TA reference design provides a small, low-cost, stand-alone system for use by ISDN developers using the Am186CC microcontroller.

The following sections explain the operation of the board in detail:

- "Layout and Placement" on page 2-2
- "Am186CC Microcontroller" on page 2-5
- "System Memory" on page 2-7
- "ISDN S/T Interface" on page 2-8
- "ISDN U Interface" on page 2-9
- "Serial PC Interface" on page 2-10
- "USB PC Interface" on page 2-11
- "Power Supply" on page 2-12
- "Test Interface Port (TIP)" on page 2-14
- "ISDN TA Pin Usage" on page 2-17
- "RESCON Configuration" on page 2-19

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Layout and Placement

The ISDN TA reference design emphasizes the small board size that can be obtained by using the Am186CC microcontroller in an embedded communications application. Refer to Figure 2-1 on page 2-4 for layout and component placement.

The ISDN TA reference design has the Flash memory, DRAM, and TIP connector located close to the processor to provide a linear, logical signal flow for the address and data bus. The connectors and the power switch are located at the back of the board, and the status indicator LEDs are located at the front of the board. This placement makes it possible to manufacture the board in a small enclosure. The ISDN interface devices are overlapped where possible to minimize board size. In Table 2-1, all of the parts are identified by part number and part description.

The ISDN TA reference design was designed to fit in a very small desktop enclosure. The circuit board is 3.85" x 4.75", and fits into a variety of enclosures. There are mounting holes on three corners; the fourth is on the side.

Table 2-1. ISDN TA Reference Design Parts List

Part Number	Part Description	Part Location (shown in Figure 2-1)
U1	Am186CC microcontroller	B-1
U2	EDO DRAM – Mosel Vitelic, 256K x 16	A-2
U3	Flash memory – Am29F400, 256K x 16	A-1
U4	ISDN S/T transceiver – Am79C32A	A-2
U5	ISDN S transformer	B-3
U6	ISDN S choke	C-3
U7	Optocoupler	B-3
U8	ISDN DC termination IC	B-3
U9	ISDN U transceiver – Lucent T7237	A-3
U10	ISDN U transformer	B-3
U13	High-Speed UART transceiver	C-2

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Table 2-1. ISDN TA Reference Design Parts List (Continued)

Part Number	Part Description	Part Location (shown in Figure 2-1)
U14	74ACT04	C-1
U15	3.3-V LDO	C-1
CR2–CR8	Status indicator LEDs	A-1–A-3
P1	RJ-45 connector	C-3
P2	DB-9 connector	C-2
P3	USB type-B connector	C-2
P4	Power connector	C-1
P5	TIP connector	B-1
SW1	Power switch	C-1
SW2	Reset button	C-2
JP1	Flash memory CS jumper	A-1
JP2	x8 boot jumper	A-1
F1	ISDN U interface line fuse	C-3
F2	1.5-A power supply main fuse	C-1

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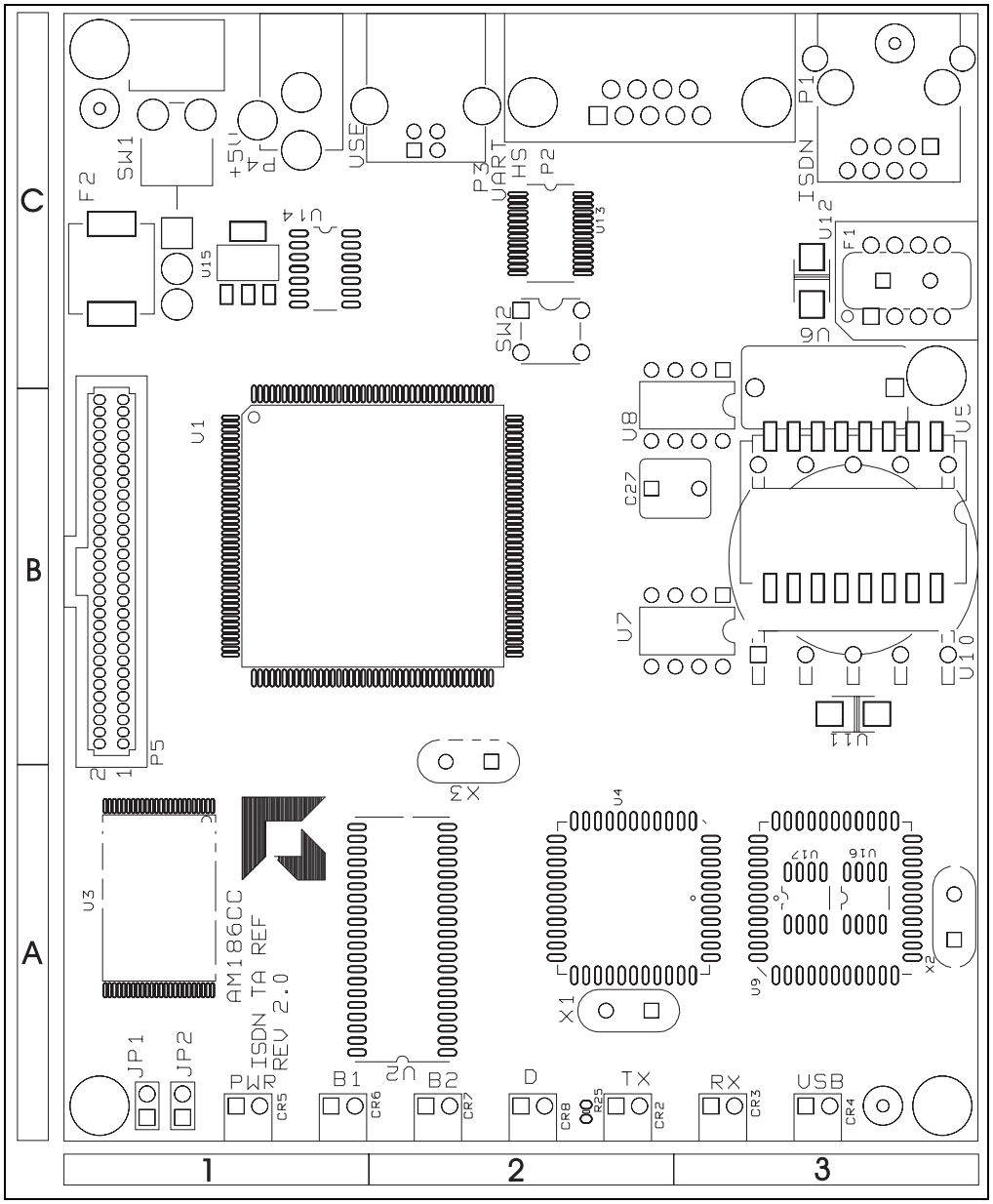

Figure 2-1. ISDN TA Reference Design Circuit Board Layout

Am186™CC Microcontroller

The Am186CC microcontroller is used to control the ISDN TA. A block diagram of the Am186CC microcontroller is shown in Figure 2-2. The many integrated features of the Am186CC microcontroller make it ideal for an ISDN application. The integrated DRAM controller allows a glueless interface to the system memory. You can use the built-in High-Speed UART with autobaud to communicate with the PC. You can also use the full-speed USB peripheral controller with built-in transceiver for a 12-Mbit/s PC interface. The HDLCs provide a glueless interface to either the S/T transceiver or the U transceiver.

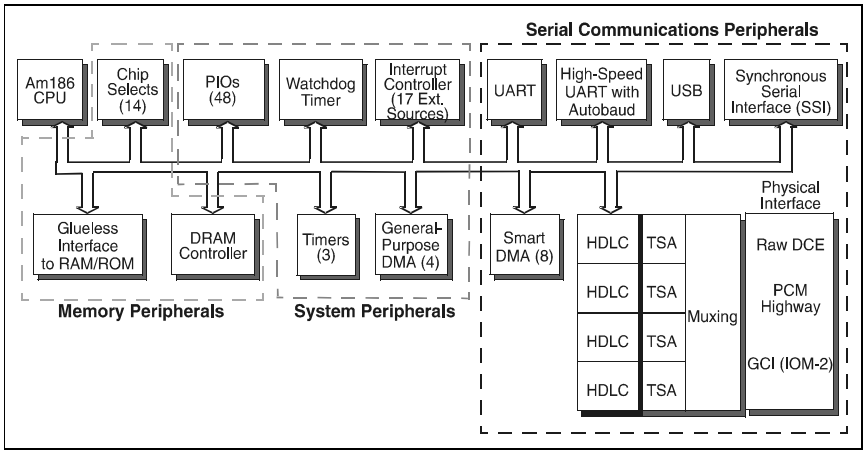

Figure 2-2. Am186™CC Microcontroller Block Diagram

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The system uses a single 24-MHz crystal. This design uses an internal 2x PLL, which provides a 48-MHz system clock and the required 48-MHz USB clock. Because the USB clock is derived from the system PLL, the USB crystal input, USBX1, is terminated. The clock generation circuit is shown in Figure 2-3 and sheet 6 of the schematics included in your kit.

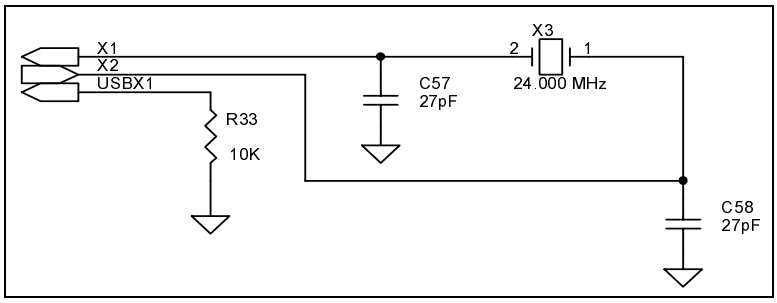

Figure 2-3. ISDN TA Clock Generation Circuit

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System Memory

This design uses 512 kbytes of AMD Flash memory for code space located from 80000h–FFFFFh, and 512 kbytes of DRAM. The memory schematic is shown in Figure 2-4 and sheet 3 of the schematics included in your kit. The Am29F400 Flash memory is used in a 256K x 16 configuration. The Am29F400 is byte/word selectable using the BYTE# pin. In case the 512 Kbytes of Flash memory are not sufficient, PIO35 is routed to the chip to act as a bank select. This allows drop-in compatibility for larger Flash memory, such as the Am29F800 device.

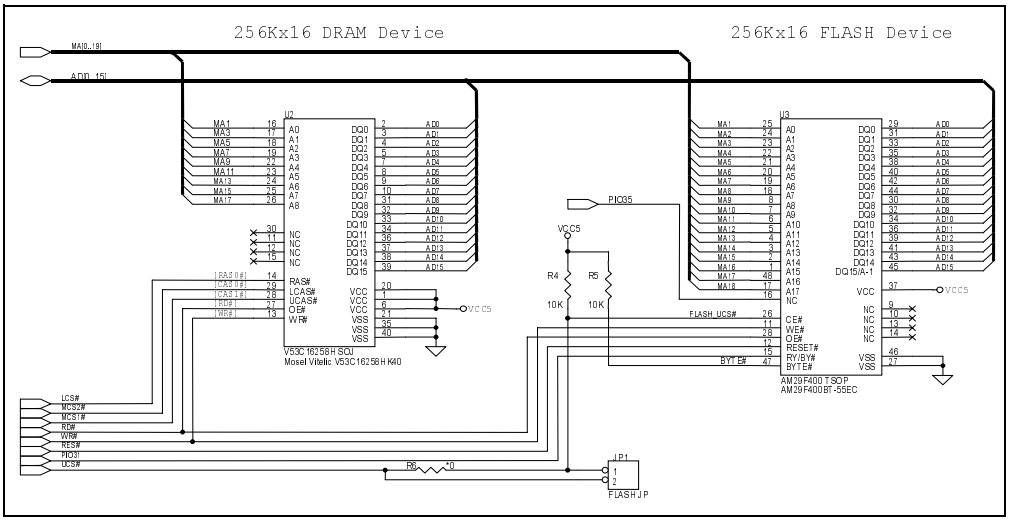

Figure 2-4. ISDN TA System Memory

DRAM was chosen over SRAM as main memory in this application because DRAM is more cost effective than SRAM and because the Am186CC microcontroller has an integrated DRAM controller that makes a glueless DRAM interface simple to use. The Am186CC microcontroller DRAM interface allows zero-wait state operation at 48 MHz using a 40-ns DRAM. This DRAM device is located from 00000h–7FFFFFh in low memory space and is selected using LCS#/ RAS0#.

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ISDN S/T Interface

The Am79C32A ISDN data controller (IDC) circuit is used to provide the four-wire 2B+D S/T interface. This device has a general circuit interface (GCI), also referred to as IOM-2, serial microprocessor interface, which is used to transfer B channel data to and from the Am186CC microcontroller's integrated HDLC controller. The Am186CC microcontroller-based ISDN TA reference design provides a full-duplex path between the terminal equipment (TE) and the network termination (NT) device. The controller processes the ISDN basic rate interface (BRI) bit stream, which consists of two 64-Kbit/s B channels and a single 16-Kbit/s D channel. The schematic for the S/T interface block is shown in Figure 2-5 and sheet 4 of the schematics included in your kit.

The Am79C32A IDC circuit includes a D-channel HDLC controller which is used by software to send and receive data on the D channel.

The four-wire ISDN S/T interface is first directed through an S transformer and line filtering devices. These isolate and protect the modem from the outside lines. The crystal is used to generate MCLK, which can be used as a master clock output and as the system clock for the microprocessor.

The signals SBIN, SBOUT, SCLK, SFS, and BCL/CH2STRB can be configured for serial bus port (SBP) or GCI. SBP is used by the current terminal adapter software and is connected to HDLC Channel A on the Am186CC microcontroller.

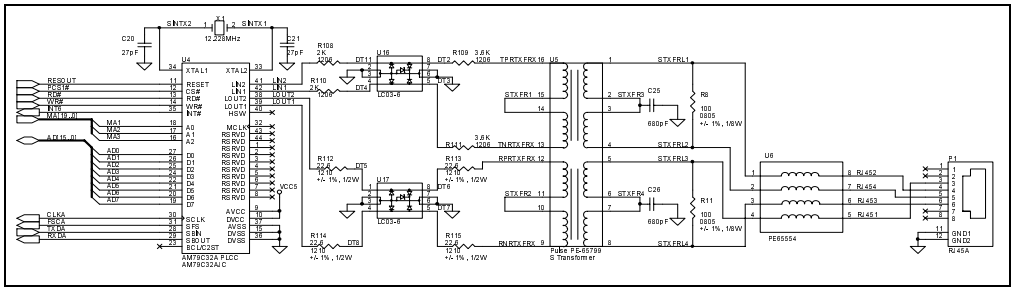

Figure 2-5. ISDN TA S/T Interface

ISDN U Interface

The Lucent T7237 circuit is used to provide the two-wire 2B+D U interface. This device has a PCM serial microprocessor interface and an SSI (synchronous serial interface). These interfaces are used to transfer data to and from the Am186CC microcontroller using its integrated HDLC. This chip provides the two-wire network termination. It processes the ISDN BRI bit stream that consists of two 64-Kbit/s B channels and a single 16-Kbit/s D channel. The schematic for the U interface block is shown in Figure 2-6 and sheet 4 of the schematics included in your kit. The U-interface circuit includes a line fuse, U transformer, DC termination IC, and opto-isolation circuitry. The LED shown in Figure 2-6 is used to indicate device status. The four states of the LED are Low, High, 1 Hz, and 8 Hz. Refer to the Lucent T7237 device data sheet for a complete description.

The U-interface data is in 2B1Q format, which provides a four-level (quaternary) amplitude modulation. A single quaternary symbol represents two binary bits. The quaternary symbols are ± 3, ± 1, which represent 00, 01, 10, and 11 in binary.

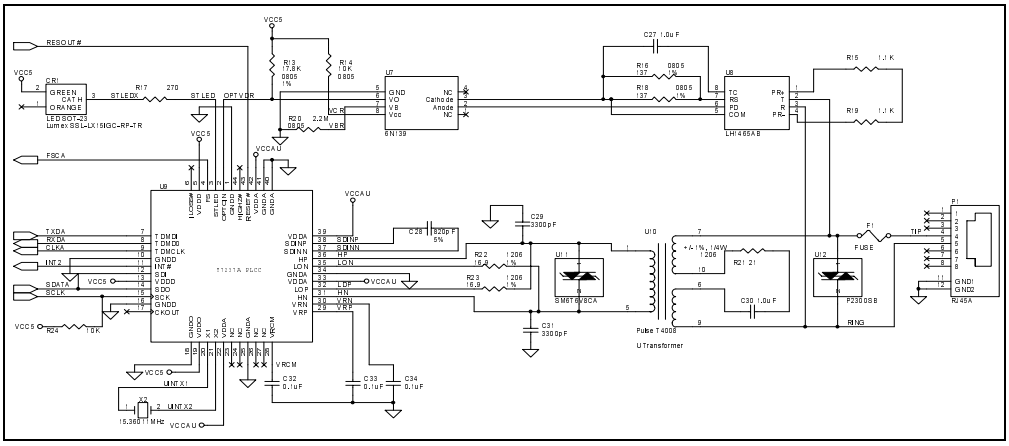

Figure 2-6. ISDN TA U Interface Circuit

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Serial PC Interface

The serial port may be used for communication with a PC. The Sipex high-speed RS-232 transceiver is used to provide serial data rates up to 230 Kbit/s. The DCE serial connection is made through a standard female DB-9, which uses a straight-through serial cable. PIO1 and PIO28 are used to provide extra flow control signaling to support Plug and Play (PnP) operation. The two LEDs are used to indicate transmit and receive activity. The schematic for the serial interface is shown in Figure 2-7 and sheet 5 of the schematics included in your kit.

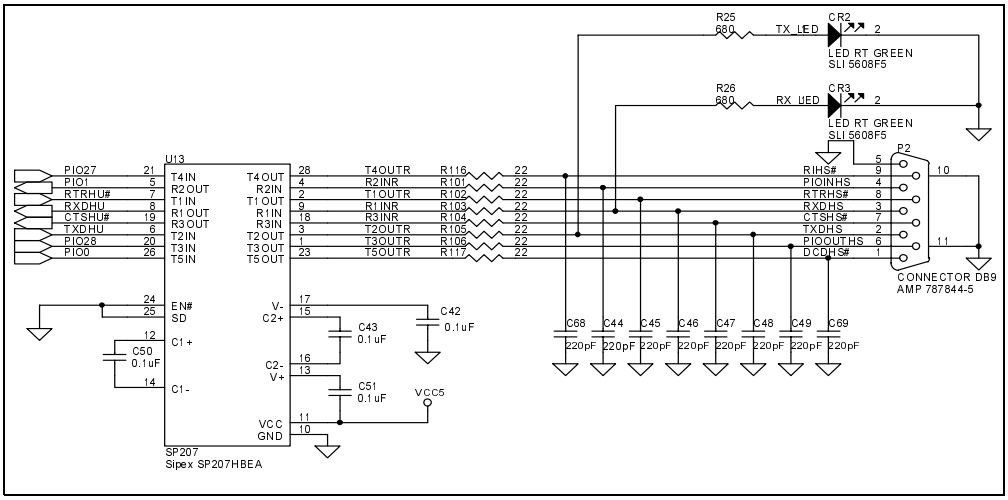

Figure 2-7. ISDN TA High-Speed Serial Interface

USB PC Interface

The ISDN TA reference design has an integrated USB peripheral controller with a built in transceiver; differential USB signals connect directly to the controller without requiring an external transceiver. A USB type-B connector is used for connection to a PC. The N MOSFETs are used with the two PIOs for V_{CC} attach and detach. The attach and detach steps are listed below. The USB interface transfers data at up to 12 Mbit/s. The schematic for the USB interface is shown in Figure 2-8 and sheet 5 of the schematics included in your kit.

Attach

1. Am186CC microcontroller polls USB_Detect (PIO42) for logic High to detect when an active host USB port is connected.
2. Am186CC microcontroller drives USB_V_{CC} (PIO43) High to enable Q1 and pulls up the USBD+ line to indicate to the host that this is a full-speed device.

Detach

1. Am186CC microcontroller polls USB_Detect for logic Low to detect a disconnect of the host.
2. Am186CC microcontroller three-states USBD± in response to a disconnect.
3. Am186CC microcontroller removes USB_V_{CC} to disable Q1; Q2 isolates USB_Detect in response to a disconnect.

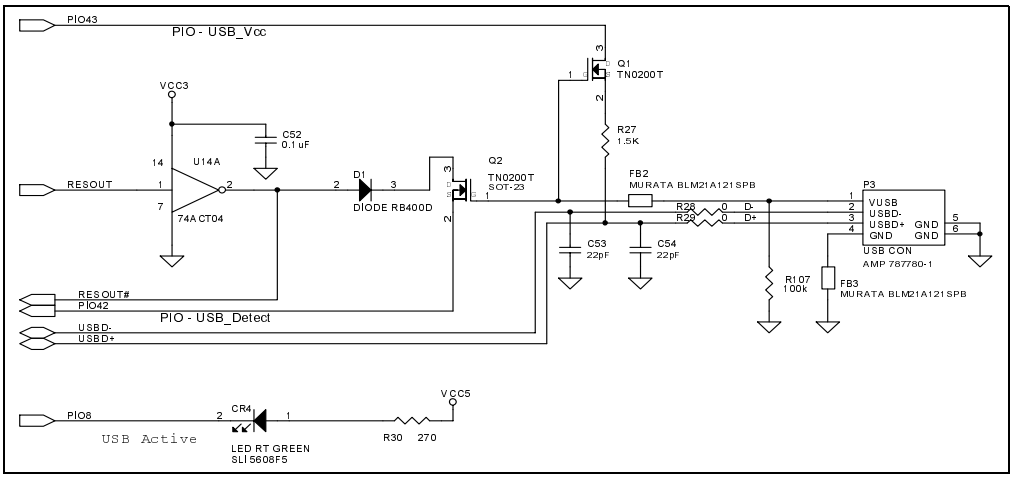

Figure 2-8. ISDN TA USB Interface

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Power Supply

This design requires only two voltages, +5 V and +3.3 V. The associated currents and power estimates are included in Table 2-2. A 5-V, 500-mA, regulated, wall-mount AC adapter is used to supply system power. The AC adapter is connected to the system using a standard 2.5-mm barrel connector. A Raychem 750-mA fuse is used to protect the circuit from a surge in current. To reset the fuse, unplug the board and allow the fuse to cool. Most of the devices on the board require 5 V. The 5 V is used directly from the regulated supply. The Am186CC microcontroller and the inverter chip are the only 3.3-V devices on this board. The 3.3 V is obtained from the LDO (Low Drop Out) linear regulator. The power supply and reset schematics are shown in Figure 2-9 and sheet 6 of the schematics included in your kit.

Table 2-2. Current and Power Estimates for the ISDN TA

Volt (V)	Device	I_{typ}(mA)	I_{max} (mA)	P_{typ} (mW)	P_{max} (mW)
3.3	Am186CC microcontroller	-	288	-	950
5	DRAM	65	99	650	990
5	Flash memory	-	60	-	300
5	UART Xcvr	20	30	100	150
5	ISDN S/T Xcvr	31	38	155	190
5	ISDN U Xcvr	54	70	270	350
3.3	Total	-	288	-	950
5	Total	-	297	-	1980

The reset circuit consists of a push button, a diode, and an RC circuit used to provide a time delay. The reset circuit is shown in Figure 2-9 and sheet 6 of the schematics included in your kit. The $\overline{\text{RES}}$ signal into the Am186CC microcontroller must be held Low for at least 1 ms to allow the internal circuitry to settle. The Am186CC microcontroller begins fetching instructions 6.5 CLKOUT periods after $\overline{\text{RES}}$ is deasserted.

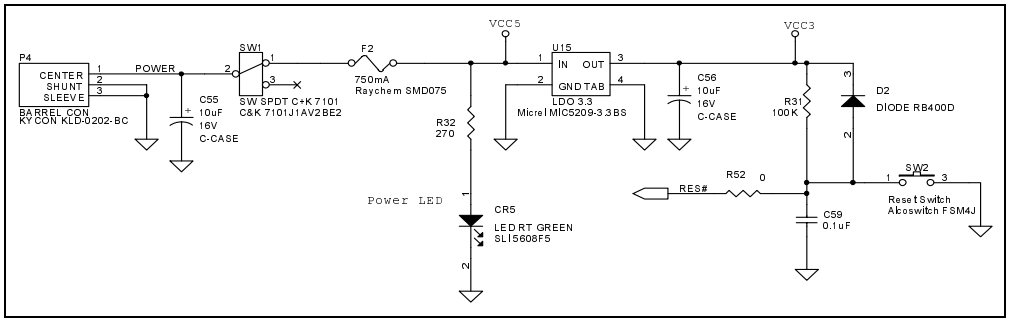
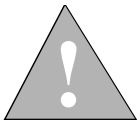


Figure 2-9. ISDN TA Power Supply and Reset Circuit



CAUTION: If using your own power supply, ensure that it is a 5-V supply. Using a 9-V or 12-V supply will permanently damage the board.

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Test Interface Port (TIP)

The test interface port (also available from AMD, but not included with the ISDN TA reference design) provides an interface to a low-cost AMD development board. This board is useful for testing, debugging, and developing software on AMD's reference designs. It contains an 8-bit Flash memory device, LEDs, hexadecimal displays, an LCD, serial ports, a parallel port, and an Ethernet controller.

In the event of a Flash memory failure on the main board, you can boot the ISDN TA from an external TIP board. Refer to the *AMD Test Interface Port Board User's Manual*, order #22505 for more information. Note that the TIP board and user's manual are available from AMD, but are not included in your kit. To order the TIP board kit, contact your local AMD sales office at the number listed on the inside back cover of this manual. The TIP connector circuit and pinout are shown in Figure 2-10 and sheet 6 of the schematics included in your kit.

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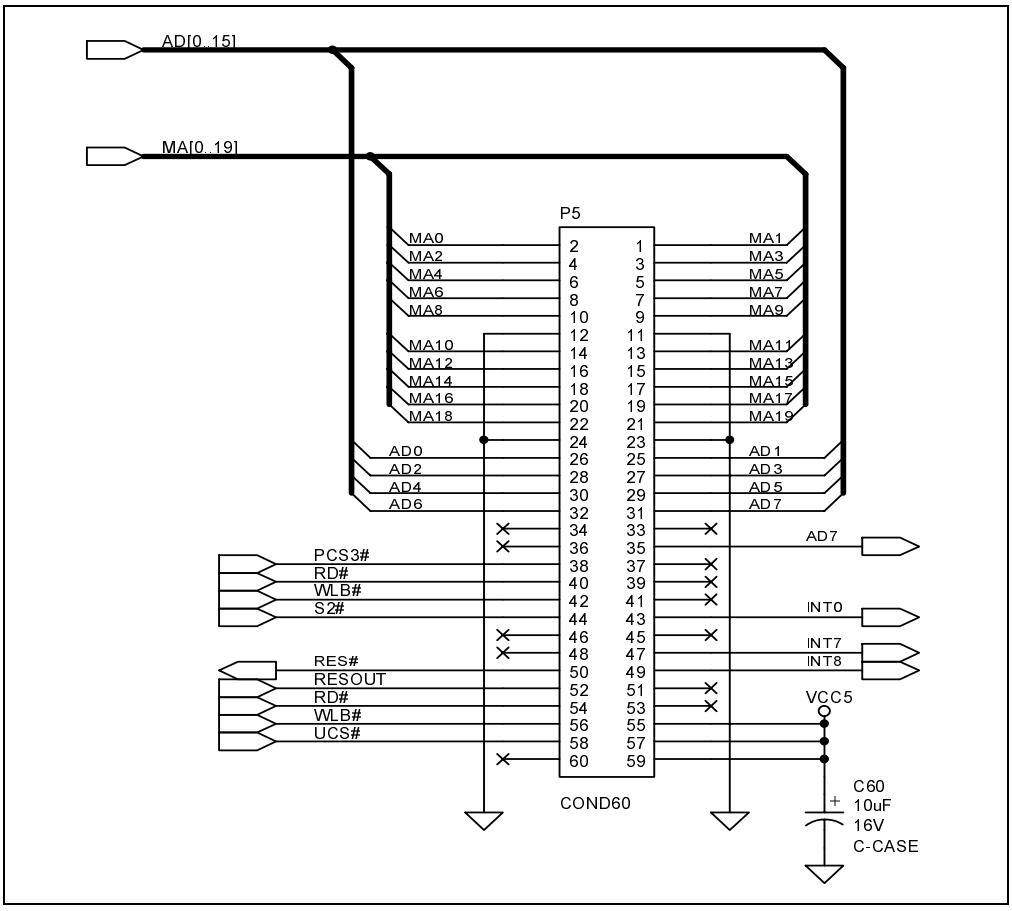

Figure 2-10. Test Interface Port (TIP) Connector Circuit

To boot from the TIP board, the Am186CC microcontroller must be reset in x8 boot mode, and the UCS# signal must be routed to the TIP Flash memory. The x8 boot is accomplished by using JP2 to pull the MCS0# signal to ground during reset (see Figure 2-11 and sheet 6 of the schematics included in your kit). To route the UCS# signal to the TIP Flash memory, remove the jumper on JP1 and install the jumper on the TIP. When booting from the on-board Flash memory, use only JP1; this routes UCS# to the ISDN TA Flash memory.

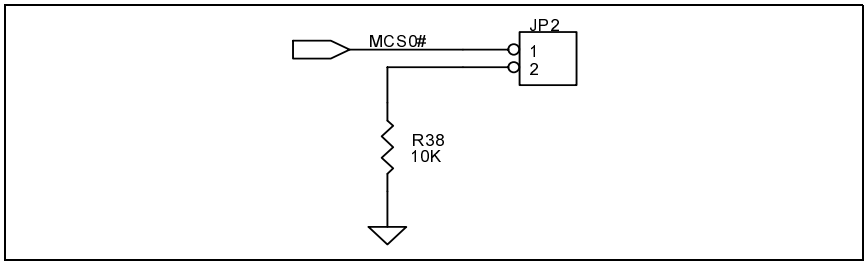

Figure 2-11. Flash Memory Jumper for x8 Boot (JP2)

To boot from the TIP Flash memory, perform the following:

- Disconnect UCS# from on board Flash memory (remove JP1).
- Route UCS# to the TIP Flash memory (install UCS# jumper on TIP).
- Boot in x8 mode (install JP2).

To boot from on-board Flash memory, perform the following:

- Route UCS# to the on-board Flash memory (install JP1).
- Boot in x16 mode (remove JP2).

A corrupted Flash memory on the main board can be restored by booting from the TIP board, entering the E86MON software **Z** command, changing the jumpers to the settings for booting from the main board, then following the prompts from the **Z** command.

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ISDN TA Pin Usage

Table 2-3 shows the Am186CC microcontroller multiplexed pin usage for the ISDN TA. The following conventions are used in the table:

- [] indicates an alternate pin function.
- {} indicates a reset configuration (pinstrap).
- **boldface** denotes the pin function.

Table 2-3. Pin Usage for the ISDN TA

Pin Name	Usage
TMRIN0 **[PIO0]**	High-Speed UART DCD
TMROUT1 **[PIO1]**	DCE serial port flow control for Plug and Play
ARDY **[PIO8]**	USB active LED
RTRA# **[PIO18]**	ISDN B1-Channel active LED
TMRIN1 **[PIO27]**	High-Speed UART RI#
TMROUT0 **[PIO28]**	DCE serial port flow control for Plug and Play
PCS7# **[PIO31]**	Flash memory RY/BY
PCS6# **[PIO32]**	ISDN D-Channel active LED
SRDY **[PIO35]**	Flash memory A18
RTRB# **[PIO39]**	ISDN B2-Channel active LED
RXDC [RXDC] **[PIO42]**	USB detect
TXDC [TXDC] **[PIO43]**	USB VCC enable
INT0	TIP – Ethernet IRQ
INT2	ISDN U transceiver interrupt
INT6	ISDN S/T transceiver interrupt
INT7 [PIO7]	TIP – serial port 1 interrupt
INT8 [PWD] [PIO6]	TIP – serial port 0 interrupt

Table 2-3. Pin Usage for the ISDN TA (Continued)

Pin Name	Usage
UCS# [ONCE#]	Flash memory CE#
LCS# **[RAS0#]**	DRAM RAS#
MCS0# **{UCSX8#}** [PIO4]	x8 TIP boot
MCS1# **[CAS1#]**	DRAM LCAS#
MCS2# **[CAS0#]**	DRAM UCAS#
PCS1# {USBSEL1} [PIO14]	S/T-transceiver chip select
PCS3#	TIP
RXDA [DDA] **[RXDA]**	HDLC Channel A interface to ISDN components
TXDA [DUA] **[TXDA]**	HDLC Channel A interface to ISDN components
RCLKA [DCLA] **[CLKA]**	HDLC Channel A interface to ISDN components
TCLKA [FSCA] **[FSCA]**	HDLC Channel A interface to ISDN components
RXDHU [PIO16]	High-Speed UART receive data
TXDHU	High-Speed UART transmit data
CTSHU# [CTSD#] [TSCD#] [PIO46]	High-Speed UART clear-to-send
RTRHU# [RTRD#] [PIO47]	High-Speed UART ready-to-receive
SCLK [PIO11]	ISDN U transceiver synchronous serial interface
SDATA [PIO12]	ISDN U transceiver synchronous serial interface

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RESCON Configuration

The RESCON register provides a way to make design-specific hardware configuration information available to software. The RESCON register is read from AD0–AD15 during reset. Because the Am186CC microcontroller has weak internal pulldowns, the default value is logic Low. Setting a bit requires a 10-kΩ pullup resistor. Figure 2-12 shows the RESCON register bits.

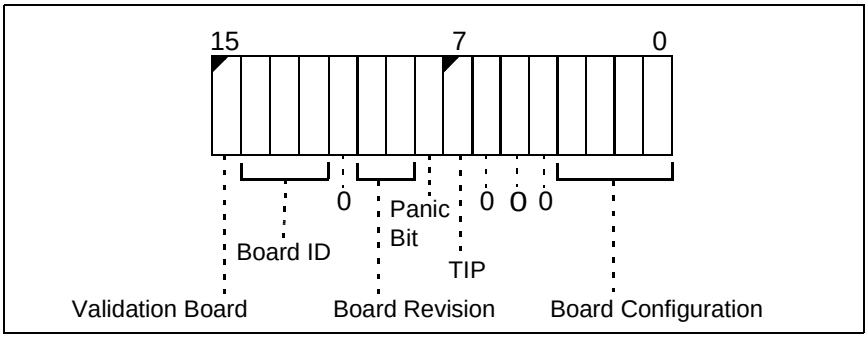
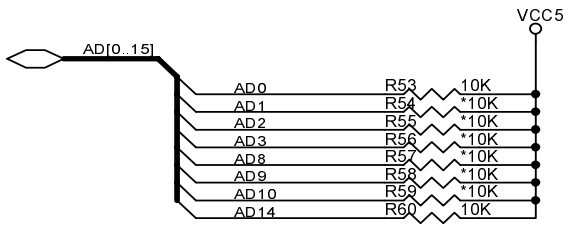


Figure 2-12. RESCON Register Bits

- **Validation Board:** Identifies if the board is a validation board.
- **Board ID:** Unique board identifier that is used to determine what features are available to the software.
- **0:** Bits are reserved for future use.
- **Panic Bit:** Enables you to set conservative values to resuscitate a monitor (e.g., E86MON software) after the CPU speed, refresh rate, or wait states have been incorrectly programmed.
- **TIP:** Identifies the TIP board as being present in the system.
- **Board Configuration:** Identifies particular population option for the board.

Figure 2-13 and sheet 6 of the schematics included in your kit show the schematic for the RESCON configuration. The Board ID for the ISDN TA is 100h. The Board Configuration for the ISDN U interface population option is 0000h. The S interface Board Configuration is 0001h.



Note: The components designated with an asterisk (*) are not populated.

Figure 2-13. ISDN TA RESCON Configuration

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Appendix A

Bill of Materials (BOM)

The ISDN TA S/T interface reference design board bill of materials begins on page A-2.

Table A-1. ISDN TA S/T Interface Board BOM

Item	Quantity	Reference	Part	Part Spec.	PCB Footprint
1	1	CR1	LED SOT-23[1]	Lumex SSL-LX15IGC-RP-TR	SOT-23
2	7	CR2,CR3,CR4, CR5,CR6,CR7,CR8	LED RT green	SLI 5608F5	TH-2
3	1	C1	3.3 µF	Tantalum, B CASE, 16V	B-CASE
4	2	C2,C14,C24	1000 pF	± 10%, X7R, 16V	603
5	2	C3,C15	0.01 µF	± 10%, X7R, 16V	603
6	18	C4,C5,C7,C8,C9, C12,C13,C23,C24, C42,C43,C50,C51, C52,C59,C64,C66, C67	0.1 µF	± 10%, X7R, 16V	603
7	7	C6,C10,C11,C61, C62,C63,C65	0.022 µF	± 10%, X7R, 16V	603
8	4	C16,C17,C18,C19	0.33 µF	± 10%, X7R, 16V	805
9	4	C20,C21,C57,C58	27 pF	± 10%, COG, 25V	603
10	4	C22,C55,C56,C60	10 µF	Tantalum, C CASE, 16V	C-CASE
11	2	C25,C26	680 pF	± 10%, X7R, 16V	603
12	1	C27	1.0 µF[1]	Phillips 2222 370 75105	TH-2
13	1	C28	820 pF[1]	± 5%, X7R, 16V	603
14	2	C29,C31	3300 pF[1]	± 10%, X7R, 16V	603
15	1	C30	1.0 µF[1]	Phillips 2222 373 41105, or Vitramon VJ9253Y105KXPM	TH-2
16	3	C32,C33,C34	1.0 µF[1]	± 10%, X7R, 16V	603

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Table A-1. ISDN TA S/T Interface Board BOM (Continued)

Item	Quantity	Reference	Part	Part Spec.	PCB Footprint
17	7	C35,C36,C37,C38, C39,C40,C41	1.01 µF[1]	± 10%, X7R, 16V	603
18	8	C44,C45,C46,C47, C48,C49,C68,C69	220 pF	± 10%, X7R, 16V	603
19	2	C54,C53	22 pF	± 10%, COG, 25V	603
20	2	D2,D1	Diode RB400D	ROHM RB400D	SOT-23
21	1	FB1	FB	MURATA BLM31P500SPB	1206
22	2	FB3,FB2	FB	MURATA BLM21A121SPB	805
23	1	F1	Fuse[1]	Raychem TR600-150	TH-2
24	1	F2	750 mA	Raychem SMD075	SMT-2
25	1	JP1	Flash JP	AMP 103186-1	TH-2
26	1	JP2	Header 2	AMP 103186-1	TH-2
27	1	P1	RJ45A	AMP 555153-1	TH-12
28	1	P2	Connector DB9	AMP 787844-5	TH-11
29	1	P3	USB connector	AMP 787780-1	TH-4
30	1	P4	Barrel connector	KYCON KLD-0202-BC	TH-3
31	1	P5	COND60	AMP 104068-6	TH-2x30
32	2	Q1,Q2	TN0200T	Temic TN0200T	SOT-23
33	23	R1,R4,R5,R33,R38, R45,R46,R47,R48, R49,R50,R53,R60, R84,R87,R89,R91, R93,R95,R97,R98, R99,R100	10K	± 5%,1/10W	603

Table A-1. ISDN TA S/T Interface Board BOM (Continued)

Item	Quantity	Reference	Part	Part Spec.	PCB Footprint
34	3	R6,R43,R44	0[1]	± 5%, 1/10W	603
35	2	R11,R8	100	± 1%, 1/8W	805
36	1	R13	17.8K[1]	± 1%, 1/8W	805
37	1	R14	10K[1]	± 5%, 1/8W	805
38	2	R15,R19	1.1K[1]	Dale WSC-2	SMT-2
39	2	R16,R18	137[1]	± 1%, 1/8W	805
40	1	R17	270[1]	± 5%,1/10W	603
41	1	R20	2.2M[1]	± 5%, 1/8W	805
42	1	R21	21[1]	± 1%, 1/4W	1206
43	2	R22,R23	16.9[1]	± 1%, 1/4W	1206
44	7	R24,R54,R55,R56, R57,R58,R59	10K[1]	± 5%, 1/10W	603
45	2	R25,R26	680	± 5%, 1/10W	603
46	1	R27	1.5K	± 5%, 1/10W	603
47	3	R28,R29,R52	0	± 5%, 1/10W	603
48	5	R30,R32,R35,R36, R37	270	± 5%, 1/10W	603
49	2	R31,R107	100K	± 5%, 1/10W	603
50	1	R51	10	± 5%, 1/10W	603
51	4	R61,R62,R64,R66	82	± 5%, 1/10W	603

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Table A-1. ISDN TA S/T Interface Board BOM (Continued)

Item	Quantity	Reference	Part	Part Spec.	PCB Footprint
52	25	R63,R65,R67,R68, R69,R70,R71,R72, R73,R74,R75,R76, R77,R78,R79,R80, R81,R82,R83,R85, R86,R88,R90,R92, R96	56	± 5%, 1/10W	603
53	8	R101,R102,R103, R104,R105,R106,R 116,R117	22	± 5%, 1/10W	603
54	2	R110,R108	2K	± 5%, 1/4W	1206
55	2	R109,R111	3.6K	± 5%, 1/4W	1206
56	4	R112,R113,R114, R115	22.6	± 1%, 1/2W	1210
57	1	SW1	SW SPDT C+K 7101	C&K 7101J1AV2BE2	TH-3
58	1	SW2	Reset switch	Alcoswitch FSM4J	TH-4
59	1	U1	Am186CC	AM186CC	PQFP-160
60	1	U2	V53C16258H SOJ	Mosel Vitelic V53C16258HK40	SOJ-40
61	1	U3	Am29F400 TSOP	AM29F400BT-55EC	TSOP-48
62	1	U4	Am79C32A PLCC	AM79C32AJC	PLCC-44
63	1	U5	S Transformer	Pulse PE-65799	SMT-16
64	1	U6	PE65554[1]	Pulse PE65554	TH-8
65	1	U7	6N139[1]	Siemens 6N139	DIP-8
66	1	U8	LH1465AB[1]	Lucent LH1465AB	DIP-8
67	1	U9	T7237A PLCC[1]	Lucent T7237A- - ML-DT	PLCC-44

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Table A-1. ISDN TA S/T Interface Board BOM (Continued)

Item	Quantity	Reference	Part	Part Spec.	PCB Footprint
68	1	U10	U Transformer[1]	Pulse T4008	TH-10
69	1	U11	SM6T6V8CA[1]	SGS-Thomson SM6T6V8CA	SMB
70	1	U12	P2300SB[1]	Teccor P2300SB,or SGS-Thomson SMP100-200	SMB
71	1	U13	SP207	Sipex SP207HBEA	SSOP-28
72	1	U14	74ACT04	National 74ACT04SC	SOIC-14
73	1	U15	LDO 3.3	Micrel MIC5209-3.3BS	SOT-223
74	2	U16,U17	LC03-6	Semtech LC03-6	SO-8
75	1	X1	12.228MHz	Ecliptek EC1-12.228M-CL100	HC-49
76	1	X2	15.36011 MHz[1]	Saronix SRX5144	HC-49
77	1	X3	24.000 MHz	Ecliptek EC2-24.000M-CL100	HC-49

1. This part is not populated.

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Appendix B

Glossary

2B+D
Describes the BRI configuration for ISDN of two bearer channels and one D channel.

2B1Q
Two binary, one quaternary, data format for the U-interface. One quaternary symbol (±3, ±1) represents two bits.

B Channel
Bearer channel, 64 Kbit/s voice/data channel for ISDN.

bit/s
Bits per second.

BRI
Basic Rate Interface. The simple 2B+D access method defined by CCITT recommendation I.430.

CCITT/ITU
International Telegraph and Telephone Consultative Committee / International Telecommunications Union. ITU is an agency of the UN. CCITT is a committee of the ITU which makes recommendations for network communications.

C.O.
Central Office.

CPE
Customer Premises Equipment. Devices such as the NT1, designated to be the customer's responsibility to provide.

D Channel
16 Kbit/s channel used to carry out-of-band network signaling or packet-mode user data. (Refer to the ITU standards found at www.itu.ch.)

FCC
Federal Communications Commission. Regulates the U.S. telephone industry.

GCI
General Circuit Interface. Also called IOM-2.

HDLC
High-Level Data-Link Controller. ISO standard for layer-2 data bit-oriented communications protocol. HDLC is used for LAPB, LAPD, V.120 and SS7.

IDC
ISDN Data Controller. Performs D channel processing on the S/T reference point data.

IOM-2
Industry standard serial bus developed by Siemens.

ISDN
Integrated Services Digital Network.

ISO
International Standardization Organization. Developed the OSI reference model and HDLC standards.

Kbit/s
Kilobits per second.

LAPB
Link Access Procedure Balanced. The X.25 data link layer protocol. X.25 is a special case of HDLC.

LAPD
Link Access Procedures on the D channel. ISDN data link layer protocol defined by CCITT. LAPD is a special case of HDLC

LE
Local Exchange. Class 5 C.O.

MPI
Microprocessor Interface.

NT1
Network Termination Type 1. Termination device located on the customer premises that converts the two-wire U-interface to a four wire S/T-interface.

NT2
Network Termination Type 2. Termination device separating the S and T reference points used for customer-controlled communication distribution (such as PBX or LAN)

OSI
Open Systems Interconnection reference model. Seven layer architecture developed by ISO for open system communications.

PBX
Private Branch Exchange. Customer site switch.

PCM
Pulse Code Modulation.

PIO
Programmable Input/Output.

R-Interface
Reference point between non-ISDN devices and terminal adapters.

SBP
Serial Bus Port. The simple PCM highway used by the Am79C32A device.

SS7
Signal System 7. High-speed, common channel interoffice signaling system necessary for ISDN implementation.

S/T-interface
The reference point comprising the four-wire interface between the network termination device (NT1) and the terminal equipment (TE1) or terminal adapter (TA). If an NT2 is used for on-site switching, the S and T reference points are considered to be separated at the NT2 device. The T reference point is between the NT1 and NT2, and the S reference point is between the NT2 and the TE1 or TA.

TA
Terminal Adapter. Converts non-ISDN information from a TE2 device to a format that can be used for ISDN.

TDM
Time Division Multiplexing.

TE
Terminal Equipment. Equipment that may be placed on ISDN (directly or indirectly).

TE1
Terminal Equipment Type 1. ISDN compatible terminal equipment.

TE2
Terminal Equipment Type 2. Non-ISDN compatible terminal equipment, which requires a terminal adapter.

U-interface
Reference point comprising the two-wire interface between the LE and NT device.

USB
Universal serial bus. Intel standard; used for PC-to-peripheral communication.

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