

DESCRIPTION

The HYM532124A is a 1M x 32-bit EDO mode CMOS DRAM module consisting of two HY5118164B in 42/42 pin SOJ or 44/50 pin TSOPII on a 72 pin glass-epoxy printed circuit board. Two 0.01 μ F decoupling capacitors are mounted for each DRAM.

The HYM532124AW/ASLW are Tin-Lead plated and HYM532124AWG/ASLWG are Gold plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 4M byte memory.

FEATURES

- Low power dissipation
Max. self-refresh 3.9mW (SL-part)
Max. battery back-up 4.9mW (SL-part)
Max. CMOS standby 3.3mW (SL-part)
11.0mW

Max. TTL standby 11.0mW

Max. operating

Speed	Power
60	1.76W
70	1.65W
80	1.54W

- Single power supply of 5V $\pm$ 10%
- TTL compatible inputs and outputs
- Fast access time

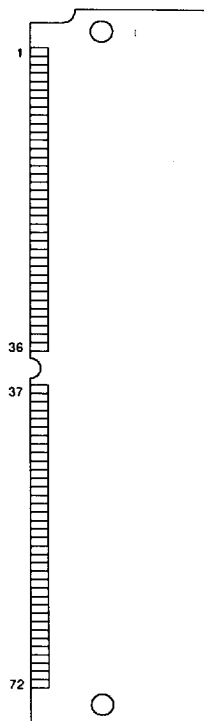
Speed	tRAC	tCAC	tHPC
60	60ns	15ns	25ns
70	70ns	20ns	30ns
80	80ns	25ns	35ns

- EDO mode operation
- CAS-before-RAS, RAS-only, Hidden refresh, Self-refresh
- 1024 refresh cycles / 256ms (SL-part)
1024 refresh cycles / 16ms

PIN DESCRIPTION

RAS0, RAS2	Row Address Strobe
CAS0-CAS3	Column Address Strobe
WE	Write Enable
A0-A9	Address Input
DQ0-DQ31	Data Input/Output
PD1-PD4	Presence Detect
Vcc	Power (+ 5V)
Vss	Ground

PIN CONNECTION



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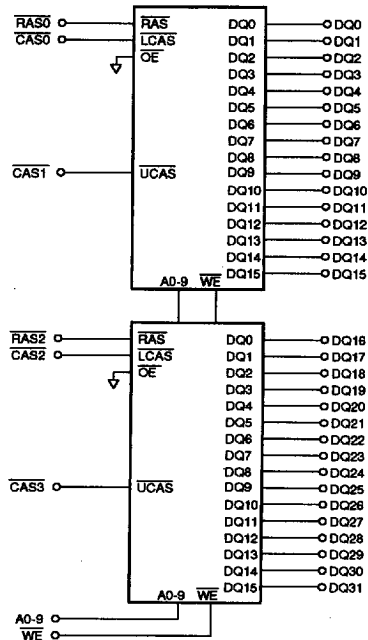
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PIN NAME

#	NAME	#	NAME
1	Vss	37	NC
2	DQ0	38	NC
3	DQ16	39	Vss
4	DQ1	40	CAS0
5	DQ17	41	CAS2
6	DQ2	42	CAS3
7	DQ18	43	CAS1
8	DQ3	44	RAS0
9	DQ19	45	NC
10	Vcc	46	NC
11	NC	47	WE
12	A0	48	NC
13	A1	49	DQ8
14	A2	50	DQ24
15	A3	51	DQ9
16	A4	52	DQ25
17	A5	53	DQ10
18	A6	54	DQ26
19	NC	55	DQ11
20	DQ4	56	DQ27
21	DQ20	57	DQ12
22	DQ5	58	DQ28
23	DQ21	59	Vcc
24	DQ6	60	DQ29
25	DQ22	61	DQ13
26	DQ7	62	DQ30
27	DQ23	63	DQ14
28	A7	64	DQ31
29	NC	65	DQ15
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	NC	69	PD3
34	RAS2	70	PD4
35	NC	71	NC
36	NC	72	Vss

BLOCK DIAGRAM



PRESENCE DETECT PINS

PIN	-60	-70	-80
PD1	Vss	Vss	Vss
PD2	Vss	Vss	Vss
PD3	NC	Vss	NC
PD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 7.0	V
VCC	Voltage on Vcc Relative to Vss	-1.0 to 7.0	V
Ios	Short Circuit Output Current	50	mA
Pd	Power Dissipation	2	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Vcc	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	Vcc+ 1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to Vss.

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DC CHARACTERISTICS

(TA= 0°C to 70°C, Vcc= 5V± 10%, Vss= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pin)	VSS ≤ VIN ≤ VCC+ 1.0, All other pins not under test= VSS		-20	20	μA	
ILO	Output Leakage Current (High Impedance State)	VSS ≤ VOUT ≤ VCC, RAS & CAS at VIH		-10	10	μA	
ICC1	Vcc Supply Current, Operating	trC= trC (min.)	60 70 80	- - -	320 300 240	mA	1,2,3
ICC2	Vcc Supply Current, TTL Standby	RAS & CAS at VIH, other inputs ≥ VSS		-	2	mA	
ICC3	Vcc Supply Current, RAS-only refresh	trC= trC (min.)	60 70 80	- - -	320 280 240	mA	1,3
ICC4	Vcc Supply Current, EDO mode	thPC= thPC (min.)	60 70 80	- - -	280 240 200	mA	1,2,3
ICC5	Vcc Supply Current, CMOS Standby	RAS & CAS ≥ VCC-0.2V	SL-part	-	2 0.6	mA	
ICC6	Vcc Supply Current, CAS-before-RAS refresh	trC= trC (min.)	60 70 80	- - -	320 300 280	mA	1,3
ICC7	Vcc Supply Current, Battery Back Up (SL-part only)	trC= 62.5μs CAS= CBR cycling or 0.2V, WE= VCC - 0.2V, A0-A9= VCC- 0.2V or 0.2V DQ0-DQ31= VCC- 0.2V, 0.2 V, or open	trAS ≤ 300ns trAS ≤ 1μs	- -	0.7 0.9	mA	1,4,5
ICC8	Vcc Supply Current, Self-Refresh (SL-part only)	RAS & CAS ≤ 0.2V other pins same as ICC7		-	0.7	mA	5
VOL	Output Low Voltage	IOL= 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH= -5mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4, ICC6 and ICC7 depend on cycle rate.
2. ICC1, ICC3, ICC4, and ICC6 depend on output loading. Specified values are obtained with the output open.
3. ICC is specified as average current. For ICC1, ICC3 and ICC6, address can be changed maximum two times while RAS= VIL. For ICC4, address can be changed maximum once while CAS= VIH.
4. trAS (max.)= 1μs only applied to refresh of battery backup but trAS (max.)= 10μs is applied to normal functional operating.
5. ICC5 (max.)= 1.2mA, ICC7 and ICC8 are applied to SL-part only (HYM532124ASLW/ASLTW)

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AC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM532124A W-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	trc	Random Read or Write Cycle Time	105	-	125	-	145	-	ns	
2	trPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	
3	thPC	EDO Mode Cycle Time	25	-	30	-	35	-	ns	
4	trHCP	Time from CAS Precharge	40	-	40	-	50	-	ns	
5	trAC	Access Time from RAS	-	60	-	70	-	80	ns	4,9,10
6	tcAC	Access Time from CAS	-	17	-	20	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	35	-	35	-	45	ns	4
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tCEZ	Output Buffer Turn-off Delay	0	15	0	15	0	15	ns	5
11	tt	Transition Time (Rise and Fall)	2.5	50	2.5	50	2.5	50	ns	3
12	trP	RAS Precharge Time	40	-	50	-	60	-	ns	
13	trAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	trASP	RAS Pulse Width (EDO Mode)	60	125K	70	125K	80	125K	ns	
15	trSH	RAS Hold Time	13	-	15	-	20	-	ns	
16	tCSH	CAS Hold Time	40	-	50	-	60	-	ns	
17	tcAS	CAS Pulse Width	13	10K	15	10K	20	10K	ns	
18	trCD	RAS to CAS Delay	20	45	20	50	20	60	ns	9
19	trAD	RAS to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	CAS Precharge Time	7	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	trAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	15	-	15	-	ns	
26	tAR	Column Address Hold Time from RAS	28	-	28	-	28	-	ns	
27	trAL	Column Address to RAS Lead Time	30	-	35	-	40	-	ns	
28	trCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	trCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6
30	trRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	twCH	Write Command Hold Time	10	-	15	-	15	-	ns	
32	twCR	Write Command Hold Time from RAS	53	-	53	-	58	-	ns	
33	tWP	Write Command Pulse Width	10	-	10	-	10	-	ns	
34	trWL	Write Command to RAS Lead Time	15	-	15	-	15	-	ns	
35	tcWL	Write Command to CAS Lead Time	13	-	15	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	10	-	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	53	-	53	-	58	-	ns	
39	tREF	Refresh Period (1024 cycles)	-	16	-	16	-	16	ms	
		SL-part	-	256	-	256	-	256	ms	12
40	twCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

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AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HYM532124A W-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
42	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
43	tcPT	CAS Precharge Time (CBR Counter Test)	30	-	35	-	40	-	ns	
44	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
45	tWRH	WE to RAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tRASS	RAS Pulse (Self Refresh)	100	-	100	-	100	-	ns	
47	tRPS	RAS Precharge Time (Self Refresh)	110	-	130	-	150	-	ns	
48	tCHS	CAS Hold Time from RAS (Self Refresh)	-50	-	-50	-	-50	-	ns	
49	tDOH	Output Data Hold Time	5	-	5	-	5	-	ns	
50	tREZ	Output Buffer Turn-off Delay (RAS)	0	15	0	15	0	15	ns	5,15
51	tWEZ	Output Buffer Turn-off Delay (WE)	0	15	0	15	0	15	ns	5
52	twPE	WE Pulse Width for Output Disable	10	-	10	-	10	-	ns	
53	twED	WE to Data Delay Time	15	-	15	-	15	-	ns	



NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If RAS= Vss during power-up, the HYM532124A could begin an active cycle. This condition results in higher power-up current than necessary demands from the power-up. It is recommended that RAS and CAS track with Vcc during power-up or be held at a valid VIH in order to minimize the power-up current.
3. Refer to the HY5118164B data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF.(VOH= 2.0V,VOL= 0.8V)
5. tCEZ(max.), tREZ(MAX) and tWEZ(MAX) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either trCH or trRH must be satisfied for a read cycle.
7. These parameters are referenced to CAS leading edge in early write cycles and to WE leading edge in late write or read-modify-write cycles.
8. twCS is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If twCS $\geq$ twCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
10. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
11. Measured with the specified current load and 100pF.
12. A burst of 1024 CAS-before-RAS refresh cycles must be executed within 16ms after exiting self refresh (for SL-part).
13. If tCWD $\geq$ twCS(MIN.), tRWD $\geq$ tRWD(MIN.), tAWD $\geq$ tAWD(MIN.) and tCPWD $\geq$ tCPWD(MIN.), the cycle is a read modify write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time and until CAS goes back to VIH) is indeterminated.
14. In CAS before RAS self refresh mode.
In case of using distributed CAS before RAS refresh, refresh 1024 times during a 256ms after reset
In case of using burst CAS before RAS refresh, refresh 1024 times during a 16ms after reset
In case of using RAS only refresh, refresh against all refresh address during a 16ms after reset
15. If RAS goes to high before CAS high going, the open circuit condition of the output is achieved by CAS high going. If CAS goes to high before RAS high going, the open circuit condition of the output is achieved by RAS high going.

CAPACITANCE

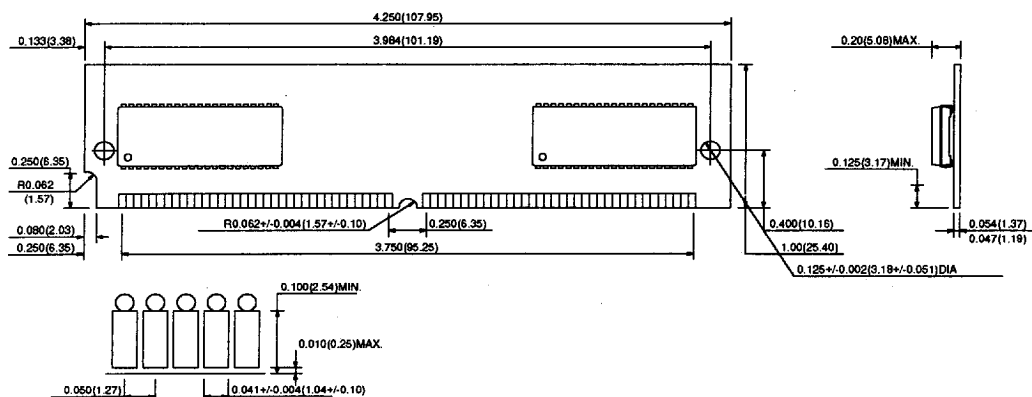
(TA= 25°C, Vcc= 5V $\pm$ 10%, Vss= 0V, f= 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A9)	-	25	pF
CIN2	Input Capacitance (WE)	-	25	pF
CIN3	Input Capacitance (RAS0,RAS2)	-	15	pF
CIN4	Input Capacitance (CAS0-CAS3)	-	15	pF
CDQ	Data Input/output Capacitance (DQ0-DQ31)	-	15	pF

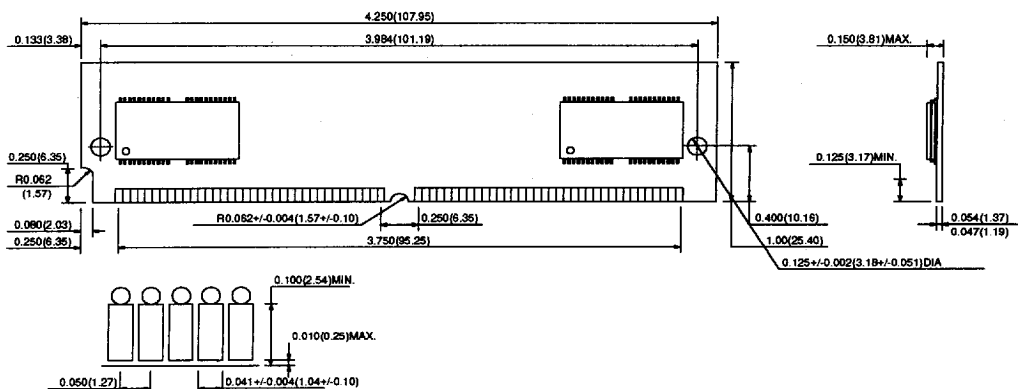
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**72 pin Single In-line Memory Module (W ; Tin-Lead plated, WG ; Gold plated)
HYM532124A (SOJ Mounted)**

UNIT : INCH(mm)
TOLERANCE : +/-0.005(0.13)



UNIT : INCH(mm)
TOLERANCE : +/-0.005(0.13)



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ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM532124AW	60/70/80		SIMM	Tin-Lead
HYM532124ASLW	60/70/80	SL-part	SIMM	Tin-Lead
HYM532124ATW	60/70/80		SIMM	Tin-Lead
HYM532124ASLTW	60/70/80	SL-part	SIMM	Tin-Lead
HYM532124AWG	60/70/80		SIMM	Gold
HYM532124ASLWG	60/70/80	SL-part	SIMM	Gold
HYM532124ATWG	60/70/80		SIMM	Gold
HYM532124ASLTWG	60/70/80	SL-part	SIMM	Gold

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