6501122 NATIONAL SEMICONDUCTOR
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National Semiconductor

PRELIMINARY

DM54AS264/DM74AS264 Look-Ahead Carry Generator

General Description

This circuit is a high speed, look-ahead carry generator capable of anticipating a carry across four counters. It is cascadable to perform look-ahead across N-bit counters. Carry, generate-carry and propagate-carry output functions are provided as shown in the connection diagram.

This circuit can accommodate counters which have either low level carry pulse or high level carry pulse outputs, and can provide high speed carry look-ahead capability for any word length. Each AS264 generates the look-ahead (anticipated carry) across a group of four counters, and in addition, other carry look-ahead circuits may be employed to anticipate a carry across sections of four look-ahead packages up to N bits. This method of cascading circuits to perform multi-level look-ahead is illustrated under Typical Applications.

Features

- Advanced oxide-isolated ion implanted Schottky TTL process
- Switching specification at 50 pF
- Switching specifications guaranteed over full temperature range and V_{CC} range
- PNP inputs reduce input loading

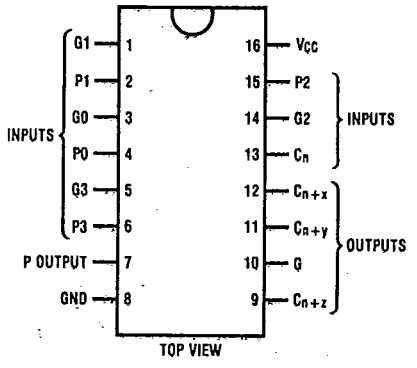
Absolute Maximum Ratings

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Operating Free-Air Temperature Range	
DM54AS264	−55°C to +125°C
DM74AS264	0°C to 70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



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DM54AS264 (J) DM74AS264 (N)

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Recommended Operating Conditions

Symbol	Parameter	DM54AS264			DM74AS264			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−2	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions	DM54AS264			DM74AS264			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	C_n	V_{CC} = 5.5V, V_I = 7V			500			500	µA
	G0, G7				700			700	
	G1				800			800	
	G3, P0, P1				400			400	
	P2				300			300	
	P3				200			200	
I_{IH}	C_n	V_{CC} = 5.5V, V_I = 2.7V			100			100	µA
	G0, G2				140			140	
	G1				160			160	
	G3, P0, P1				80			80	
	P2				60			60	
	P3				40			40	
I_{IL}	C_n	V_{CC} = 5.5V, V_I = 0.4V			−2.5			−2.5	mA
	G0				−3.5			−3.5	
	G1, G2				−4			−4	
	G3, P0, P1				−2			−2	
	P2				−1			−1	
	P3				−1.5			−1.5	
I_O (Note 2)	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V	−30		−112	−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V		26			26		mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V		28			28		mA

Switching Characteristics over recommended supply and temperature range (Note 1)

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter		From (Input)	To (Output)	Conditions	DM54AS264			DM74AS264			Units
					Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	G0, G1, G2, G3, P0, P1, P2, or P3	C_{n+x}, C_{n+y}, or C_{n+z}	$C_L = 50$ pF, $R_L = 500\Omega$		5			5		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					5			5		
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	G0, G1, G2, G3, P1, P2, or P3	G			5			5		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					5			5		
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	P0, P1, P2, or P3	P			5			5		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					5			5		
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	C_{n+x}, C_{n+y}, or C_{n+z}			6			6		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					5			5		

Note 1: See Section 1 for test waveforms and output load.

Function Tables

Logic Equations for the 'AS264 are:

Active High Carry Counters (C_n = H)

$C_{n+x} = \overline{G0}$
$C_{n+y} = \overline{G0} \cdot \overline{G1}$
$C_{n+z} = \overline{G0} \cdot \overline{G1} \cdot \overline{G2}$
$\overline{G} = \overline{G0} \cdot \overline{G1} \cdot \overline{G2} \cdot \overline{G3}$
$\overline{P} = 0$

Active Low Carry Counters (C_n = L)

$C_{n+x} = \overline{P0}$
$C_{n+y} = \overline{P0} \cdot \overline{P1}$
$C_{n+z} = \overline{P0} \cdot \overline{P1} \cdot \overline{P2}$
$\overline{P} = \overline{P0} + \overline{P1} + \overline{P2} + \overline{P3}$
$G = \overline{P1}\,\overline{G3}\,\overline{G2}\,\overline{G1} + \overline{P2}\,\overline{G3}\,\overline{G2}\,\overline{G1} + \overline{P3}\,\overline{G3}$

Inputs								Output
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{G}$
L	X	X	X	X	X	X	X	L
X	L	X	X	L	X	X	X	L
X	X	L	X	L	L	X	X	L
X	X	X	L	L	L	L	X	L
X	X	X	X	L	L	L	L	L
All Other Combinations								H

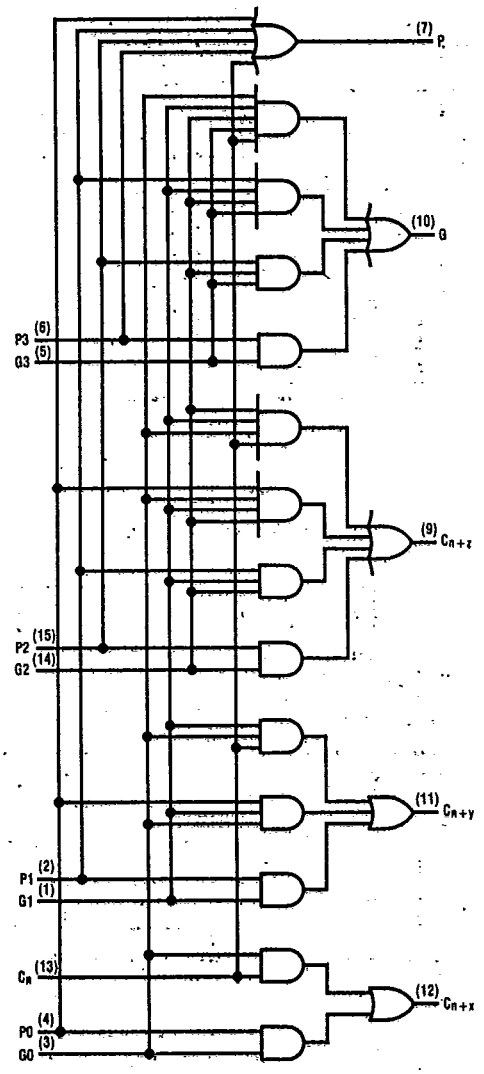
Inputs					Output
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	C_n	$\overline{P}$
L	L	L	L	L	L
All Other Combinations					H

Inputs			Output
G0	P0	C_n	C_{n+x}
H	H	X	H
H	X	H	H
All Other Combinations			L

Inputs					Output
G1	G0	P1	P0	C_n	C_{n+y}
H	X	H	X	X	H
H	H	X	H	X	H
H	H	X	X	H	H
All Other Combinations					L

Inputs							Output
G2	G1	G0	P2	P1	P0	C_n	C_{n+z}
H	X	X	H	X	X	X	H
H	H	X	X	H	X	X	H
H	H	H	X	X	H	X	H
H	H	H	X	X	X	H	H
All Other Combinations							L

Logic Diagram



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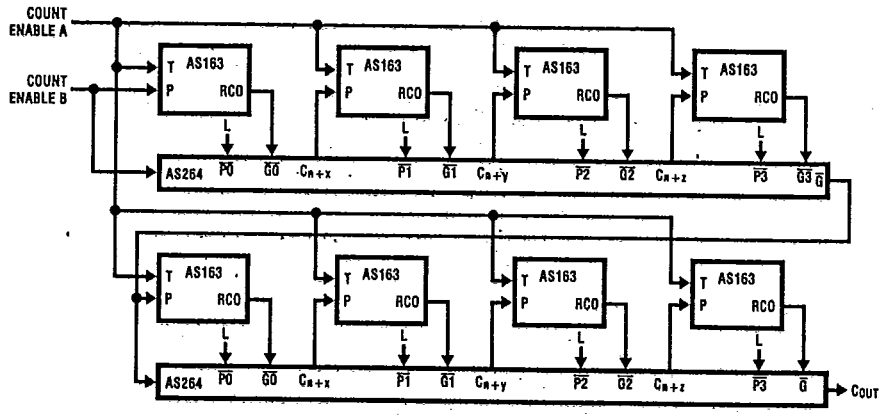
V_{CC} = pin 16
GND = pin 8

Typical Applications

Active High Carry Scheme



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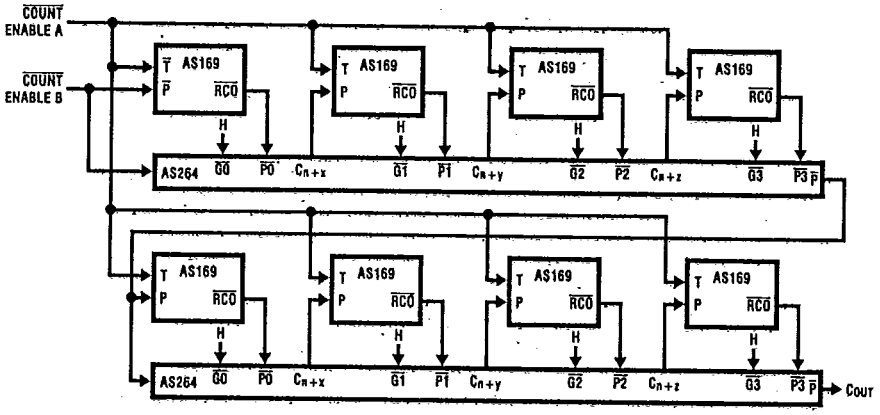
Active Low Carry Scheme



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