REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes to 1.2.1. Made technical changes to table I. Added a square chip carrier package to 1.2.2. Changes to figure 1 and figure 4. Added vendor CAGE number 59621 for the square chip carrier package.	91-10-18	Monica L. Poelking
B	Added device types 05 through 08. Made technical changes to table I. Added CAGE number 65896 for device types 05 through 08. Editorial changes throughout.	92-06-19	Tim Noh

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV	B	B	B	B	B														
SHEET	15	16	17	18	19														

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Phu Nguyen

CHECKED BY
Tim H. Noh

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
88-11-07

REVISION LEVEL
B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS, 8 X 8 MULTIPLIER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-88739
A	67268	

SHEET 1 OF 19

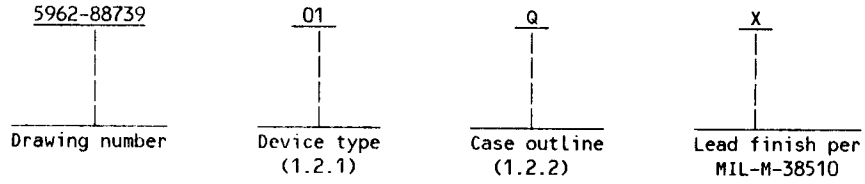
DESC FORM 193
JUL 91

5962-E461

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Multiply time
01	TMC208KV	Two's complement 8 x 8 multiplier	70 ns
02	TMC208KV1	Two's complement 8 x 8 multiplier	50 ns
03	TMC28KUV	Unsigned magnitude 8 x 8 multiplier	70 ns
04	TMC28KUV1	Unsigned magnitude 8 x 8 multiplier	50 ns
05	LMU0860	Two's complement 8 x 8 multiplier	60 ns
06	LMU0845	Two's complement 8 x 8 multiplier	45 ns
07	LMU8U60	Unsigned magnitude 8 x 8 multiplier	60 ns
08	LMU8U45	Unsigned magnitude 8 x 8 multiplier	45 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package
X	C-5 (44-lead, .662" x .662" x .120"), leadless chip carrier

1.3 Absolute maximum ratings.

Supply voltage (V_{DD})	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs	
Devices 01,02,03,04	-0.5 V dc to V_{DD} + 0.5 V dc
Devices 05,06,07,08	-3.0 V dc to +7.0 V dc
DC input voltage:	
Devices 01,02,03,04	-0.5 V dc to V_{DD} + 0.5 V dc
Devices 05,06,07,08	-3.0 V dc to +7.0 V dc
Maximum power dissipation 1/	550 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	+4.5 V dc to +5.5 V dc
Output high current (I_{OH})	-2.0 mA maximum
Output low current (I_{OL})	
Devices 01, 02, 03, 04	4.0 mA maximum
Devices 05, 06, 07, 08	8.0 mA maximum
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Input/output data format. The input/output data format shall be as specified on figure 2.

3.2.4 Block diagram. The functional block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified 1/		Device types	Group A subgroups	Limits		Unit
						Min	Max	
Output high voltage	V_{OH}	V_{DD} = 4.5 V, I_{OH} = -2.0 mA		01,02, 03,04	1,2,3	2.4		V
				05,06, 07,08	1,2,3	3.5		V
Output low voltage	V_{OL}	V_{DD} = 4.5 V	I_{OL} = 4.0 mA	01,02, 03,04	1,2,3		0.4	V
			I_{OL} = 8.0 mA	05,06, 07,08	1,2,3		0.5	V
Input high voltage	V_{IH}	V_{DD} = 5.5 V		01,02, 03,04	1,2,3	2.0		V
				05,06, 07,08	1,2,3	2.0		V
Input low voltage	V_{IL}	V_{DD} = 5.5 V		01,02, 03,04	1,2,3		0.8	V
				05,06, 07,08	1,2,3		0.8	V
Input low current	I_{IL}	V_{DD} = 5.5 V V_{IN} = 0 V		01,02, 03,04	1,2,3		-10	µA
				05,06, 07,08	1,2,3		-20	µA
Input high current	I_{IH}	V_{DD} = 5.5 V V_{IN} = V_{DD}		01,02, 03,04	1,2,3		+10	µA
				05,06, 07,08	1,2,3		+20	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified 1/		Device types	Group A subgroups	Limits		Unit
						Min	Max	
Output leakage current, low	I_{OZL}	V_{DD} = 5.5 V V_{IN} = 0 V		01,02, 03,04	1,2,3		-40	µA
				05,06, 07,08	1,2,3		-20	µA
Output leakage current, high	I_{OZH}	V_{DD} = 5.5 V V_{IN} = V_{DD}		01,02, 03,04	1,2,3		+40	µA
				05,06, 07,08	1,2,3		+20	µA
Output short circuit current 2/ 3/	I_{OS}	V_{DD} = 5.5 V		01,02, 03,04	1,2,3		-100	mA
				05,06, 07,08	1,2,3		-125	mA
Supply current, quiescent	I_{DDQ}	V_{DD} = 5.5 V	V_{IN} = 0 V	01,02, 03,04	1,2,3		5	mA
			4/	05,06, 07,08	1,2,3		1.0	mA
Supply current, dynamic	I_{DDU}	V_{DD} = 5.5 V; TRIM, TRIL = 5.0 V; F = 10 MHz		01,02, 03,04	1,2,3		50	mA
		V_{DD} = 5.5 V; TRIM, TRIL = 5.0 V; F = 22 MHz		01,02, 03,04	1,2,3		100	mA
	I_{DD}	V_{DD} = 5.5 V, F = 5 MHz, TRIM, TRIL = 5.0 V		05,06, 07,08	1,2,3		24	mA
Input capacitance	C_{IN}	f = 1.0 MHz TC = +25°C See 4.3.1c		All	4		10	pF
Output capacitance	C_{OUT}						10	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified 1/	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Functional testing 5/		V_{DD} = 4.5, 5.5 V See 4.3.1d	All	7,8			
Multiply accumulate time	t_{MPY}	See figure 4 5/ V_{DD} = 4.5 V C_L = 20 pF	01,03	9,10,11		70	ns
			02,04	10		50	ns
			05,07	9,10,11		60	ns
			06,08	9,10,11		45	ns
Output delay	t_D		01,03	9,10,11		45	ns
			02,04	10		30	ns
			05,06, 07,08	9,10,11		22	ns
Input setup time	t_S		01,03	9,10,11	30		ns
			02,04	10	25		ns
			05,06, 07,08	9,10,11	15		ns
Input hold time 3/	t_H		All	9,10,11	0		ns
Clock pulse width, high	t_{PWH}		01,02, 03,04	9,10,11	15		ns
			05,07	9,10,11	20		ns
			06,08	9,10,11	15		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified 1/	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Clock pulse width, low	t_{PWL}	Not shown 5/ V_{DD} = 4.5 V C_L = 20 pF	01,02, 03,04	9,10,11	15		ns
			05,07	9,10,11	20		ns
			06,08	9,10,11	15		ns
Three-state output enable time	t_{ENA}	See figure 4 5/ V_{DD} = 4.5 V C_L = 20 pF	01,03	9,10,11		45	ns
			02,04	10		25	ns
			05,06, 07,08	9,10,11		24	ns
Three-state output disable time	t_{DIS}		01,03	9,10,11		45	ns
			02,04	10		25	ns
			05,06, 07,08	9,10,11		22	ns

1/ Unless otherwise specified, all testing shall be conducted under worst-case conditions.

2/ One output to ground, 1 second duration maximum, output high.

3/ Guaranteed, if not tested, to the specified limits.

4/ Tested with all inputs within 0.1 V of V_{DD} or ground, no load.

5/ All transitions are measured at a 1.5 V level except t_{DIS} and t_{ENA}.

Device types	All						
Case outline	Q						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	P_{10}	11	P_3	21	X_6	31	Y_4
2	P_9	12	P_2	22	X_7	32	GND
3	P_8	13	P_1	23	CLK X	33	Y_5
4	CLK P	14	P_0	24	CLK Y	34	Y_6
5	TRIM	15	X_0	25	RND	35	Y_7
6	TRIL	16	X_1	26	Y_0	36	P_{15}
7	P_7	17	X_2	27	Y_1	37	P_{14}
8	P_6	18	X_3	28	Y_2	38	P_{13}
9	P_5	19	X_4	29	Y_3	39	P_{12}
10	P_4	20	X_5	30	V_{DD}	40	P_{11}

FIGURE 1. Terminal connections.

Device types	All						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	P_{10}	12	P_3	23	X_6	34	Y_4
2	P_9	13	P_2	24	X_7	35	GND
3	P_8	14	P_1	25	CLK X	36	Y_5
4	CLK P	15	P_0	26	CLK Y	37	Y_6
5	TRIM	16	X_0	27	RND	38	Y_7
6	NC	17	NC	28	NC	39	NC
7	TRIL	18	X_1	29	Y_0	40	P_{15}
8	P_7	19	X_2	30	Y_1	41	P_{14}
9	P_6	20	X_3	31	Y_2	42	P_{13}
10	P_5	21	X_4	32	Y_3	43	P_{12}
11	P_4	22	X_5	33	V_{DD}	44	P_{11}

FIGURE 1. Terminal connections - Continued.

Fractional two's complement notation

Binary point

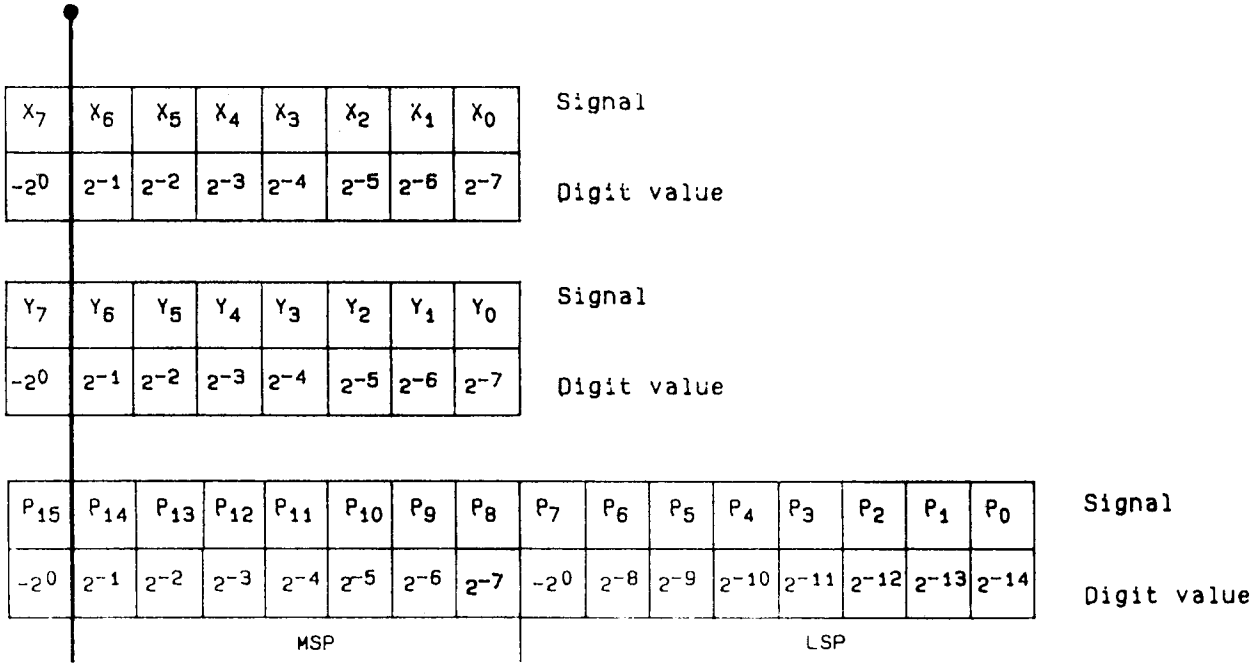


FIGURE 2. Input/output data format.

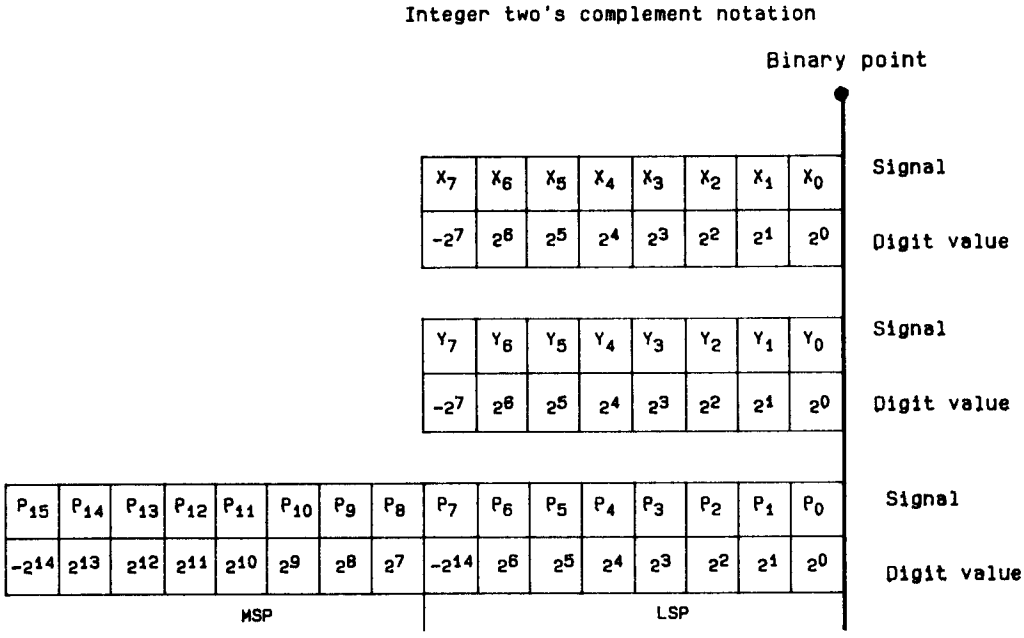


FIGURE 2. Input/output data format - Continued.

Fractional unsigned magnitude notation

Binary point

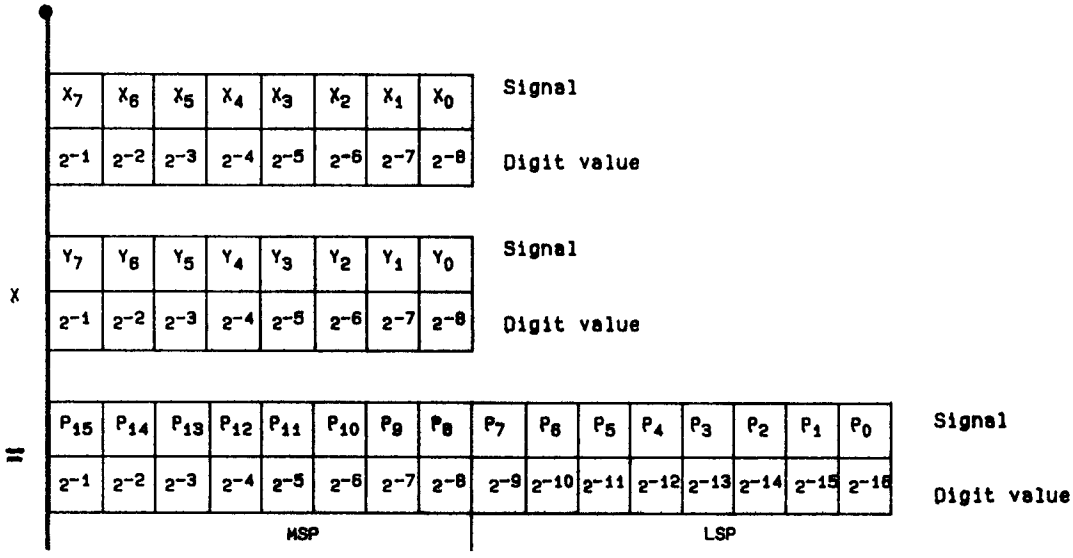


FIGURE 2. Input/output data format - Continued.

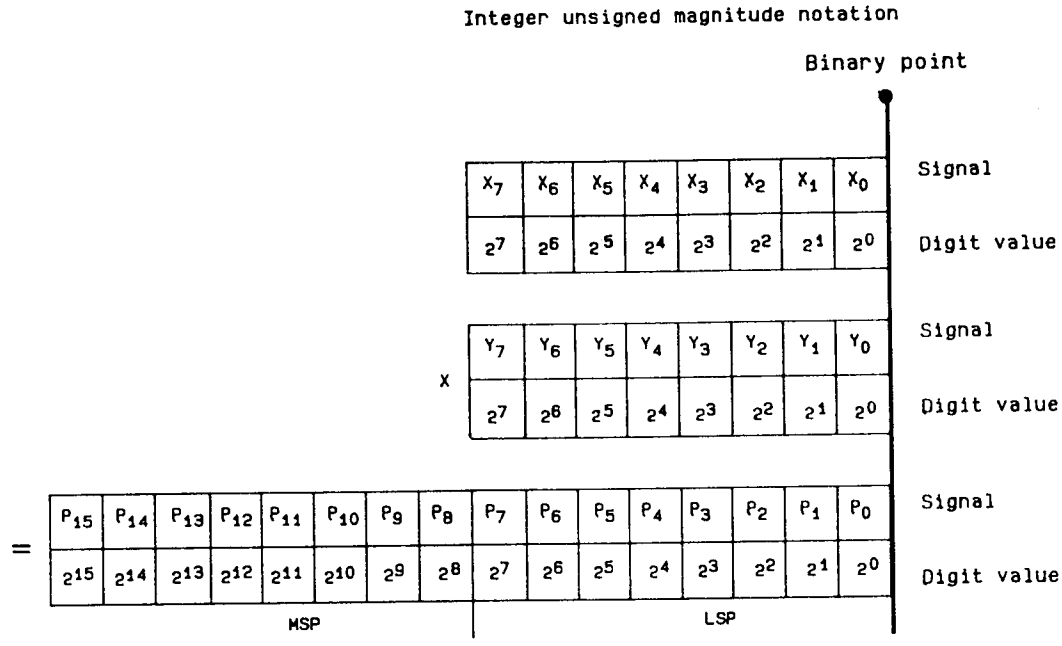


FIGURE 2. Input/output data format - Continued.

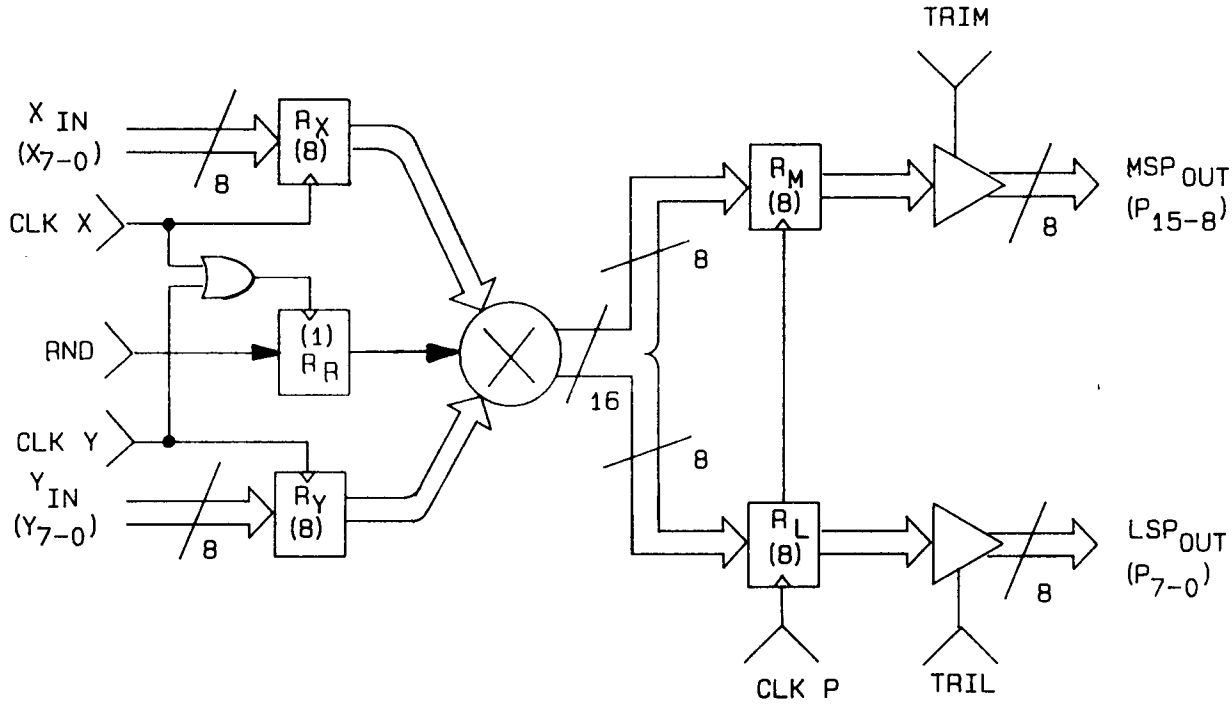


FIGURE 3. Block diagram.

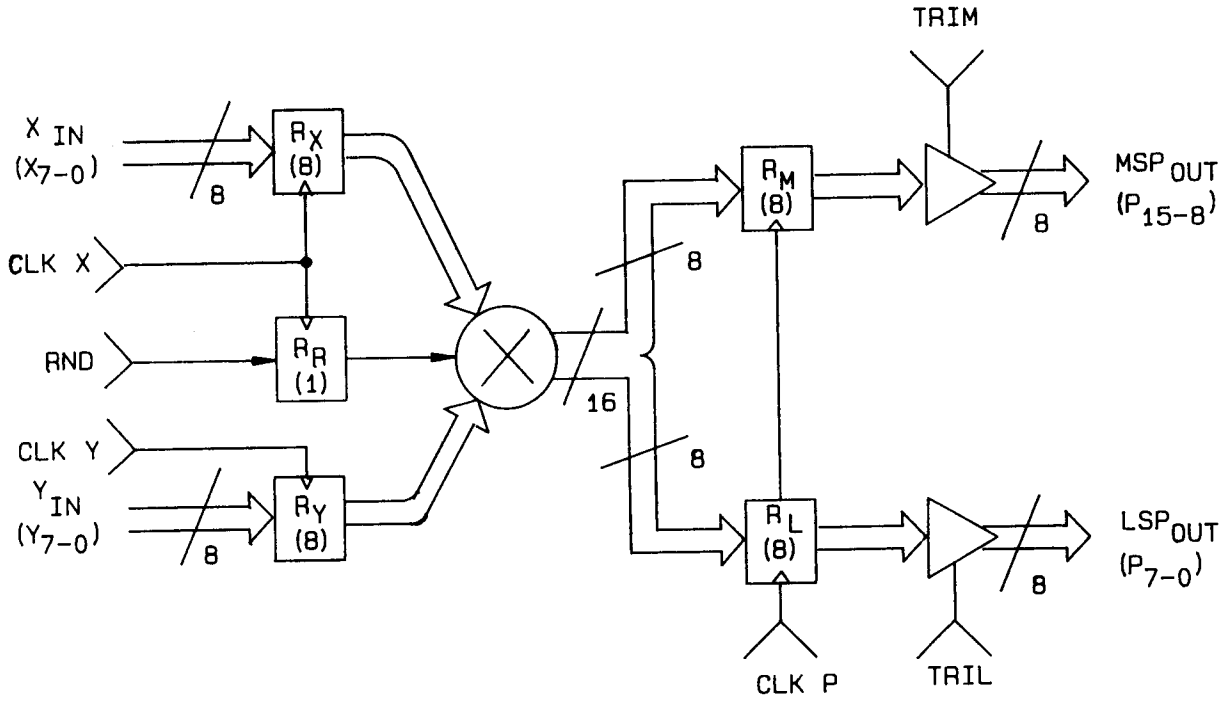
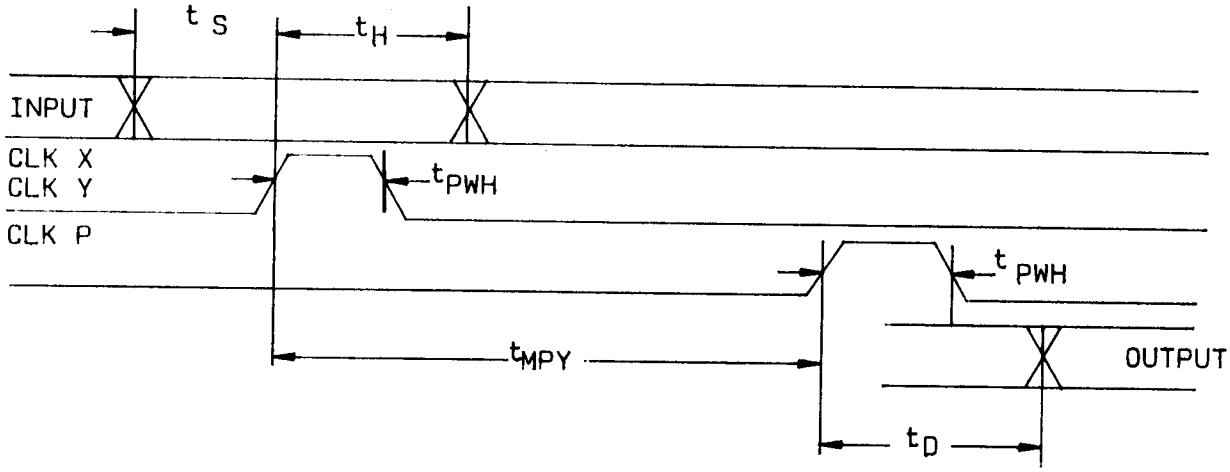
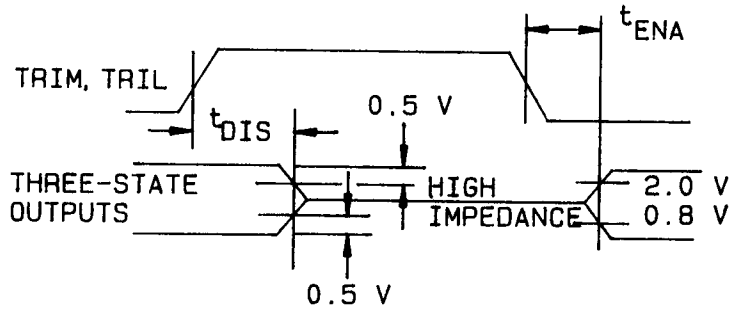


FIGURE 3. Block diagram - Continued.





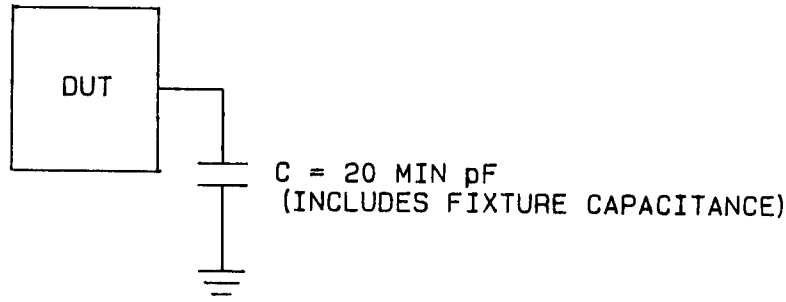


FIGURE 4. Waveforms and test circuit.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*, 8,9,10,11
Group A test requirements (method 5005)	1,2,3,4,7, 8,9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,7,9

* PDA applies to subgroups 1 and 7.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of five devices with zero rejects shall be required.

d. Subgroups 7 and 8 shall consist of verifying the functionality of the device.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.5 Pin descriptions. See table III.

6.6 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8526.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.

TABLE III. Pin descriptions.

Pin	Description
V_{DD}, GND	The devices operate from a single +5 volt supply. All power and ground lines must be connected.
X_{7-0}	Devices 01, 02, 05, and 06 have two 8-bit two's complement data inputs labeled X and Y.
Y_{7-0}	Devices 03, 04, 07, and 08 have two 8-bit unsigned magnitude data inputs labeled X and Y. The most significant bits (MSB's) X_7 and Y_7, carry the sign information for the two's complement notation in devices 01, 02, 05, and 06. The remaining bits are X_{6-0} and Y_{6-0} with X_0 and Y_0 the LSB's. The input and output formats for fractional and integer two's complement, and fractional and integer unsigned magnitude notations are shown on figure 2.
P_{15-0}	Devices 01, 02, 05, and 06 have a 16-bit two's complement output which is the product of the two input X and Y values. Devices 03, 04, 07, and 08 have a 16-bit unsigned magnitude output which is the product of the two input X and Y values. This output is divided into two 8-bit output words, the MSP and LSP. The MSB of both the MSP and LSP is the sign bit in devices 01, 02, 05, and 06. The input and output formats for fractional and integer two's complement, and fractional and integer unsigned magnitude notations are shown on figure 2. Note that since +1 cannot be exactly represented in fractional two's complement notation, some provision for handling the case (-1)*(-1) must be made. Devices 01, 02, 05, and 06 output a -1 in this case. As a result, external error handling provisions may be required.
CLK X, CLK Y, CLK P	These devices have three clock lines, one for each input register (CLK X and CLK Y) and one for the product register (CLK P). Data present at the inputs of these registers are loaded into the registers on the rising edge of the appropriate clock. In devices 01, 02, 05, and 06, the RND input is registered and clocked in on the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally high clock signals are used. Problems with loading this control signal can be avoided by the use of normally low clocks. In devices 03, 04, 07, and 08, the RND input is registered and clocked in on the rising edge of CLK X.
TRIM, TRIL	TRIM and TRIL are the three-state enable lines for the MSP and the LSP. The output driver is in the high impedance state when TRIM or TRIL is high, and enabled when low. TRIM and TRIL are not registered.
RND	When RND (round) is high, one is added to the MSB of the LSP. A one will be added to the P_6 bit in devices 01, 02, 05, and 06, or the P_7 bit in devices 03, 04, 07, and 08. Note that rounding always occurs in the positive direction. In some applications, this may introduce a systematic bias. The RND input is registered and used when a rounded 8-bit product is desired.