| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Add the F-9 and F-10 packages to the drawing, also added vendor CAGE number 65786 to the drawing. Changes to table I, figure 1, and 6.4. Also added paragraph 4.3.3 to drawing. Editorial changes throughout. | 1989 JAN 27 | DRC |

| REV | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SHEET | | | | | | | | | | | | | | | | | | | | | | | | |
| REV | | | | | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | | | | | |

| REV STATUS OF SHEETS | REV | A | A | | A | A | A | A | A | A | A | A | A | | | | | | A | A | A | A |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 |

PMIC N/A

**STANDARDIZED MILITARY DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: James E. Jamison

CHECKED BY: Ray Monnin

APPROVED BY: DRC

DRAWING APPROVAL DATE: 15 APRIL 1988

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS 64 X 5 PARALLEL FIFO, MONOLITHIC SILICON

| SIZE | CAGE CODE | |
|---|---|---|
| A | 67268 | 5962-86846 |

SHEET 1 OF 21

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1097

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

| 5962-86846 | 01 | V | X |
|---|---|---|---|
| Drawing number | Device type (1.2.1) | Case outline (1.2.2) | Lead finish per MIL-M-38510 |

1.2.1 Device type. The device type shall identify the circuit function as follows:

| Device type | Generic number | Circuit function | Shift in/out rate |
|---|---|---|---|
| 01 | (See 6.4) | 64 x 5 CMOS parallel FIFO | 10 MHz |
| 02 | (See 6.4) | 64 x 5 CMOS parallel FIFO | 15 MHz |
| 03 | (See 6.4) | 64 x 5 CMOS parallel FIFO | 25 MHz |
| 04 | (See 6.4) | 64 x 5 CMOS parallel FIFO | 35 MHz |

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

| Outline letter | Case outline |
|---|---|
| S | F-9 (20-lead, .540" x .300" x .100"), flat package |
| V | D-6 (18-lead, .960" x .310" x .200"), dual-in-line package |
| 2 | C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package |
| X | F-10 (18-lead, .540" x .370" x .092"), flat package |

1.3 Absolute maximum ratings.

| | |
|---|---|
| Terminal voltage with respect to ground | -0.5 V dc to +7.0 V dc |
| DC output current | 50 mA |
| Storage temperature range | -65°C to +150°C |
| Maximum power dissipation ($P_D$) 1/ | 1.0 W |
| Lead temperature (soldering, 10 seconds) | +260°C |
| Thermal resistance, junction-to-case ($\theta_{JC}$): Cases S, V, X, and 2 | See MIL-M-38510, appendix C |
| Junction temperature ($T_J$) | +175°C |

1.4 Recommended operating conditions.

| | |
|---|---|
| Supply voltage ($V_{CC}$) | 4.5 V dc to 5.5 V dc |
| Supply voltage (GND) | 0 V dc |
| Input high voltage ($V_{IH}$) | 2.0 V dc minimum |
| Input low voltage ($V_{IL}$) | 0.8 V dc maximum 2/ |
| Case operating temperature range ($T_C$) | -55°C to +125°C |

1/ Must withstand the added $P_D$ due to short-circuit, test e.g., $I_{OS}$.
2/ -1.5 V undershoots are allowed for 10 ns once per cycle.



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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The block diagram shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions<br>$-55°C < T_C < +125°C$<br>$V_{CC}$ = 4.5 V to 5.5 V<br>unless otherwise specified | Group A subgroups | Device types | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Input low current | $I_{IL}$ | 0 V ≤ $V_{IN}$ ≤ 5.5 V, $V_{CC}$ = 5.5 V | 1, 2, 3 | All | -10 | | µA |
| Input high current | $I_{IH}$ | 0 V ≤ $V_{IN}$ ≤ 5.5 V, $V_{CC}$ = 5.5 V | 1, 2, 3 | All | | +10 | µA |
| Output low voltage | $V_{OL}$ | $V_{CC}$ = 4.5 V, $I_{OL}$ = 8.0 mA<br>$V_{IL}$ = 0.8 V, $V_{IH}$ = 2.0 V | 1, 2, 3 | All | | 0.4 | V |
| Output high voltage | $V_{OH}$ | $V_{CC}$ = 4.5 V, $I_{OH}$ = -4.0 mA<br>$V_{IL}$ = 0.8 V, $V_{IH}$ = 2.0 V | 1, 2, 3 | All | 2.4 | | V |
| Output short-circuit current 1/ | $I_{OS}$ | $V_{CC}$ = 5.5 V, $V_O$ = 0 V | 1, 2, 3 | All | -20 | -90 | mA |
| Off-state output high current | $I_{HZ}$ | $V_{CC}$ = 5.5 V, $V_O$ = 2.4 V | 1, 2, 3 | All | | +50 | µA |
| Off-state output low current | $I_{LZ}$ | $V_{CC}$ = 5.5 V, $V_O$ = 0.4 V | 1, 2, 3 | All | -50 | | µA |
| Operating supply current | $I_{CC}$ | Inputs = $V_{IH}$<br>outputs open | 1, 2, 3 | All | | 90 | mA |
| Input capacitance | $C_{IN}$ | $V_{IN}$ = 0 V, f = 1.0 MHz,<br>$T_A$ = +25°C, see 4.3.1c | 4 | All | | 7.0 | pF |
| Output capacitance | $C_{OUT}$ | $V_{OUT}$ = 0 V, f = 1.0 MHz,<br>$T_A$ = +25°C, see 4.3.1c | 4 | All | | 7.0 | pF |
| Functional test | | See 4.3.1d | 7, 8 | All | | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 4.5$ V to 5.5 V unless otherwise specified | Group A subgroups | Device types | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| Shift in rate | $f_{IN}$ | See figures 3 and 4 2/ | 9, 10, 11 | 01 | | 10 | MHz |
| | | | | 02 | | 15 | MHz |
| | | | | 03 | | 25 | MHz |
| | | | | 04 | | 35 | MHz |
| Shift in to input ready low 3/ | $t_{IRL}$ | See figures 3 and 4 2/ | 9, 10, 11 | 01 | | 40 | ns |
| | | | | 02 | | 35 | ns |
| | | | | 03 | | 22 | ns |
| | | | | 04 | | 18 | ns |
| Shift in to input ready high 3/ | $t_{IRH}$ | See figures 3 and 4 2/ | 9, 10, 11 | 01 | | 45 | ns |
| | | | | 02 | | 40 | ns |
| | | | | 03 | | 30 | ns |
| | | | | 04 | | 20 | ns |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions<br>$-55°C < T_C < +125°C$<br>$V_{CC}$ = 4.5 V to 5.5 V<br>unless otherwise specified | Group A subgroups | Device types | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Shift out rate | $f_{OUT}$ | See figures 3 and 5 2/ | 9, 10, 11 | 01 | | 10 | MHz |
| | | | | 02 | | 15 | MHz |
| | | | | 03 | | 25 | MHz |
| | | | | 04 | | 35 | MHz |
| Shift out to output ready low 3/ | $t_{ORL}$ | See figures 3 and 5 2/ | 9, 10, 11 | 01 | | 40 | ns |
| | | | | 02 | | 35 | ns |
| | | | | 03 | | 21 | ns |
| | | | | 04 | | 18 | ns |
| Shift out to output ready high 3/ | $t_{ORH}$ | See figures 3 and 5 2/ | 9, 10, 11 | 01 | | 55 | ns |
| | | | | 02 | | 40 | ns |
| | | | | 03 | | 37 | ns |
| | | | | 04 | | 20 | ns |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C < T_C < +125°C$ $V_{CC} = 4.5$ V to 5.5 V unless otherwise specified | Group A subgroups | Device types | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| Output data hold (previous word) 4/ | $t_{ODH}$ | See figures 3 and 5 2/ | 9, 10, 11 | 01, 02 | 5.0 | | ns |
| | | | | 03, 04 | 5.0 | | ns |
| Output data shift (next word) | $t_{ODS}$ | See figures 3 and 5 2/ 5/ | 9, 10, 11 | 01, 02 | | 55 | ns |
| | | | | 03 | | 37 | ns |
| | | | | 04 | | 25 | ns |
| Data throughput or "fall through" 4/ | $t_{PT}$ | See figures 3, 6, and 7 2/ | 9, 10, 11 | 01, 02 | | 65 | ns |
| | | | | 03 | | 60 | ns |
| | | | | 04 | | 28 | ns |
| $\overline{\text{MASTER}}$ $\overline{\text{RESET}}$ to OR low | $t_{MRORL}$ | See figures 3 and 8 2/ | 9, 10, 11 | 01 | | 40 | ns |
| | | | | 02, 03 | | 35 | ns |
| | | | | 04 | | 28 | ns |
| $\overline{\text{MASTER}}$ $\overline{\text{RESET}}$ to IR high 4/ | $t_{MRIRH}$ | See figures 3 and 8 2/ | 9, 10, 11 | 01 | | 40 | ns |
| | | | | 02, 03 | | 35 | ns |
| | | | | 04 | | 28 | ns |

See footnotes at end of table.



☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—550-547

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C < T_C < +125°C$ $V_{CC} = 4.5$ V to 5.5 V unless otherwise specified | Group A subgroups | Device types | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| MASTER RESET to data output low | $t_{MRQ}$ | See figures 3 and 8 2/ | 9, 10, 11 | 01 | | 40 | ns |
| | | | | 02 | | 35 | ns |
| | | | | 03 | | 25 | ns |
| | | | | 04 | | 20 | ns |
| Output valid from $\overline{OE}$ low | $t_{OOE}$ | See figures 3 and 9 2/ | 9, 10, 11 | 01 | | 35 | ns |
| | | | | 02 | | 30 | ns |
| | | | | 03 | | 20 | ns |
| | | | | 04 | | 15 | ns |
| Output high impedance from $\overline{OE}$ high 4/ | $t_{HZOE}$ | See figures 3 and 9 2/ | 9, 10, 11 | 01 | | 30 | ns |
| | | | | 02 | | 25 | ns |
| | | | | 03 | | 15 | ns |
| | | | | 04 | | 12 | ns |
| Input ready pulse high 4/ 5/ | $t_{IPH}$ | See figures 3 and 6 2/ | 9, 10, 11 | 01,02,03 | 10 | | ns |
| | | | | 04 | 5.0 | | ns |

See footnotes at end of table.



☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—550-547

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C < T_C < +125°C$ $V_{CC} = 4.5$ V to 5.5 V unless otherwise specified | Group A subgroups | Device types | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Output ready pulse high 4/ 5/ | $t_{OPH}$ | See figures 3 and 7 2/ | 9, 10, 11 | 01,02,03 | 10 | | ns |
| | | | | 04 | 5.0 | | ns |
| Shift in high time 3/ | $t_{SIH}$ | See figures 3 and 4 2/ | 9, 10, 11 | 01, 02 | 20 | | ns |
| | | | | 03 | 11 | | ns |
| | | | | 04 | 9.0 | | ns |
| Shift in low time | $t_{SIL}$ | See figures 3 and 4 2/ | 9, 10, 11 | 01 | 30 | | ns |
| | | | | 02 | 25 | | ns |
| | | | | 03 | 24 | | ns |
| | | | | 04 | 17 | | ns |
| Input data setup time | $t_{IDS}$ | See figures 3 and 4 2/ | 9, 10, 11 | All | 0 | | ns |
| Input data hold time | $t_{IDH}$ | See figures 3 and 4 2/ | 9, 10, 11 | 01 | 40 | | ns |
| | | | | 02 | 30 | | ns |
| | | | | 03 | 20 | | ns |
| | | | | 04 | 15 | | ns |

See footnotes at end of table.



☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—550-547

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 4.5\ V$ to $5.5\ V$ unless otherwise specified | Group A subgroups | Device types | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Shift out high time 3/ | $t_{SOH}$ | See figures 3 and 5 2/ | 9, 10, 11 | 01, 02 | 20 | | ns |
| | | | | 03 | 11 | | ns |
| | | | | 04 | 9.0 | | ns |
| Shift out low time | $t_{SOL}$ | See figures 3 and 5 2/ | 9, 10, 11 | 01 | 30 | | ns |
| | | | | 02 | 25 | | ns |
| | | | | 03 | 24 | | ns |
| | | | | 04 | 17 | | ns |
| MASTER RESET pulse width | $t_{MRW}$ | See figures 3 and 8 2/ | 9, 10, 11 | 01 | 30 | | ns |
| | | | | 02,03,04 | 25 | | ns |
| MASTER RESET pulse to SI 4/ | $t_{MRS}$ | See figures 3 and 8 2/ | 9, 10, 11 | 01 | 35 | | ns |
| | | | | 02 | 25 | | ns |
| | | | | 03, 04 | 10 | | ns |

See footnotes at end of table.



☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—550-547

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 4.5$ V to 5.5 V unless otherwise specified | Group A subgroups | Device types | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| Data setup to IR 4/ | $t_{SIR}$ | See figures 3 and 6 2/ | 9, 10, 11 | 01,02,03 | 5.0 | | ns |
| | | | | 04 | 3.0 | | ns |
| Data hold from IR 4/ | $t_{HIR}$ | See figures 3 and 6 2/ | 9, 10, 11 | 01, 02 | 30 | | ns |
| | | | | 03 | 20 | | ns |
| | | | | 04 | 15 | | ns |
| Data setup to OR high 4/ | $t_{SOR}$ | See figures 3 and 7 2/ | 9, 10, 11 | All | 0 | | ns |

1/ Not more than one output should be shorted at a time. Duration of the short-circuit condition should not exceed one second.

2/ AC measurements assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V and output loading of 30 pF load capacitance. Output timing reference is 1.5 V.

3/ Since these devices are very high speed, care must be exercised in the design of the hardware and timing utilized in the design. Device grounding and decoupling are crucial to correct operation as the device will respond to very small glitches due to long reflective lines, high capacitances or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1 µF directly between $V_{CC}$ and GND with very short lead lengths is recommended.

4/ May not be tested, but shall be guaranteed to the limits specified in table I.

5/ This parameter applies to devices communicating with each other in a cascaded mode.



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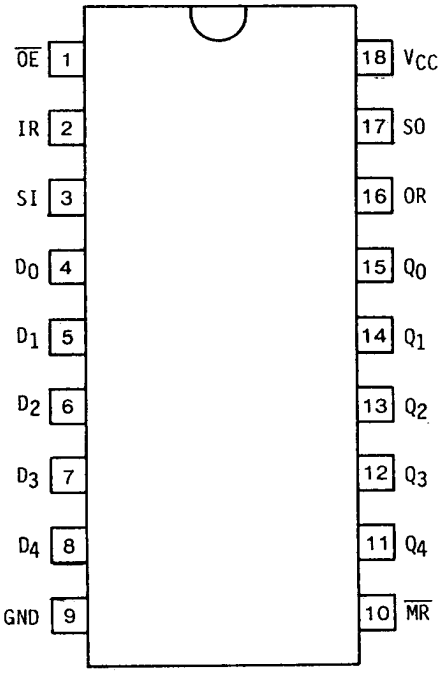
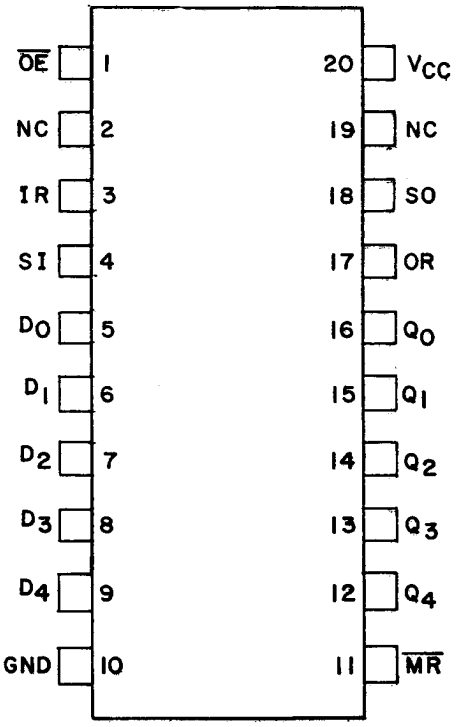
Device types 01 - 04

Cases V and X




Case S




Case 2

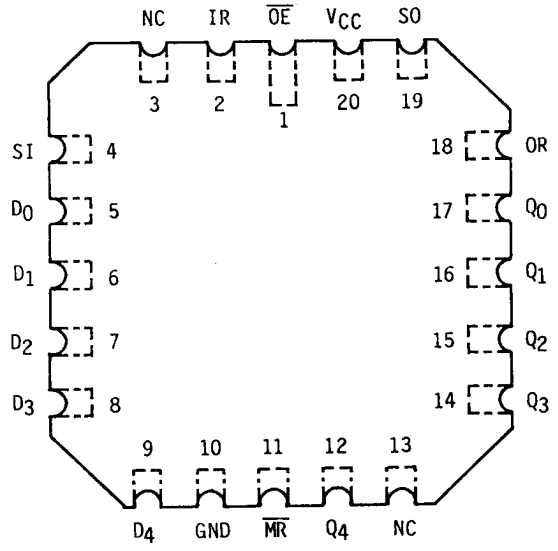



FIGURE 1. Terminal connections (top view).

| STANDARDIZED MILITARY DRAWING<br>DEFENSE ELECTRONICS SUPPLY CENTER<br>DAYTON, OHIO 45444 | SIZE<br>A | | 5962-86846 |
|---|---|---|---|
| | | REVISION LEVEL A | SHEET 12 |

Device types 01 - 04

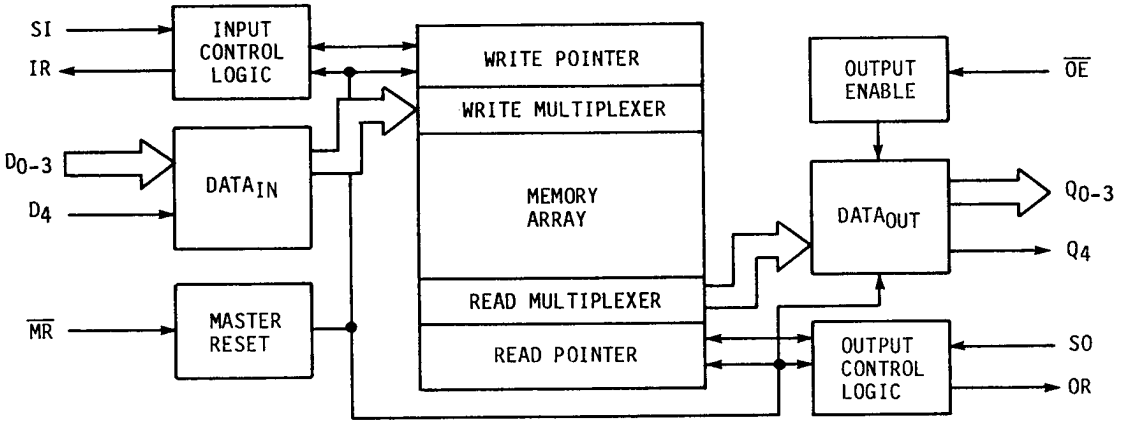
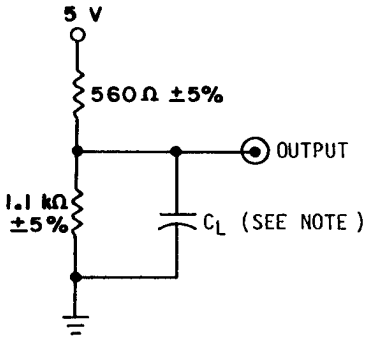



FIGURE 2. Block diagram.




NOTE: $C_L$ = 5.0 pF maximum for $t_{HZOE}$ and $t_{OOE}$ and $C_L$ = 30 pF maximum for all other measurements. $C_L$ includes jig and scope capacitance.

FIGURE 3. Output load circuit.

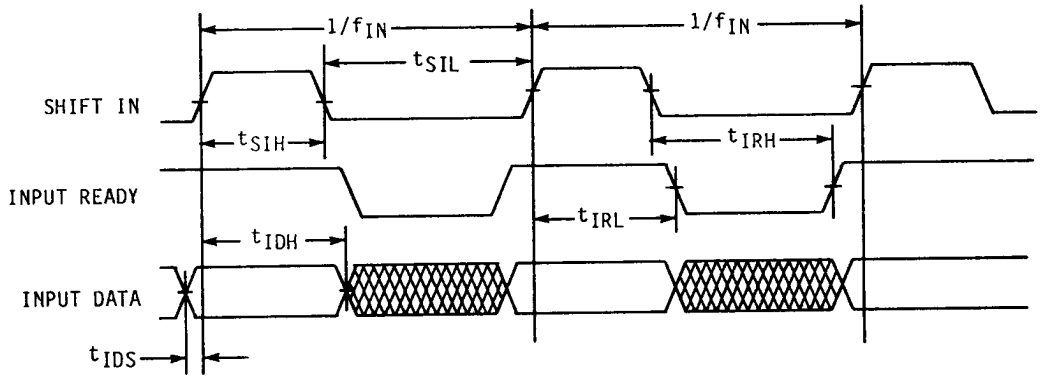
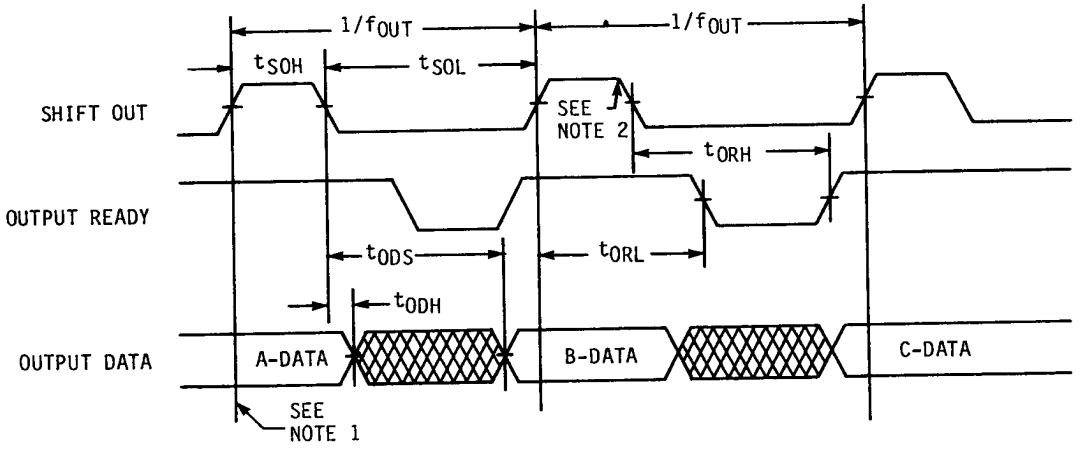


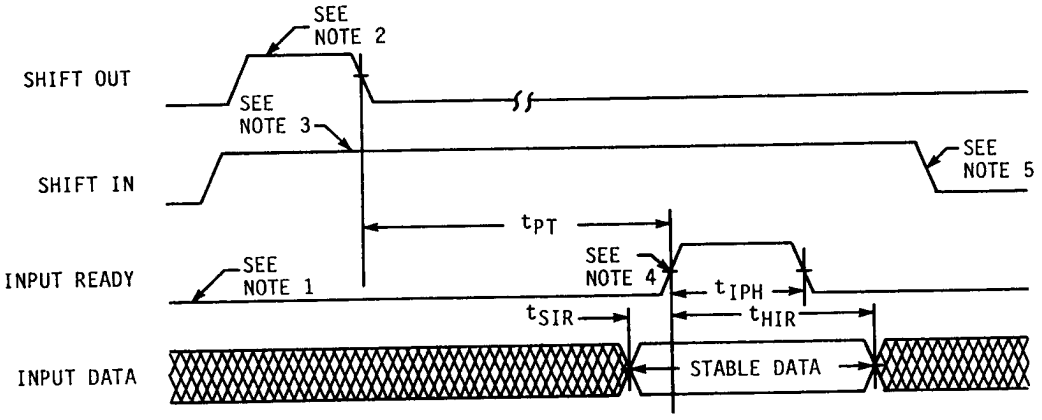

FIGURE 4. Input timing diagram.




NOTES:

1. This data is loaded consecutively, A, B, C.
2. Data is shifted out when Shift Out makes a HIGH to LOW transition.

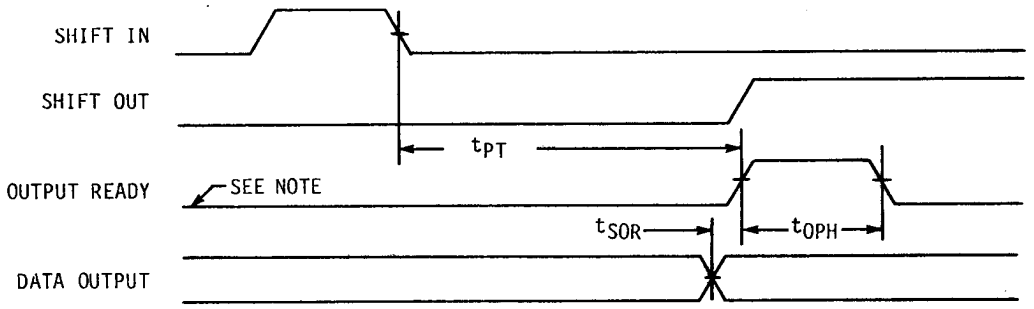
FIGURE 5. Output timing diagram.




NOTES:

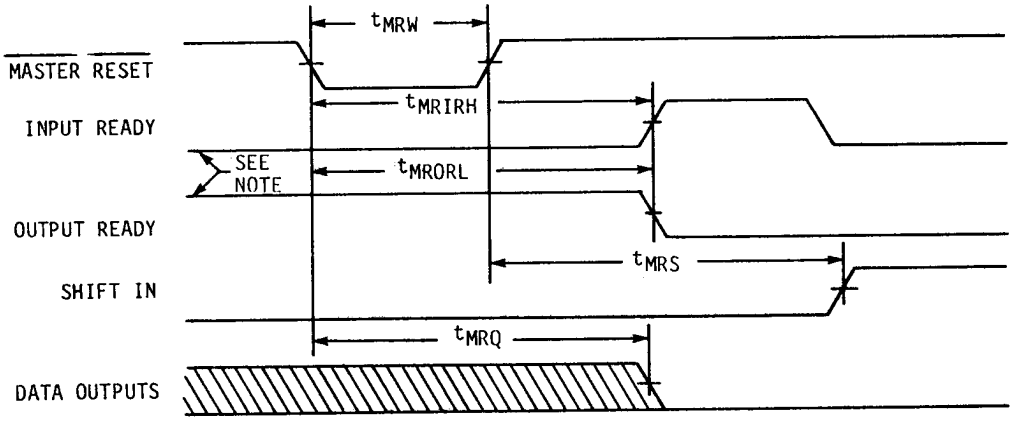
1. FIFO is initially full.
2. Shift Out pulse is applied.
3. Shift In is held HIGH.
4. As soon as input ready becomes HIGH the input data is loaded into the FIFO.
5. The write pointer is incremented.

FIGURE 6. $t_{IPH}$, $t_{HIR}$ and $t_{SIR}$ timing diagram.



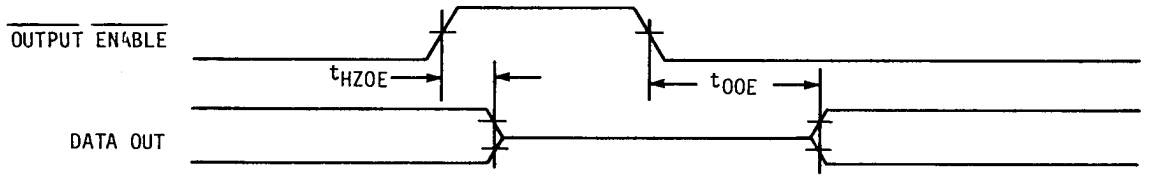

NOTE: FIFO initially empty

FIGURE 7. $t_{PT}$ and $t_{OPH}$ timing diagram.




NOTE: Worst case, FIFO initially full.

FIGURE 8. Master RESET timing.




NOTE: High-Z transitions are referenced to the steady-state $V_{OH}$ - 500 mV and $V_{OL}$ + 500 mV levels on the output.

FIGURE 9. Output enable timing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 ($C_{IN}/C_{OUT}$ measurements) shall be measured for initial device characterization and after any process or design changes which may affect capacitance. Sample size is fifteen devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 tests shall be sufficient to verify the functional operation of the device. It forms a part of the vendor's test tape and shall be maintained and available from the approved source of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) $T_A$ = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

| MIL-STD-883 test requirements | Subgroups (per method 5005, table I) |
|---|---|
| Interim electrical parameters (method 5004) | --- |
| Final electrical test parameters (method 5004) | 1*, 2, 3, 7*, 8, 9, 10, 11 |
| Group A test requirements (method 5005) | 1, 2, 3, 4**, 7, 8, 9, 10, 11 |
| Groups C and D end-point electrical parameters (method 5005) | 1, 2, 3, 7, 8 |

* PDA applies to subgroups 1 and 7.
** For subgroup 4, see 4.3.1c

4.3.3 Electrostatic discharge sensitivity (ESDS). Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015 and MIL-M-38510 for initial testing and after any design or process changes which may affect input or output protection circuitry. The option to categorize devices as ESD sensitive without performing the test is not allowed. Only those device types that pass ESDS testing at 1,000 volts or greater shall be considered as conforming to the requirements of this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

| Military drawing part number | Vendor CAGE number | Vendor similar part number 1/ |
|---|---|---|
| 5962-8684601VX | 61772<br>65786 | IDT72404L10DB<br>CY7C404-10MB |
| 5962-86846012X | 61772<br>65786 | IDT72404L10LB<br>CY7C404-10LMB |
| 5962-8684601SX | 61772 | IDT72404EB |
| 5962-8684601XX | 65786 | CY7C404-10FMB |
| 5962-8684602VX | 61772<br>65786 | IDT72404L15DB<br>CY7C404-15DMB |
| 5962-86846022X | 61772<br>65786 | IDT72404L15LB<br>CY7C404-15LMB |
| 5962-8684602SX | 61772 | IDT72404EB |
| 5962-8684602XX | 65786 | CY7C404-15FMB |
| 5962-8684603VX | 61772<br>65786 | IDT72404L25DB<br>CY7C404-25DMB |
| 5962-86846032X | 61772<br>65786 | IDT72404L25LB<br>CY7C404-25LMB |
| 5962-8684603SX | 61772 | IDT72404EB |
| 5962-8684603XX | 65786 | CY7C404-25FMB |
| 5962-8684604VX | 61772 | IDT72404L35DB |
| 5962-86846042X | 61772 | IDT72404L35LB |
| 5962-8684604SX | 61772 | IDT72404EB |

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 61772 | Integrated Device Technology, Incorporated<br>3236 Scott Boulevard<br>Santa Clara, CA 95052 |
| 65786 | Cypress Semiconductor Corporation<br>3901 North First Street<br>San Jose, CA 95134 |