NEC

PRELIMINARY DATA SHEET

μPD461318/36LS1

Bi-CMOS Synchronous Static Ram

MAR. 1995

Description

The μPD461318/36LS1 is a 65,536-word by 18-bit / 32,768-word by 36-bit synchronous static RAM fabricated with advanced Bi-CMOS technology using N-channel memory cell.

This technology and unique peripheral circuits make the μPD461318/36LS1 a high-speed device. The μPD461318/36LS1 is suitable for applications which require high-speed, low voltage, high-density memory and wide bit configuration, such as cache and buffer memory.

The μPD461318/36LS1 is packaged in a 119-pin plastic BGA (Ball Grid Array).

Features

- Fully Synchronous Operation
- Fast Clock Access Time

  Register-Register : 3ns / 200MHz, 3.25ns / 182MHz, 3.5ns / 166MHz, 4ns / 143MHz

  Register-Latch : 6ns / 200MHz, 6.25ns / 182MHz, 6.5ns / 166MHz, 9ns / 143MHz
- Asynchronous Output Enable Control : G\
- Byte Write control : SBa\(DQa1-9), SBb\(DQb1-9), SBc\(DQc1-9), SBd\(DQd1-9)
- Common I/O using Three-state Outputs
- Internally self-timed Write Cycle
- Late write with 1 dead cycle between Read-Write.
- User-option by Mode Select Pin

  Single Differential Clock Registered Input / Registered Output or

  Dual Differential Clock Registered Input / Latched Output
- User-configurable Outputs

  Controlled Impedance outputs or Push-Pull outputs

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64K x18 Pin Assignment

		Column 1	2	3	4	5	6	7
Row	A	VDDQ	SA12	SA9	NC	SA6	SA2	VDDQ
	B	NC	NC	NC	NC	NC	NC	NC
	C	NC	SA13	SA10	VDD	SA7	SA3	NC
	D	DQb1	NC	VSS	ZQ	VSS	DQa9	NC
	E	NC	DQb2	VSS	SS\	VSS	NC	DQa8
	F	VDDQ	NC	VSS	G\	VSS	DQa7	VDDQ
	G	NC	DQb3	SBb\	C\	VSS	NC	DQa6
	H	DQb4	NC	VSS	C	VSS	DQa5	NC
	J	VDDQ	VDD	VREF	VDD	VREF	VDD	VDDQ
	K	NC	DQb5	VSS	K	VSS	NC	DQa4
	L	DQb6	NC	VSS	K\	SBa\	DQa3	NC
	M	VDDQ	DQb7	VSS	SW\	VSS	NC	VDDQ
	N	DQb8	NC	VSS	SA1	VSS	DQa2	NC
	P	NC	DQb9	VSS	SA0	VSS	NC	DQa1
	R	NC	SA14	M1	VDD	M2	SA4	NC
	T	NC	SA15	SA11	NC	SA8	SA5	NC
	U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

Pin Names and Functions

Pin Name	Description	Function
VDD	Core Power Supply	Supplies power for RAM core
VSS	Ground	
VDDQ	Output Power Supply	Supplies power for output buffers
VREF	Input Reference	
K, K\	Main Clock	
C, C\	Data I/O Clock	Controls only data bus registers when in use
SA0~SA15	Sync. Address Input	
DQa1~DQb9	Sync. Data Input / Output	
SS\	Sync. Chip Select	Logically selects SRAM
SW\	Sync. Global Write Enable	Writes all bytes
SBa\	Sync. Byte "a" Write Enable	Write DQa1~DQa9
SBb\	Sync. Byte "b" Write Enable	Write DQb1~DQb9
G\	Async. Output Enable	Asynchronous Input
ZQ	Output Impedance Control	
M1, M2	Mode Select	Selects operation mode
NC	No Connect	

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32K x36 Pin Assignment

		Column 1	2	3	4	5	6	7
Row	A	VDDQ	SA12	SA9	NC	SA5	SA2	VDDQ
	B	NC	NC	NC	NC	NC	NC	NC
	C	NC	SA13	SA10	VDD	SA6	SA3	NC
	D	DQc8	DQc9	VSS	ZQ	VSS	DQb9	DQb8
	E	DQc6	DQc7	VSS	SS\	VSS	DQb7	DQb6
	F	VDDQ	DQc5	VSS	G\	VSS	DQb5	VDDQ
	G	DQc3	DQc4	SBc\	C\	SBb\	DQb4	DQb3
	H	DQc1	DQc2	VSS	C	VSS	DQb2	DQb1
	J	VDDQ	VDD	VREF	VDD	VREF	VDD	VDDQ
	K	DQd1	DQd2	VSS	K	VSS	DQa2	DQa1
	L	DQd3	DQd4	SBd\	K\	SBa\	DQa4	DQa3
	M	VDDQ	DQd5	VSS	SW\	VSS	DQa5	VDDQ
	N	DQd6	DQd7	VSS	SA1	VSS	DQa7	DQa6
	P	DQd8	DQd9	VSS	SA0	VSS	DQa9	DQa8
	R	NC	SA14	M1	VDD	M2	SA4	NC
	T	NC	NC	SA11	SA8	SA7	NC	NC
	U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

Pin Names and Functions

Pin Name	Description	Function
VDD	Core Power Supply	Supplies power for RAM core
VSS	Ground	
VDDQ	Output Power Supply	Supplies power for output buffers
VREF	Input Reference	
K, K\	Main Clock	
C, C\	Data I/O Clock	Controls only data bus registers when in use
SA0~SA14	Sync. Address Input	
DQa1~DQd9	Sync. Data Input / Output	
SS\	Sync. Chip Select	Logically Selects SRAM
SW\	Sync. Global Write Enable	Writes all bytes
SBa\	Sync. Byte "a" Write Enable	Write DQa1~DQa9
SBb\	Sync. Byte "b" Write Enable	Write DQb1~DQb9
SBc\	Sync. Byte "c" Write Enable	Write DQc1~DQc9
SBd\	Sync. Byte "d" Write Enable	Write DQd1~DQd9
G\	Async. Output Enable	Asynchronous Input
ZQ	Output Impedance Control	
M1, M2	Mode Select	Selects operation mode
NC	No Connect	

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Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Core Supply Voltage	VDD	-0.5* to 4.6	V
Output Buffer Supply Voltage	VDDQ	-0.5* to 1.6	V
Input Voltage	VIN	-0.5* to VDD+0.5	V
Input / Output Voltage	VI/O	-0.5* to VDD+0.5	V
Operating Temperature	Topr	0 to 70	°C
Storage Temperature	Tstg	-55 to 125	°C

* -1.0v Min (Pulse Width 10% Tcyc)

The device is tested under the minimum transverse air flow of 2.5 meters per second for the DC and AC specifications shown in the tables.

Recommended DC Operating Conditions (Ta=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Core Supply Voltage	VDD	3.15	3.3	3.45	V
Output Buffer Supply Voltage	VDDQ	1.14	1.2	1.26	V
Input Reference Voltage	VREF	VDDQ/2-2%		2VDDQ/3+2%	V
Input Low Voltage	VIL	-0.3*		VREF-0.1	V
Input High Voltage	VIH	VREF+0.1		VDDQ+0.3	V

* -1.0v Min (Pulse Width 10% Tcyc)

Recommended AC Operating Conditions (Ta=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Reference Voltage	VREF(RMS)	-5%		+5%	
Input Low Voltage	VIL	-0.3		VREF-0.2	V
Input High Voltage	VIH	VREF+0.2		VDDQ+0.3	V

Capacitance (Ta=25°C f=1MHz)

Parameter*	Symbol	Conditions	Max	Unit
Input Pin Capacitance	CIN	VIN=0V	5	pF
Input/Output Pin Capacitance	CI/O	VI/O=0V	7	pF
Clock Pin (K/$\overline{K}$,C/$\overline{C}$) Capacitance	CCLK	VCLK=0V	5	pF

* This parameter is sampled and not 100% tested.

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Synchronous Truth Table

SS\	SW\	SBa\	SBb\	SBc\	SBd\	Mode	DQa1-9	DQb1-9	DQc1-9	DQd1-9	Power
H	X	X	X	X	X	Not Selected	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Standby
L	H	X	X	X	X	Read	Dout	Dout	Dout	Dout	Active
L	L	L	L	L	L	Write	Din	Din	Din	Din	Active
		L	H	H	H	Write	Din	Hi-Z	Hi-Z	Hi-Z	Active
		H	L	L	L	Write	Hi-Z	Din	Din	Din	Active

Mode Select

M1	M2	ZQ	Mode
VSS	VDD	X	Single Differential Clock (K/K\ ), R / R Mode
VDD	VDD	X	Dual Differential Clock (K/K\ & C/C\ ), R / L Mode
X	X	IZQ * RQ	Controlled Impedance Push-Pull Output Buffer Mode
X	X	VDD	Push-Pull Output Buffer Mode

NOTES

1. Mode Select Pins (M1,M2) are to be tied to either VDD or VSS.
2. R / R : Registered Input / Registered Output
3. R / L : Registered Input / Latched Output

DC Characteristics (Ta=0 to 70 °C, VDD=3.3V±5%)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Input Leakage Current	ILI	VIN=0~VDD	-10		10	μA	
DQ Leakage Current	ILO	VI/O=0~VDDQ	-10		10	μA	1
Operating Supply Current	ICC	SS\=VIL Idq=0mA 200MHz			600	mA	
Output Low Voltage	VOL	|IOL|≤10uA, Fig.1	VSS		0.1	V	2, 4
Output High Voltage	VOH	|IOH|≤10uA, Fig.1	VDDQ-0.1		VDDQ	V	2, 5
Output Low Voltage	VOL	IOL=4mA, Fig.2	VSS		0.4	V	3
Output High Voltage	VOH	IOH=-4mA, Fig.2	0.8		VDDQ	V	3

NOTES

1. SS\ = VIH or G\ = VIH
2. Controlled Impedance Push-Pull Output Buffer Mode (VZQ=IZQ * RQ)
3. Push-Pull Output Buffer Mode (VZQ=VDD)
4. IOL = 2.5VDDQ/RQ+/-10% @VOL=VDDQ/2 for 200Ω ≤ RQ ≤ 400Ω
5. IOH = 2.5VDDQ/RQ+/-10% @VOH=VDDQ/2 for 200Ω ≤ RQ ≤ 400Ω

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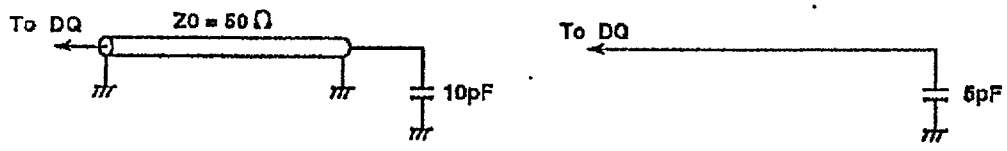
AC Test Conditions

Input Pulse Levels	VSS to 1.2V
Input Pulse Rise and Fall Time	0.5ns (10% to 90%)
Input Timing Reference Level	VREF for Single-ended Signals Cross-point for Differential Signals
Output Timing Reference Level	VTT or VDDQ/2

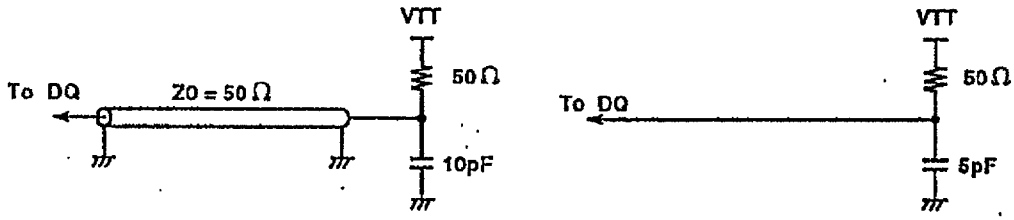
Output Test Load

Controlled Impedance Push-Pull Output Buffer Mode	Fig.1	Fig.3	
Push-Pull Output Buffer Mode	Fig.2	Fig.4	Vtt=0.6V



(a) (b)

Fig. 1



(a) (b)

Fig. 2

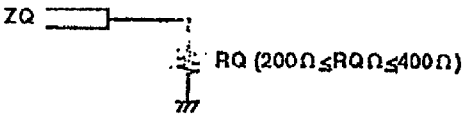


Fig. 3

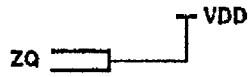


Fig. 4

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Single Differential Clock, Registered Input / Registered Output Mode

Parameter	Symbol	-5 (200MHz)		-55 (182MHz)		-6 (166MHz)		-7 (143MHz)		Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock Cycle Time	TKHKH	5.0	10	5.5	10	6.0	10	7	10	4
Clock Phase Time	TKHKL / TKLKH	2.0		2.25		2.5		3		
Setup Time Address	TAVKH	0.5		0.5		1.0		1.0		
Write Data	TDVKH	0.5		0.5		1.0		1.0		
Write Enable	TWVKH	0.5		0.5		1.0		1.0		
Chip Select	TEVKH	0.5		0.5		1.0		1.0		
Hold Time Address	TKHAX	1.5		1.5		1.5		2.0		
Write Data	TKHDX	1.5		1.5		1.5		2.0		
Write Enable	TKHWX	1.5		1.5		1.5		2.0		
Chip Select	TKHEX	1.5		1.5		1.5		2.0		
Clock Access Time	TKHQV		3		3.25		3.5		4	1
K High to Q Change	TKHQX	0.5		0.5		0.5		0.5		2
G\ Low to Q Valid	TGLQV		3		3.25		3.5		4	1
G\ Low to Q Change	TGLQX	0.5		0.5		0.5		0.5		2
G\ High to Q Hi-z	TGHQZ	0.5	3	0.5	3.25	0.5	3.5	0.5	4	2
K High to Q Hi-z	TKHQZ	0.5	3	0.5	3.25	0.5	3.5	0.5	4	2
K High to Q Lo-z	TKHQX2	0.5		0.5		0.5		0.5		
G\ High Pulse Width	TGHGL	TKHKH		TKHKH		TKHKH		TKHKH		3

Notes

1. Load Model (a)
2. Load Model (b)
3. Controlled Impedance Push-Pull Output Buffer Mode Only
4. After Power-On, 2000 cycles proper K clock input is needed before starting operation.

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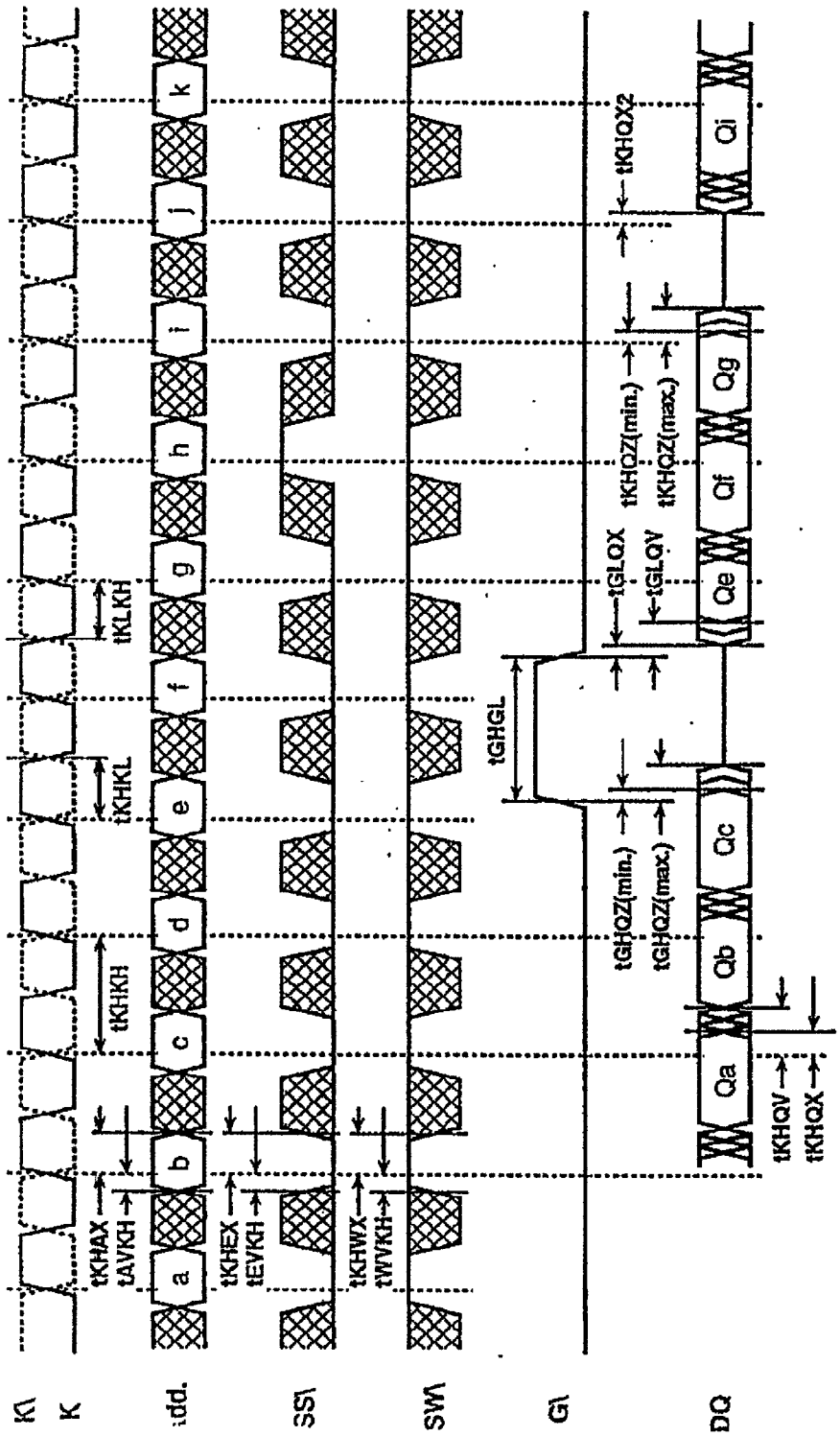
Single Differential Clock, Registered Input / Registered Output Mode (Read Operation)



6427525 0057010 019

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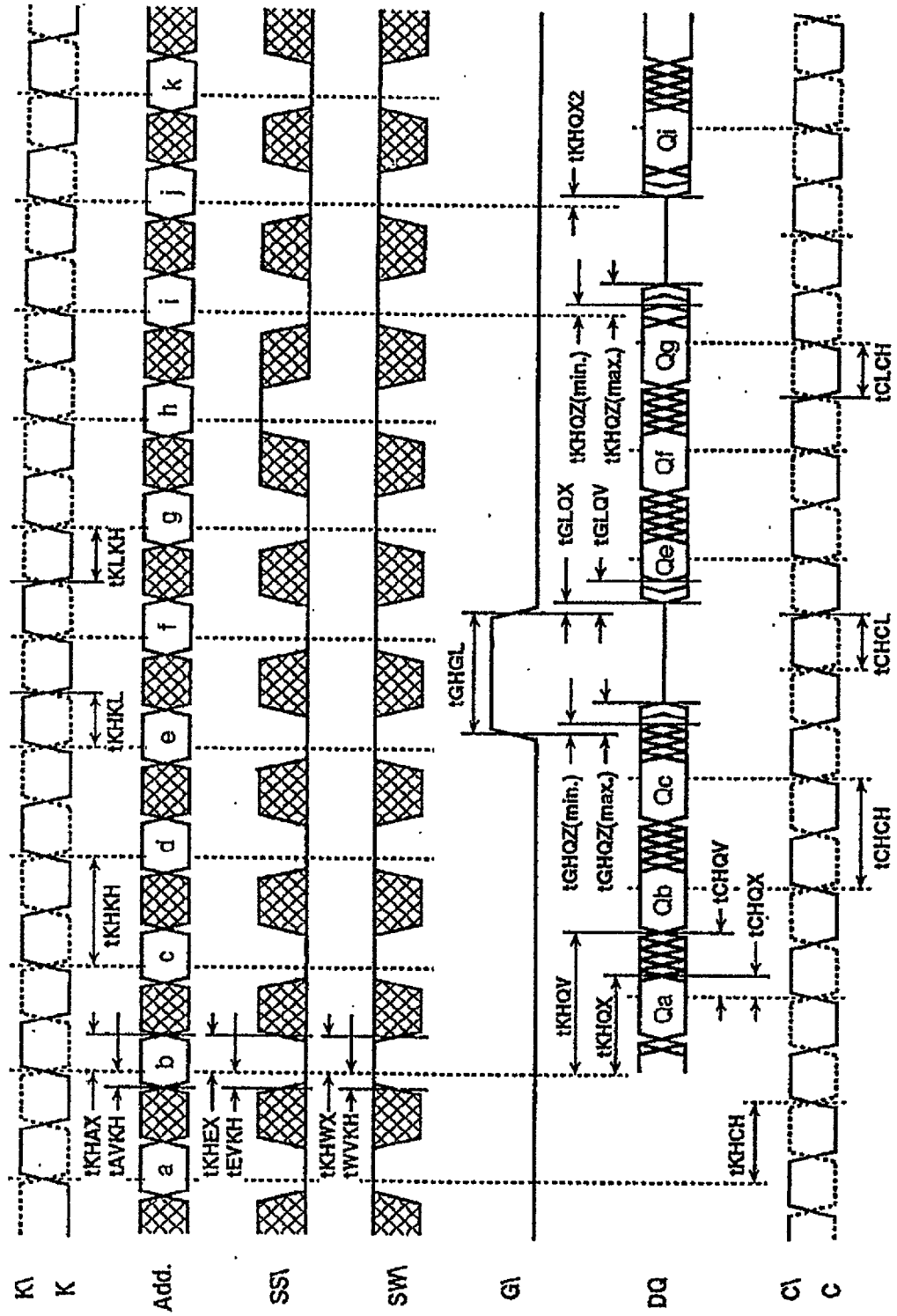
Dual Differential Clock, Registered Input / Latched Output Mode (Read Operation)



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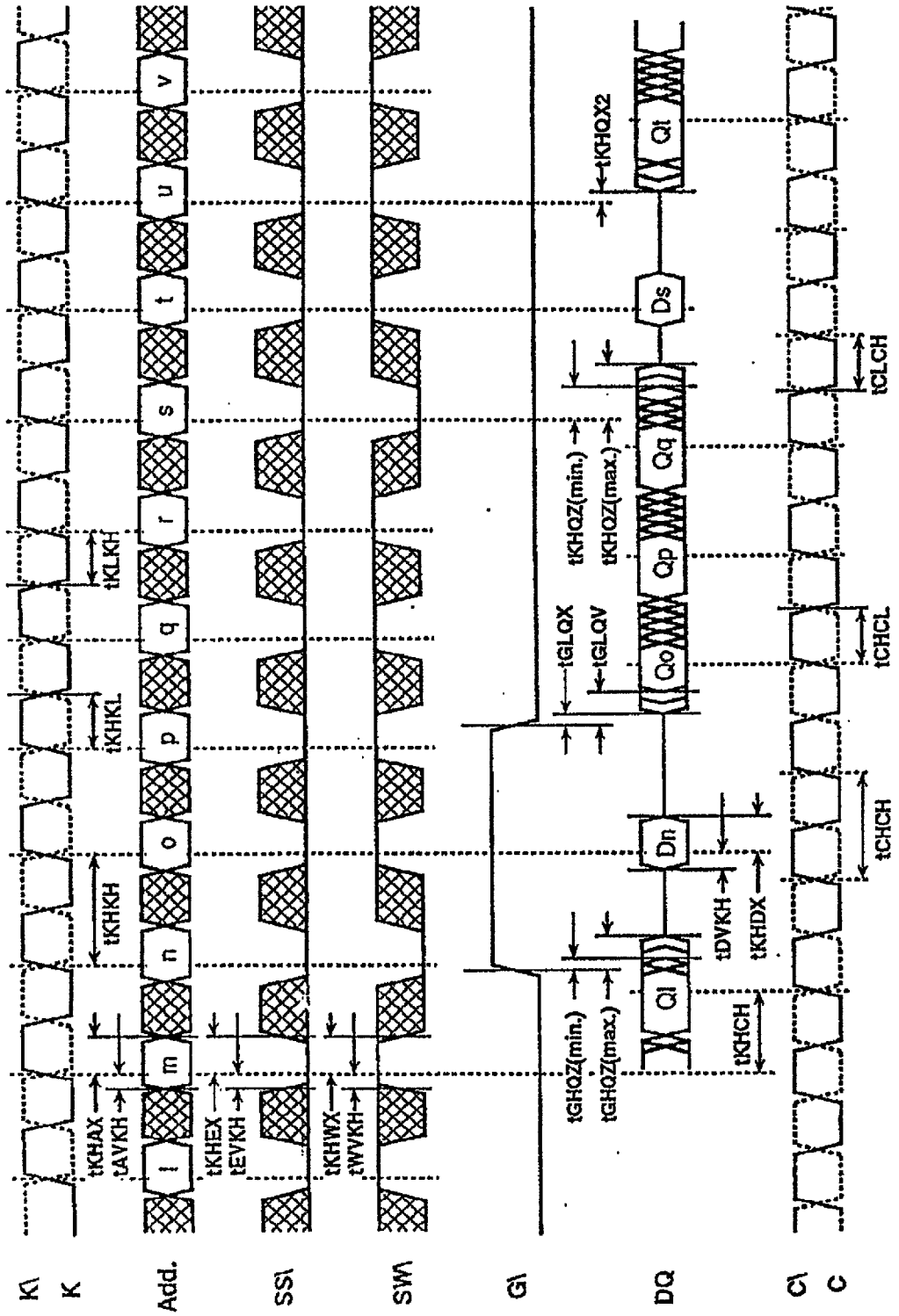
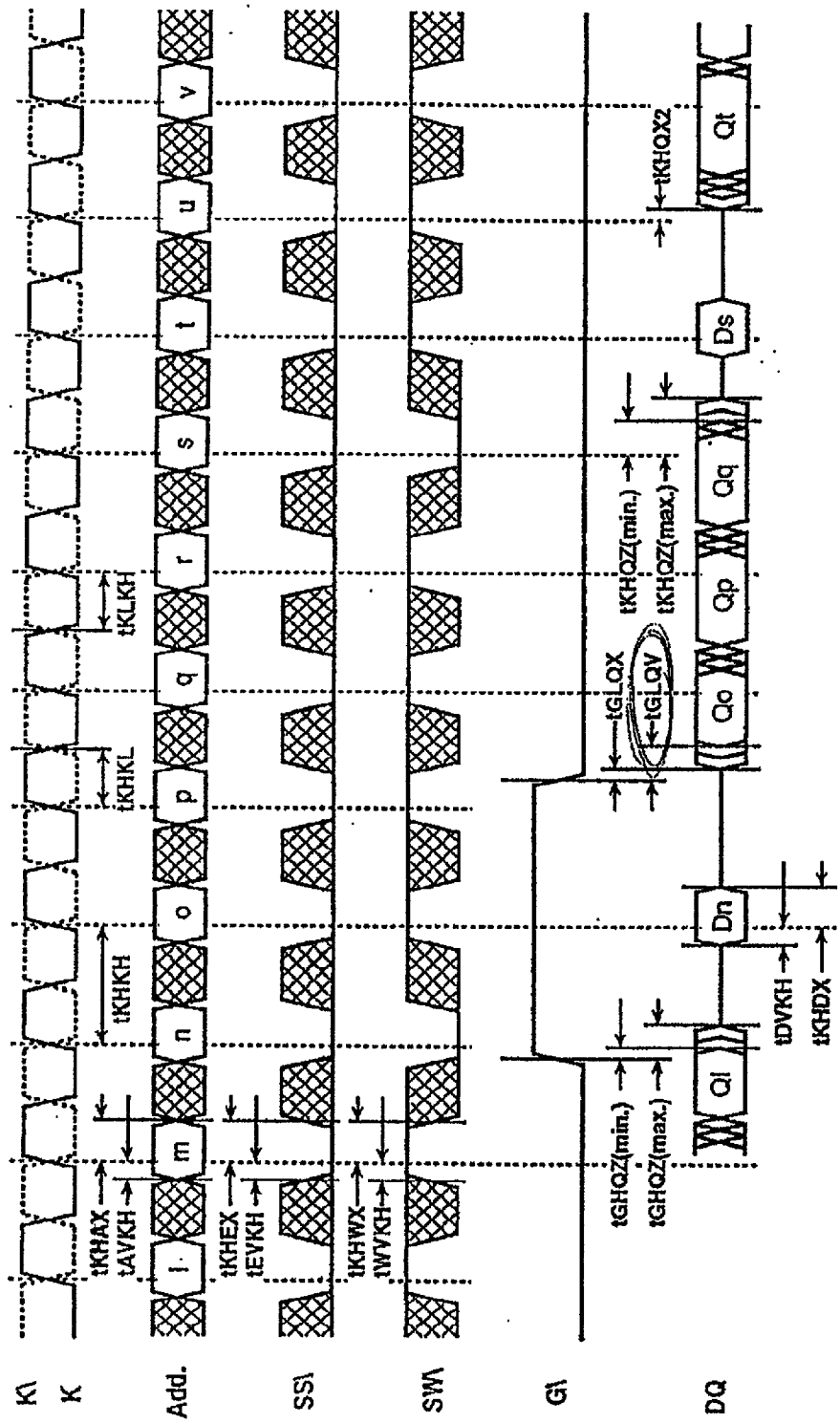
Dual Differential Clock, Registered Input / Latched Output Mode (Write Operation)



Single Differential Clock, Registered Input / Registered Output Mode (Write Operation)



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Dual Diffential Clock, Registered Input / Latched Output Mode

Parameter		Symbol	-5 (200MHz)		-55 (182MHz)		-6 (166MHz)		-7 (150MHz)		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock Cycle Time	K/K\	TKHKH	5.0	10	5.5	10	6.0	10	7	10	1,7
	C/C\	TCHCH	5.0	10	5.5	10	6.0	10	7	10	1,7
Clock Phase Time	K/K\	TKHKL / TKLKH	2.0		2.25		2.5		3		
	C/C\	TCHCL / TCLCH	2.0		2.25		2.5		3		
K to C Delay Time		TKHCH	1.5	TKHKH - 2.0	1.5	TKHKH - 2.0	1.5	TKHKH - 2.0	1.5	TKHKH - 2.0	
Setup Time	Address	TAVKH	0.5		0.5		1.0		1.0		
	Write Data	TDVKH	0.5		0.5		1.0		1.0		
	Write Enable	TWVKH	0.5		0.5		1.0		1.0		
	Chip Select	TEVKH	0.5		0.5		1.0		1.0		
Hold Time	Address	TKHAX	1.5		1.5		1.5		2.0		
	Write Data	TKHDX	1.5		1.5		1.5		2.0		
	Write Enable	TKHWX	1.5		1.5		1.5		2.0		
	Chip Select	TKHEX	1.5		1.5		1.5		2.0		
Address Access Time		TKHQV		8		8.25		8.5		9	4
K High to Q Change		TKHQX									3
C Clock Access Time		TCHQV		3		3.25		3.5		4	2
C Low to Q Change		TCHQX	0.5		0.5		0.5		0.5		5
G\ Low to Q Valid		TGLQV		3		3.25		3.5		4	4
G\ Low to Q Change		TGLQX	0.5		0.5		0.5		0.5		5
G\ High to Q Hi-z		TGHQZ	0.5	3	0.5	3.25	0.5	3.5	0.5	4	5
K High to Q Hi-z		TKHQZ	0.5	3	0.5	3.25	0.5	3.5	0.5	4	5
K High to Q Lo-z		TKHQX2	0.5		0.5		0.5		0.5		
G\ High Pulse Width		TGHGL	TKHKH		TKHKH		TKHKH		TKHKH		6

Notes

1. TKHKH=TCHCH
2. TCHQV = TKHQV - TKHCH
3. TKHQX = TKHCH + TCHQX
4. Load Model (a)
5. Load Model (b)
6. Controlled Impedance
   Push-Pull Output Buffer Mode only
7. After Power-On, 2000 cycles proper K and C clock inputs are needed before starting operation.

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Scan Exit Order

μPD461318LS1 (64Kx18)

1	M2	5R	26	NC	3B
2	SA5	6T	27	NC	2B
3	SA0	4P	28	SA9	3A
			29	SA10	3C
4	SA4	6R	30	SA13	2C
5	SA8	5T	31	SA12	2A
6	NC	7T			
			32	DQb1	1D
7	DQa1	7P	33	DQb2	2E
8	DQa2	6N			
			34	DQb3	2G
9	DQa3	6L			
			35	DQb4	1H
10	DQa4	7K	36	SBb\	3G
11	SBa\	5L	37	ZQ	4D
12	K\	4L	38	SS\	4E
13	K	4K	39	C\	4G
14	G\	4F	40	C	4H
			41	SW\	4M
15	DQa5	6H			
16	DQa6	7G	42	DQb5	2K
			43	DQb6	1L
17	DQa7	6F			
18	DQa8	7E	44	DQb7	2M
			45	DQb8	1N
19	DQa9	6D			
20	SA2	6A	46	DQb9	2P
21	SA3	6C	47	SA11	3T
22	SA7	5C	48	SA14	2R
23	SA6	5A	49	SA1	4N
24	NC	6B	50	SA15	2T
25	NC	5B	51	M1	3R

μPD461336LS1 (32Kx36)

1	M2	5R	36	NC	3B
			37	NC	2B
2	SA0	4P	38	SA9	3A
3	SA8	4T	39	SA10	3C
4	SA4	6R	40	SA13	2C
5	SA7	5T	41	SA12	2A
6	NC	7T	42	DQc9	2D
7	DQa9	6P	43	DQc8	1D
8	DQa8	7P	44	DQc7	2E
9	DQa7	6N	45	DQc6	1E
10	DQa6	7N	46	DQc5	2F
11	DQa5	6M	47	DQc4	2G
12	DQa4	6L	48	DQc3	1G
13	DQa3	7L	49	DQc2	2H
14	DQa2	6K	50	DQc1	1H
15	DQa1	7K	51	SBc\	3G
16	SBa\	5L	52	ZQ	4D
17	K\	4L	53	SS\	4E
18	K	4K	54	C\	4G
19	G\	4F	55	C	4H
20	SBb\	5G	56	SW\	4M
21	DQb1	7H	57	SBd\	3L
22	DQb2	6H	58	DQd1	1K
23	DQb3	7G	59	DQd2	2K
24	DQb4	6G	60	DQd3	1L
25	DQb5	6F	61	DQd4	2L
26	DQb6	7E	62	DQd5	2M
27	DQb7	6E	63	DQd6	1N
28	DQb8	7D	64	DQd7	2N
29	DQb9	6D	65	DQd8	1P
30	SA2	6A	66	DQd9	2P
31	SA3	6C	67	SA11	3T
32	SA6	5C	68	SA14	2R
33	SA5	5A	69	SA1	4N
34	NC	6B			
35	NC	5B	70	M1	3R