SGS-THOMSON MICROELECTRONICS

TEA2128

COLOR TV SCANNING AND POWER SUPPLY PROCESSOR

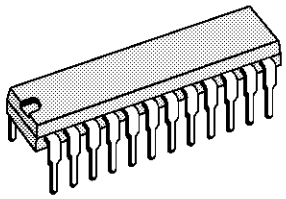
ADVANCE DATA

DEFLECTION

- AUTOMATIC VCR MODE RECOGNITION FOR TIME CONSTANT SWITCHING
- VIDEO IDENTIFICATION CIRCUIT
- DEFLECTION 500kHz RESONATOR OSCILLATOR
- NO LINE AND FRAME OSCILLATOR ADJUSTMENT
- DUAL PLL FOR LINE DEFLECTION
- SUPER SANDCASTLE OUTPUT
- INTERNAL SYNCHRO INHIBITION FOR OSD MODE
- AUTOMATIC 50Hz/60Hz STANDARD IDENTIFICATION
- EXCELLENT INTERLACING CONTROL
- FRAME SAFETY INPUT
- FRAME SAWTOOTH GENERATOR

S.M.P.S. CONTROL

- ERROR AMPLIFIER AND PHASE MODULATOR
- SYNCHRONIZATION WITH HORIZONTAL DEFLECTION
- START UP PROCESSOR
- MASTER/SLAVE CONCEPT FACILITIES



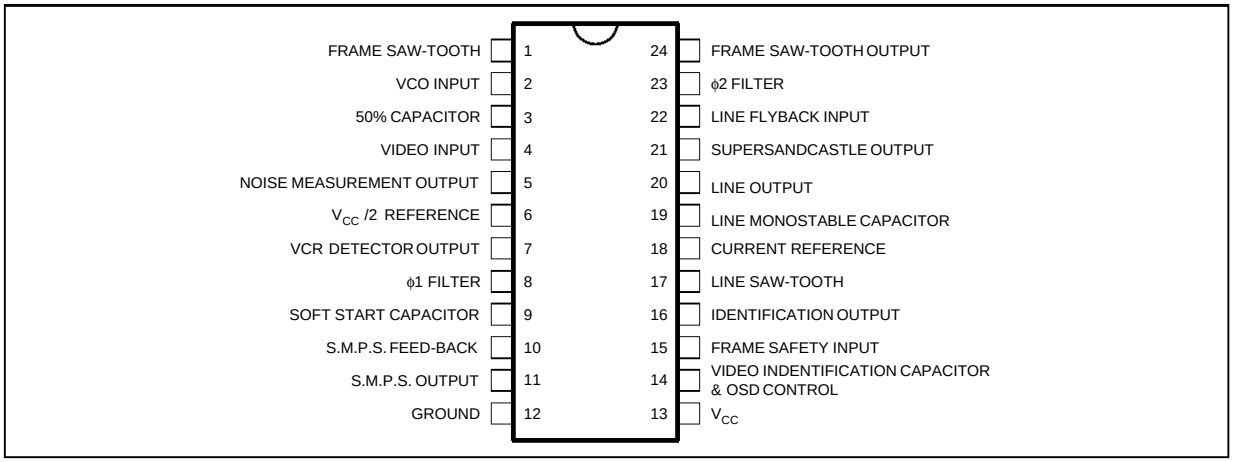
SHRINK24
(Plastic Package)

ORDER CODE : TEA2128

DESCRIPTION

The TEA2128 is a complete (horizontal and vertical) deflection processor with secondary to primary S.M.P.S. control for color TV sets.

PIN CONNECTIONS



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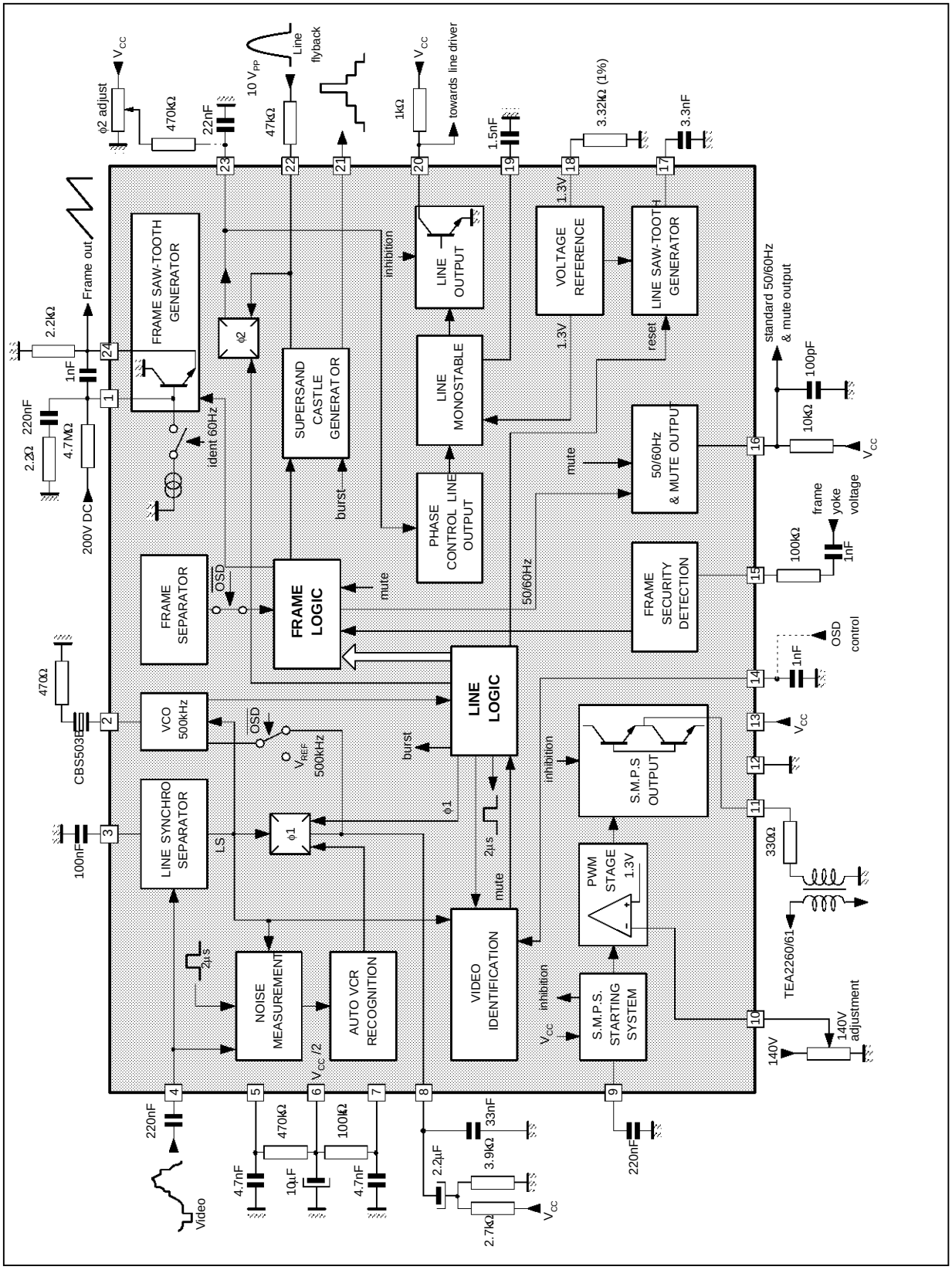
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	13.5	V
I_{11}	Output Current	80	mA
I_{20}	Input Current	40	mA
I_{22}	Input Current	± 5	mA
T_{AMB}	Operating Ambient Temperature	0 , 70	°C

2128-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction-ambient Thermal Resistance	60	°C/W

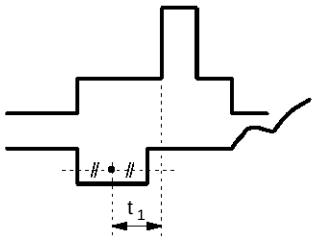
2128-02.TBL

ELECTRICAL CHARACTERISTICS (T_{AMB} = 25°C; V_{CC} = 12V; Pulse duration 50% of the amplitude)

Symbol	Parameter	Pins	Test conditions	Min.	Typ.	Max.	Unit
	Supply Voltage	13			12		V
	Supply Current	13	Without load in Pins 11, 16, 21, 24		30		mA
VIDEO INPUT							
	Video Signal Amplitude	4	Z source < 200Ω	0.2	1	3	V_{PP}
	Push out Current	4	During the synch. pulse		- 30		µA
	Pull in Current	4	During the line		5		µA
50% SYNCH. PULSE CLAMP							
	Push out Current	3	During the synch. pulse		- 350	-900	µA
	Pull in Current	3	During the line		25		µA
ϕ 1 AND ϕ 3 COMPARATOR							
	Short Time Output Current	7 - 8	Identification high		± 1.5		mA
	Long Time Output Current	7 - 8	Identification high		± 0.5		mA
VCO							
	Catching Range	2	Ceramic CSB 503B, R_{SERIAL} = 470Ω	15		16.3	kHz
	Transfer Characteristic		ΔF Pin 20/ΔV Pin 8		2		kHz/V
	Free Running Frequency		Without video signal		15.6		kHz
VIDEO IDENTIFICATION AND STANDARD OUTPUT							
	No video on Pin 4	16	I_{16} = 3mA		0	500	mV
	60Hz video	16	I_{16} = 3mA	5.7	6	6.3	V
	50Hz video	16	I_{16} = 10µA	10.5	11		V
VIDEO IDENTIFICATION AND O.S.D. CONTROL							
	Identification Time	14			2		µs
	Output Current		• 2µs pulse within the synchro pulse • 2µs pulse outside the synchro pulse	-135 65	-160 80	-185 95	µA µA
	Identification Threshold				4.6		V
	OSD Switching Threshold		lower than			1	V
REFERENCE VOLTAGE							
	Output voltage	6	I_6 = 0		$V_{CC}/2$		V
	Output impedance		ΔI_6 = ± 50µA		600		Ω
	Max output current					200	µA
AUTO VCR SWITCH							
	Switching threshold /V_6	7	• With no noise on the video ($V_5 \leq$ 6V) • With noise on video (6V < V_5 < 7.3V) St* = 0.69 V_5 - 3.85	± 0.28	± 0.3 St*	± 0.32	V V

2128-03.TBL

ELECTRICAL CHARACTERISTICS (continued)
(T_{AMB} = 25°C; V_{CC} = 12V; Pulse duration 50% of the amplitude)

Symbol	Parameter	Pins	Test conditions	Min.	Typ.	Max.	Unit
NOISE GATE							
	Measure sampling time	5	On the synch. pulse bottom		2		µs
	Max. push out current		Max. noise		350		µA
	VCR switch inhibition threshold				7.3		V
	Measure bandwidth (-3dB)			700		2000	kHz
	Short time constant manual switching threshold		Active under threshold	4.5	5	5.5	V
	Long time constant		From lower to higher voltage	6.9	7.3	7.6	V
	Manual switching threshold		From higher to lower voltage	6.8	7.2	7.5	V
ϕ 2 COMPARATOR (Pin 14)							
	Output current		During line flyback		± 600		µA
	Delay between ϕ 2 falling edge and the middle video sync. pulse	23 -4	F_{VCO} = 500 kHz		2.8		µs
LINE MONOSTABLE							
	Charge current	19	Line output high		- 67		µA
	Discharge current	19	Line output low		120		µA
	Flip-Flop threshold	19	Falling edge on the line output		1.3		V
LINE OUTPUT							
	Low level	20	I_{20}= 20 mA			1	V
	Pulse duration		R_{18} = 3.32kΩ , C_{19} = 1.5nF	27.5	29	30.5	µs
	ϕ 2 adjustment range	20	Controlled by V_{23} compared with video signal		16		µs
LINE SAW-TOOTH							
	Charge Current	17	R_{18} = 3.32 kΩ		- 180		µA
	Discharge Current	17			7		mA
	Discharge Duration		Controlled by logic VCO 500kHz		6.5		µs
LINE FLYBACK INPUT							
	Blanking Line Threshold	22		0.38	0.4	0.42	V
	ϕ 2 Loop Threshold and Line Output Inhibition	20		2.85	3	3.15	V
	Input Current		- 0.4V < V_{22} < 0.4V 0.4V < V_{22} < 3V 3V < V_{22}		-10 - 5	 - 1	µA µA µA
SUPER SANDCASTLE GENERATOR							
	Burst Level	21	R_L = 2.2 kΩ to ground	9			V
	Line Blanking	21		4	4.5	5	V
	Frame Blanking	21		2	2.5	3	V
	Delay between the midde of the video sync. pulse and the rising edge of the burst (t_1)	21	 2128-03.EPS		2.8		µs

2128-04.TBL

ELECTRICAL CHARACTERISTICS (continued)

(T_{AMB} = 25°C; V_{CC} = 12V; Pulse duration 50% of the amplitude)

Symbol	Parameter	Pins	Test conditions	Min.	Typ.	Max.	Unit
SUPER SANDCASTLE GENERATOR (continued)							
	Burst Pulse Duration	21 21	• 50Hz • 60Hz		4.4 3.9		µs µs
	Line Blanking Duration	22	Fixed by flyback Signal pin 22				
	Frame Blanking Duration	21	Fixed by the logic		21		Line
FRAME SAW-TOOTH GENERATOR							
	Low DC Voltage	24			1.3		V
	Discharge Current	1		15		60	mA
	60Hz Internal	1			8		µA
FRAME LOGIC SYNCH.							
	Free Running Period	1-24	Without video signal		315		Line
	Synchronization Windows		Identification low Identification 50Hz high Identification 60Hz high VCR mode	247 309 247 247		361 315 277 361	Line Line Line Line
FRAME SAFETY INPUT							
	Switching Threshold	15	Actived without negative pulse during frame blanking time.		1.3		V
	Output current			40	50	67	µA
S.M.P.S.							
	Input Current	10	$V_{Pin\ 10} = V_{REF}$			2	µA
	Transfer Characteristic		$\Delta t_{Pin\ 11} / \Delta V_{Pin\ 10}$		1.9		µs/µV
$t_{ON\ (max.)}$		11			28		µs
$t_{ON\ (min.)}$		11			1		µs
	High Level Voltage	11	R_{load} / GND = 500Ω	9			V
SOFT-START							
	V_{CC} Starting Voltage for Line and S.M.P.S.	13	V_{CC} rising		7	7.4	V
	Switch-off Voltage For Line and S.M.P.S. Output	13	V_{CC} decreasing		6.5		V
	Discharge Current	9	• Before soft start period, V_{CC} > 7V $V_{Pin\ 9} > V_{max.\ Pin\ 17}$ • During soft start period, V_{CC} > 7V $V_{Pin\ 9} < V_{max.\ Pin\ 17}$		60 2.3		µA µA
CURRENT REFERENCE							
	V_{18} Voltage	18	R_{18} = 3.32 kΩ (1%)	1.21	1.3	1.39	V
	Temperature Shift	18	ΔT = 80°C			± 1	%

2128-05.TBL

GENERAL DESCRIPTION

Introduction

This integrated circuit uses high density I2L bipolar technology and combines analog signal processing with digital processing.

Timing signals are obtained from a voltage-controlled oscillator (VCO) operating at 500kHz by means of a cheap ceramic resonator. This avoid the frequency adjustment normally required with line and frame oscillators.

A chain of dividers and appropriate logic circuitry produces very accurate defined sampling pulses and the necessary timing signals.

Internal Functions

- Horizontal scanning processor
- Frame scanning processor
- B class frame output stage using an external power amplifier with flyback generator
- Line and frame synchronization separation
- Dual phase-locked loop horizontal scanning

- High performance frame and line synchronization with interlacing control.
- Supersandcastle generator
- Automatic 50Hz / 60Hz standard identification
- Frame saw-tooth generator
- Video identification circuit
- Very steady free running mode of the line and frame oscillator in OSD mode. This allows on screen display without phase Jitter in research mode of the tuner
- Automatic VCR mode recognition for time constant switching
- Switching mode regulated supply comprising error amplifier and phase modulator. This allowed a secondary switch mode power regulation with a master slave concept and provides **active standby** facilities
- Line and S.M.P.S. start-up processor
- Frame safety input

WORKING DESCRIPTION

Synchronization Separator

Line synchronization separator is clamped to black level of input video signal with synchronization pulse bottom level measurement.

The synchronization pulses are divided centrally between the black level and the synchronization pulse bottom level, to improve performance on video signal in noise conditions.

Frame Synchronization

Frame synchronization is fully integrated (no external capacitor required).

The frame timing identification logic permits automatic adaptation to 50-60Hz standards or non-interlaced video.

An automatic synchronization window width system provides:
- Fast frame capture (7.3ms wide window)
- Good noise immunity (0.4ms narrow window)

The internal generator starts the discharge of the sawtooth generator capacitor, so that it is not disturbed by line flyback effects.

Thanks to the logic control, the beginning of the charge phase does not depend on any disturbing effect of the line flyback. A 32µs timing is automatically applied on standardized transmissions for perfect interlacing.

In VCR mode, the discharge time is controlled by an internal monostable independent of the line frequency and gives a direct frame synchronization.

Horizontal Scanning

The horizontal scanning frequency is obtained from the 500kHz VCO.

The circuit uses two PLL:
- The first one controls the frequency
- The second one controls the relative phase of the synchronization and the line flyback signals.

The output pulse has a constant duration of 29µs, independent of V_{CC} and of any delay in switching-off the scanning transistor.

Supersandcastle Generator

This output delivers a 3 level synchronization signal:
- Burst level
- Line blanking level
- Frame blanking level

In the event of vertical scanning failure, the frame blanking level goes high to protect the tube.

Frame Scanning

The current to charge the frame sawtooth generator is automatically switched to 60Hz operation to maintain constant amplitude.

Automatic VCR Mode Recognition for Time Constant Switching

- A third phase comparator is used to detect VCR signals and to switch the $\phi 1$ short time constant.
- A noise level measurement is realized on the video synchronization pulse to inhibit the short time constant if the noise level is superior to an adjustable threshold.
- VCR signals are detected if peak to peak signal on Pin 7 is superior to an internal threshold.

This threshold is depending on the noise level. So with a no noisy video signal, the auto VCR switch sensitivity is maximum, and it decreases when the noise increases.
- The sensitivity of the noise gate and the auto VCR switch is adjustable by external resistance.
- Long and short time constants can be selected manually by Pin 5.

Video Identification

The horizontal synchronization signal is sampled by a 2µs pulse within the synchronization pulse. The signal is integrated by an external capacitor.

Identification Output

The identification function provides three different levels :
- 0V : No video identification
- 6V : 60Hz video identification
- 12V : 50Hz video identification

This information may be used for timing research in the case of frequency or voltage synthetizer type receivers and for audio muting.

O.S.D. Mode

The O.S.D. (On Screen Display) function is available when Pin 14 is switch to ground. This function fixes line and frame frequencies to standard deflection frequencies (f_H = 15.6kHz, f_V = 50Hz) and inhibits Φ1 PLL. This allows to have a stable text display when no signal is coming from antenna.

Switch Mode Power Supply Secondary to Primary Regulation

This power supply uses a differential error amplifier with an internal reference voltage of 1.3V and a phase modulator operating at the line frequency. The power transistor is turned-off during the line retrace by the falling edge of the horizontal sawtooth.

The maximum conduction angle may be monitored by forcing a voltage at Pin 9. This pin can also be used for current limitation.

The output pulse is sent to the primary IC (TEA2260/61 via a low cost synchro transformer).

S.M.P.S. Start-up Processor

The "soft-start" device imposes a very small conduction angle on starting-up. This angle progressively increases to its nominal regulation value.

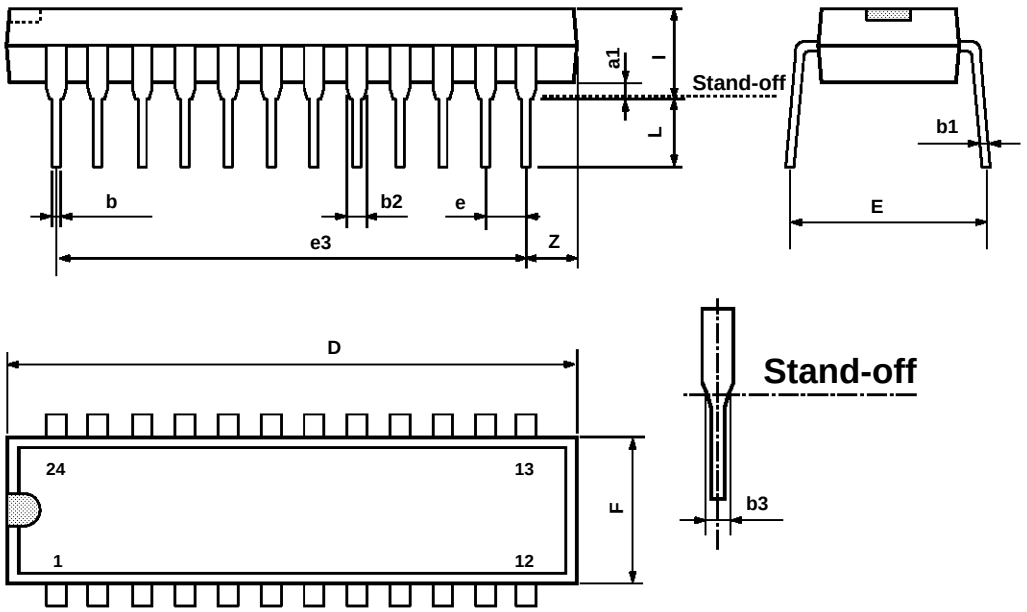
On starting-up the horizontal scanning function comes into operation at V_{CC} = 7V. The power supply then comes into operation progressively.

Frame Blanking Safety Input (Pin 15)

The frame blanking safety checks the normal frame scanning. In the event of vertical scanning failure, the frame blanking level goes high to protect the CRT.

PACKAGE MECHANICAL DATA

24 PINS - PLASTIC SHRINK DIP



PMSDIP24.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.3			0.130	
a1	0.51			0.020		
b	0.35		0.59	0.014		0.023
b1	0.2		0.36	0.008		0.014
b2	0.75		1.42	0.030		0.056
b3	0.75			0.030		
D			23.11			0.910
E	7.95		9.73	0.313		0.383
e		1.778			0.070	
e3		19.558			0.770	
e4		7.62			0.300	
F			6.86			0270
i			5.08			0.200
L	2.54			0.100		

SDIP24.TBL