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JUPITER

CDMA and FM (AMPS) I/Q Filter

Preliminary Information

DS4724 - 3.1 May 1998

The JUPITER circuit is designed for use in dual band and dual mode mobile phones (CDMA/AMPS) and meets the requirements for IS-95 when used with other chips from Mitel that form the Planet chipset. JUPITER is an active filter incorporating circuits for receiving both CDMA and FM (AMPS).

FEATURES

- Low Power and Low Voltage Operation with a Sleep Mode
- Integrated CDMA and FM Filter with Wide Dynamic Range
- Low Inband Gain Ripple Performance and Good I/Q Matching for the Filter

ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{CC\ MAX}$	−0·7V to +5·3V
Operating temperature, T_{OP} (at pins)	−30°C to+70°C
Storage temperature, T_{STG} (ambient)	−40°C to +150°C
Junction temperature	−30°C to +125°C
CMOS input logic high, V_{IH}	V_{CC}+0·6V (Max.)
CMOS input logic low, V_{IL}	−0·6V (Min.)
Maximum input voltage at all pins	−0·6V to $V_{CC\ MAX}$+0·6V

ORDERING INFORMATION

JUPITER-1/KG/NP1S

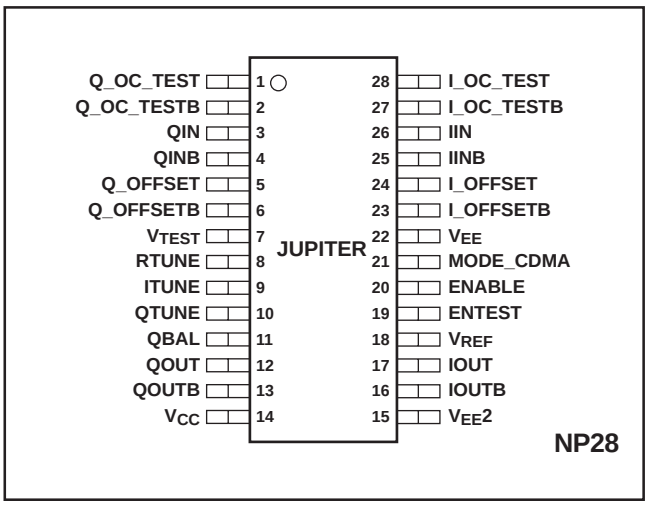


Fig. 1 Pin connections - top view

ESD PROTECTION

All pins are protected against electrostatic discharge to both supplies. At least 2kV protection is provided to MIL-STD-883D Method 3015.7 (human body model).

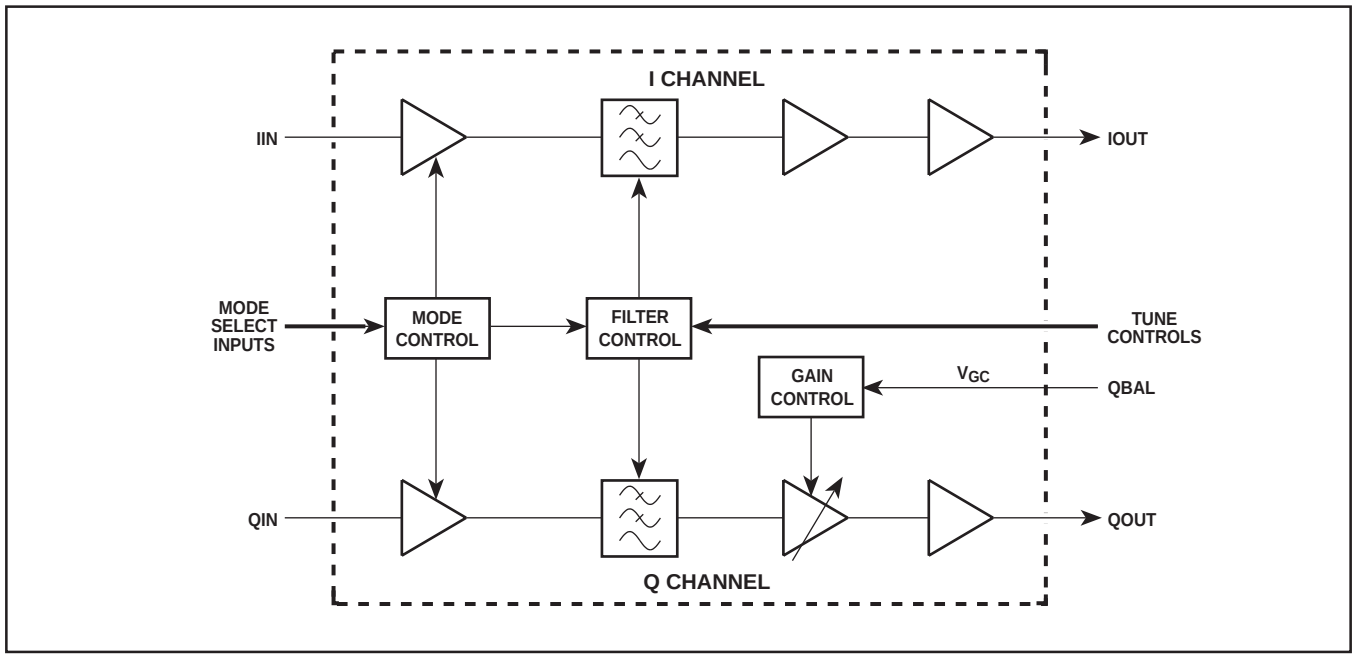


Fig. 2 Simplified block diagram

CIRCUIT DESCRIPTION

The block diagram of the JUPITER filter is shown in Fig. 3. Two tunable active low-pass gyrator filters are designed with balanced I/Q inputs and outputs.

CDMA MODE

In CDMA mode the filter (F1 on Fig. 3) is a 7th order 0.1dB ripple continuously tunable elliptic type with the corner frequency tuned to 690kHz for best stop band attenuation and minimal phase error (in the overall system). Variable gain stages after the filter provide the gain control capability. Overall, each of the CDMA I/Q channels has 45dB nominal voltage gain with the Q channel having ±2dB gain adjustment range. Separate I/Q frequency tuning functions are built into the device.

FM MODE

In FM mode the same filter is used; however, the biasing is designed such that the current density in the transconductor cells is reduced by a factor of 46, changing the filter's cutoff frequency to 15kHz. The filter characteristic of the main channel filter (gyrator filter) remains the same, i.e. a 0.1dB 7th order elliptic. In FM mode additional 2nd order Sallen and Key 0.1dB ripple Chebeyshev filters (F2) are included in the signal path prior to the gyrators. These improve the out-of-band blocking of the overall filter. Different amplifiers are used in FM mode to those used in CDMA mode to enable optimization of the gain distribution in FM mode for current consumption and dynamic range.

OPERATION

Signal inputs are DC coupled in both CDMA and FM modes. The device modes are selected by CMOS compatible logic signals as shown in Table 2. An external resistor should be connected between RTUNE and ground to set internal currents; a resistor with a tolerance of ±5% and a temperature coefficient of less than 100ppm is recommended. V_{REF} (pin 18) should be decoupled to V_{CC} to give optimum supply rejection.

A test mode is provided for filter calibration. In this mode, a test signal is applied to the V_{TEST} input (pin 7) with ENTEST held high. The test mode is designed to interface with the PLUTO baseband processor, which can provide the test signal and I/QTUNE voltages and calibrates the filters using an internal auto calibration algorithm. The algorithm generates two test frequencies and calibrates the filters to give the correct attenuation at the upper frequency. The calibration is normally carried out in CDMA mode: the FM filter performance is scaled accordingly.

Pins are provided for DC offset control for I and Q channels (I_OFFSET, I_OFFSETB, Q_OFFSET and Q_OFFSETB). In typical operation, the I_OFFSET/Q_OFFSET pins would be controlled by a voltage derived from the baseband processor. However, it is also possible to minimise the DC offset using external components; this is primarily intended for test purposes. These feedback components between IOUT/QOUT and I_OFFSET/Q_OFFSET are shown in Fig. 4 but would not be used in the normal application

In test mode, these offset controls are disabled and the offsets are controlled using on-chip feedback. The loop filter for this feedback uses external 10nF capacitors on pins I_OC_TEST/B and Q_OC_TEST/B as shown in Fig. 4.

Pin	Name	I/O	Description
1	Q_OC_TEST	I	Q channel offset control in test mode
2	Q_OC_TESTB	I	Q channel offset control in test mode (balanced)
3	QIN	I	Q channel CDMA/FM input.
4	QINB	I	Q channel CDMA/FM input (balanced)
5	Q_OFFSET	I	Q channel offset control
6	Q_OFFSETB	I	Q channel offset control (high gain mode)
7	V_{TEST}	I	Test mode signal input for tuning operation
8	RTUNE		Precision resistor for current definition (18k)
9	ITUNE	I	I filter tuning control
10	QTUNE	I	Q filter tuning control
11	QBAL	I	Q channel gain adjust voltage, VGC
12	QOUT	O	Q channel CDMA/FM output
13	QOUTB	O	Q channel CDMA/FM output (balanced)
14	V_{CC}	P	Supply
15	$V_{EE}2$	P	Ground
16	IOUTB	O	I channel CDMA (balanced)
17	IOUT	O	I channel CDMA
18	V_{REF}		Reference voltage decouple
19	ENTEST	I	Mode control (see Table 2)
20	ENABLE	I	Mode control (see Table 2)
21	MODE_CDMA	I	Mode control (see Table 2)
22	V_{EE}	P	Ground (substrate)
23	I_OFFSETB	I	I channel offset control (high gain mode)
24	I_OFFSET	I	I channel offset control
25	IINB	I	I channel CDMA (balanced)
26	IIN	I	I channel CDMA
27	I_OC_TESTB	I	I channel offset control in test mode (balanced)
28	I_OC_TEST	I	I channel offset control in test mode

Table 1 Pin descriptions

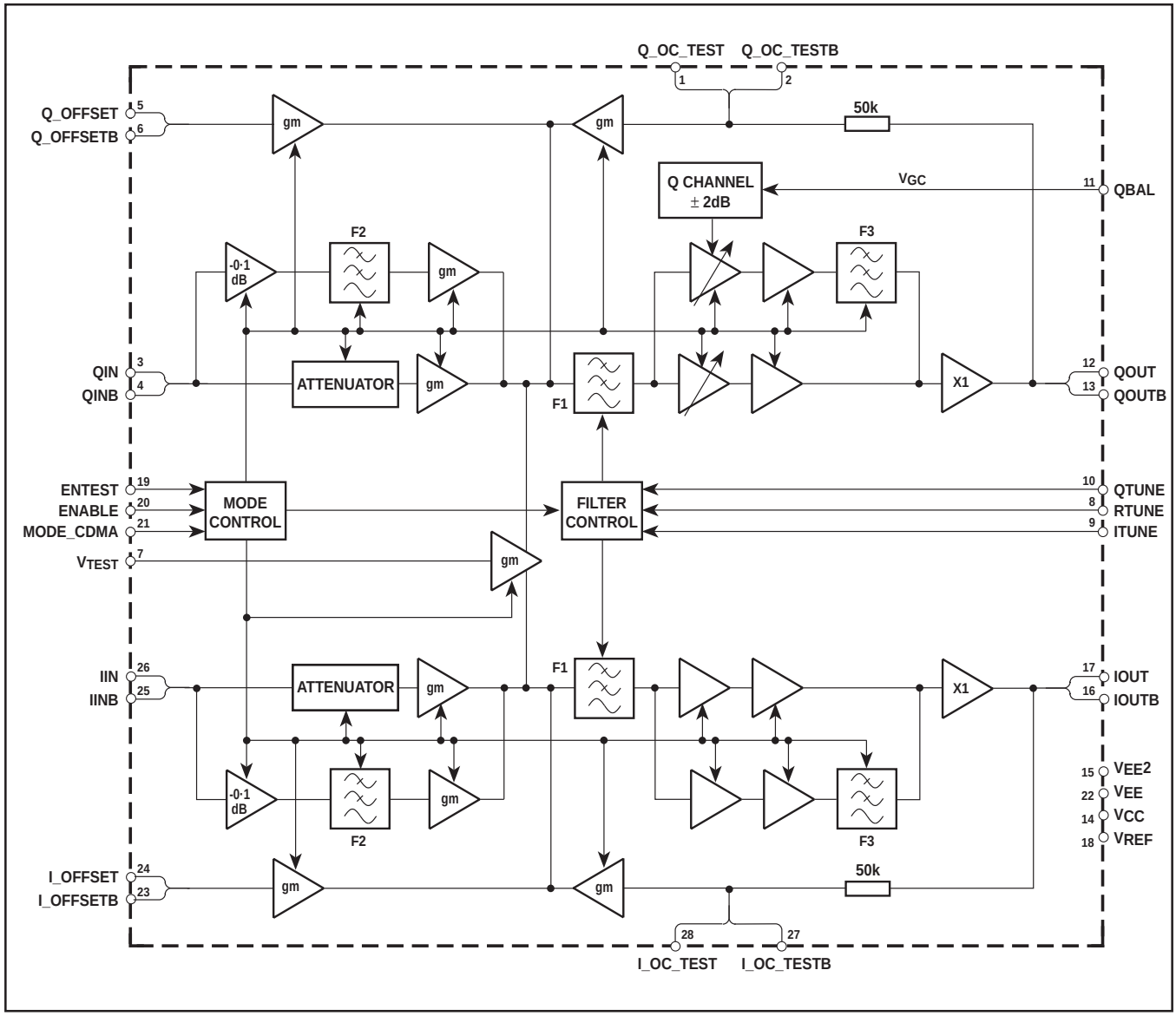


Fig. 3 Block diagram

Description	ENABLE	MODE_ CDMA	ENTEST	Comments
Sleep mode	0	X	1	All circuits powered down
CDMA mode	1	1	0	Biasing and CDMA signal path on
FM mode	1	0	0	Biasing and FM signal path on
CDMA filter testmode	1	1	1	Biasing, CDMA test and CDMA signal path on, excluding input amplifier
FM filter test mode	1	0	1	Biasing, FM test and FM signal path on, excluding input amplifier.
Disallowed mode	0	X	0	This is functionally the same as sleep mode but has higher I_{CC}. In sleep mode PLUTO applies a logic high to ENTEST

Table 2 Truth table for mode control lines

ELECTRICAL CHARACTERISTICS

The Electrical Characteristics are guaranteed over the following range of operating conditions unless otherwise stated (see Fig. 4 for test circuit):

T_{AMB} = − 30°C to +70°C, V_{CC} = 3V +0·6V/−0·3V

DC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
General					
Supply voltage, V_{CC}	2·7	3·0	3·6	V	
Operating temperature, T_{AMB}	−30		+70	°C	
Supply Current, I_{CC}					
Sleep mode			0·15	mA	QBAL = ITUNE = QTUNE <0·5V
FM mode		3·4	5·2	mA	QBAL = ITUNE = QTUNE = 1·2V
CDMA mode		7·3	11·0	mA	QBAL = ITUNE = QTUNE = 1·2V
Turn off time, CDMA/FM mode to Sleep mode		100		µs	I_{CC} reduced to 10% of active value
Mode Control Lines (CMOS)					
Input logic high, V_{IH}	2·0		V_{CC}+0·1	V	All logic inputs
Input logic low, V_{IL}	−0·1		0·5	V	
Input high current I_{IH}	−20		20	µA	
Input low current, I_{IL}	−20		20	µA	
Tune/Gain Control Lines					
DC level	0·5		2·0	V	
Input impedances:					
QBAL, ITUNE and QTUNE		200		kΩ	Referenced to on-chip ref. voltage (1·2V)
I_OFFSET/B and Q_OFFSET/B		500		kΩ	
I/O DC Voltages					
Inputs IIN/B and QIN/B	V_{CC}−0·6	V_{CC}−0·4	V_{CC}−0·2	V	
Outputs IOUT/B and QOUT/B	V_{CC}−1·6	V_{CC}−1·4	V_{CC}−1·2	V	

ELECTRICAL CHARACTERISTICS

FM Mode AC Characteristics

All parameters are defined as differential unless otherwise stated

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Maximum input frequency			10	MHz	
Gain Characteristics					
I voltage gain (A_V) IIN/B to IOUT/B	39	41	43		External load = 50kΩ//5pF
Q voltage gain QIN/B to QOUT/B	$A_V-1{\cdot}5$		$A_V+1{\cdot}5$	dB	QBAL = 1·2V
Q channel gain adjust	±2			dB	QBAL = 0·5 to 2V
Q channel gain control		4·0	8·0	dB/V	
Gain variation over temperature and supply voltage	−0·75		+0·75	dB	V_{CC} = ±150mV
Differential output amplitude balance, QOUT/QOUTB, IOUT/IOUTB			±0·25	dB	
Power Supply Rejection					
In-band		10		dB	Measured at I/Q output frequency = 10kHz
Out of band		0		dB	Measured at I/Q output frequency = 630kHz
Noise					
Input referred		30	45	µVrms	Bandwidth = 10Hz to 5MHz. I and Q channels
1dB Compression					
Output 1dB compression	1·5	1·9		Vp-p	Frequency = 2kHz
Out of band blocking signal causing 1dB compression of in-band signal					
Blocking signal at 60kHz	266			mVrms	In-band frequency = 2kHz. All conditions
		380		mVrms	27°C only
Blocking signal at 120kHz	266			mVrms	In-band frequency = 2kHz. All conditions
		380		mVrms	27°C only
Intermodulation					
Input referred intermodulation product		−101		dBV	Unmodulated interferers
		8·8		µVrms	60kHz 75mVrms, 120kHz 7·5mVrms
Filter Characteristic (Note 1)					
3dB pass band	14·5	16·5	19·5	kHz	
Stop band attenuation 45kHz	48	63		dB	
Stop band attenuation 60kHz to 10MHz	60	70		dB	
I and Q bandwidth matching			5	%	ITUNE = QTUNE = 1·2V
In-band gain ripple			1·0	dBp-p	} Frequency = 100Hz to 12·2kHz
Group delay variation		30		µs	
Average phase balance, I and Q channels			10	deg	
Offset Loop Correction					
Filter offset adjustment gain:					
I_OFFSET/Q_OFFSET	0·6	1·0	1·4	V/V	
I_OFFSET B/Q_OFFSETB		10		V/V	
Amplifier offset settling time:					
After power on		4·0		ms	Settling to within 5mV
After CDMA to FM cycling			4·0	ms	Settling to within 5mV
Input Impedances					
QIN/QINB and IN/INB	8·0	10	12	kΩ	Frequency = 2kHz
Output Impedances					
QOUT/QOUTB and IOUT/IOUTB		1·0		kΩ	Frequency = 2kHz

NOTE 1. Filter tuned in CDMA mode to −8dB at 720kHz

ELECTRICAL CHARACTERISTICS

CDMA Mode AC Characteristics

All parameters are defined as differential unless otherwise stated

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Maximum input frequency			10	MHz	
Gain Characteristics					
I voltage gain (A_V) IIN/B to IOUT/B	43	45	47		External load = 50kΩ//5pF
Q voltage gain QIN/B to QOUT/B	$A_V-1{\cdot}5$		$A_V+1{\cdot}5$	dB	QBAL = 1·2V
Q channel gain adjust	±2			dB	QBAL = 0·5 to 2V
Q channel gain control		4·0	8·0	dB/V	
Gain variation over temperature and supply voltage	−0·75		+0·75	dB	V_{CC} = ±150mV
Differential output amplitude balance, QOUT/QOUTB, IOUT/IOUTB			±0·25	dB	
Power Supply Rejection					
In-band		20		dB	Measured at I/Q output frequency = 690kHz
Noise					
Input referred		110		µVrms	Bandwidth = 10Hz to 5MHz. I and Q channels
1dB Compression					
Output 1dB compression	1·5	1·9		Vp-p	Frequency = 2kHz
Out of band blocking signal causing 1dB compression of in-band signal					
Blocking signal at 60kHz	110			mVrms	In-band frequency = 100kHz. All conditions
		150		mVrms	27°C only
Blocking signal at 120kHz	110			mVrms	In-band frequency = 100kHz. All conditions
		150		mVrms	27°C only
Intermodulation					
Input referred intermodulation product			−84·8	dBV	Unmodulated interferers
			57	µVrms	900kHz 24mVrms, 1700kHz 15mVrms
		−101		dBV	27°C only
		8·8		µVrms	
Input referred intermodulation product			−84·8	dBV	Unmodulated interferers
			57	µVrms	1·25MHz 24mVrms, 2·25MHz 15mVrms
		−101		dBV	27°C only
		8·8		µVrms	
Filter Characteristic (Note 1)					
ITUNE/QTUNE voltage	0·5	1·2	2·0	V	Tuning voltage to set filter to −8dB at 720kHz relative to 350kHz
Pass band variation over supply and temperature variation	−3	0	+3	%	V_{CC} = ±150mV
I/Q tuning gain		240		kHz/V	
Stop band attenuation 900kHz to 10MHz	50	55		dB	
I and Q bandwidth matching			4	%	ITUNE = QTUNE = 1·2V
In-band gain ripple			1·0	dBp-p	Frequency = 1kHz to 630kHz
Average phase balance, I and Q channels			3	deg	Frequency = 1kHz to 630kHz

NOTE 1. Filter tuned to −8dB at 720kHz relative to 350kHz

Cont…

ELECTRICAL CHARACTERISTICS

CDMA Mode AC Characteristics (continued)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Offset Loop Correction					
Filter offset adjustment gain:					
I_OFFSET/Q_OFFSET	1·2	2·0	2·8	V/V	
I_OFFSET B/Q_OFFSETB		2·0		V/V	
Amplifier offset settling time:					
After power on			10	ms	Settling to within 6mV
After FM to CDMA cycling			4·0	ms	Settling to within 6mV
Input Impedances					
QIN/QINB and IN/INB	8·0	10	12	kΩ	Frequency = 2kHz
Output Impedances					
QOUT/QOUTB and IOUT/IOUTB		1·0		kΩ	Frequency = 2kHz

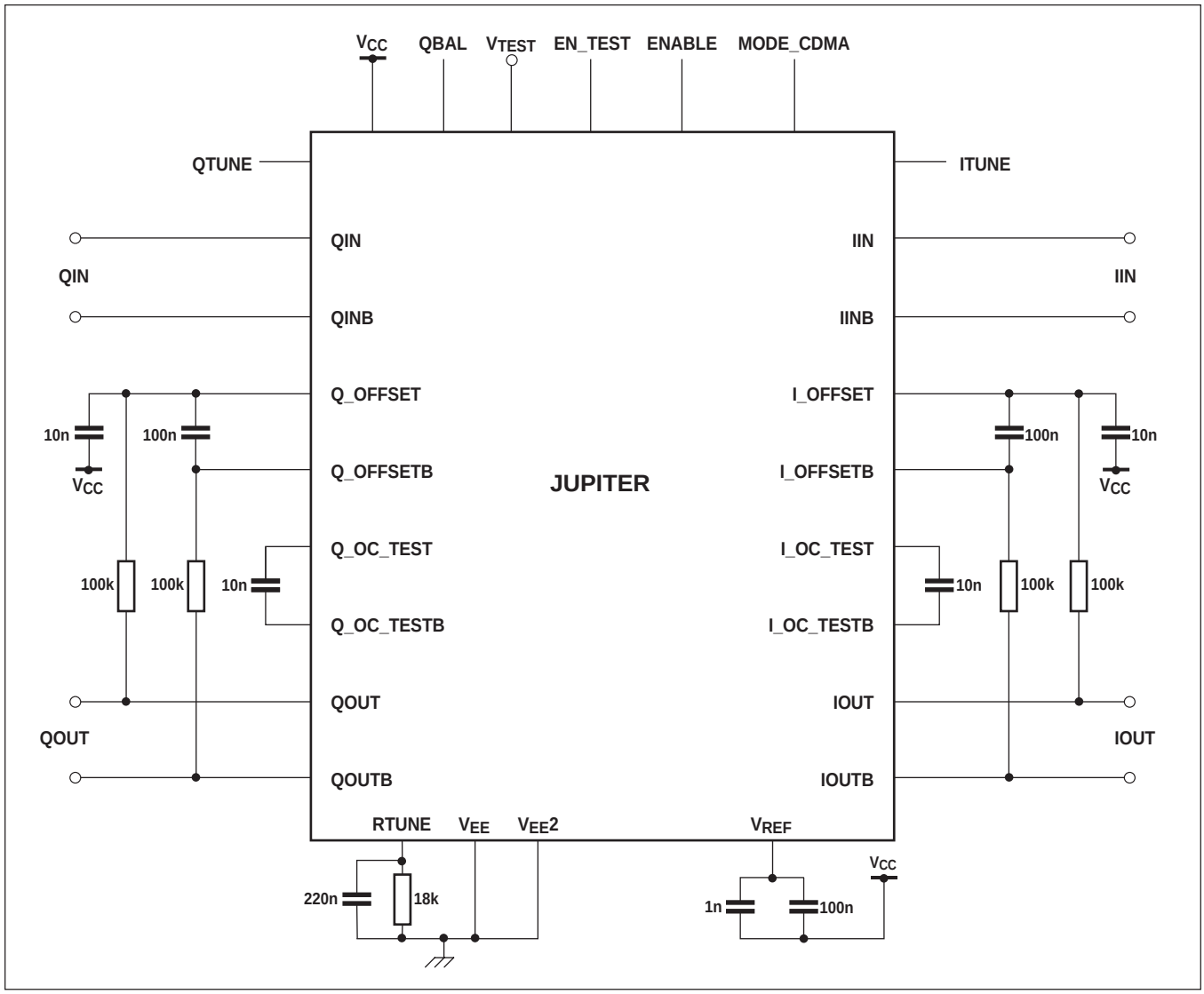
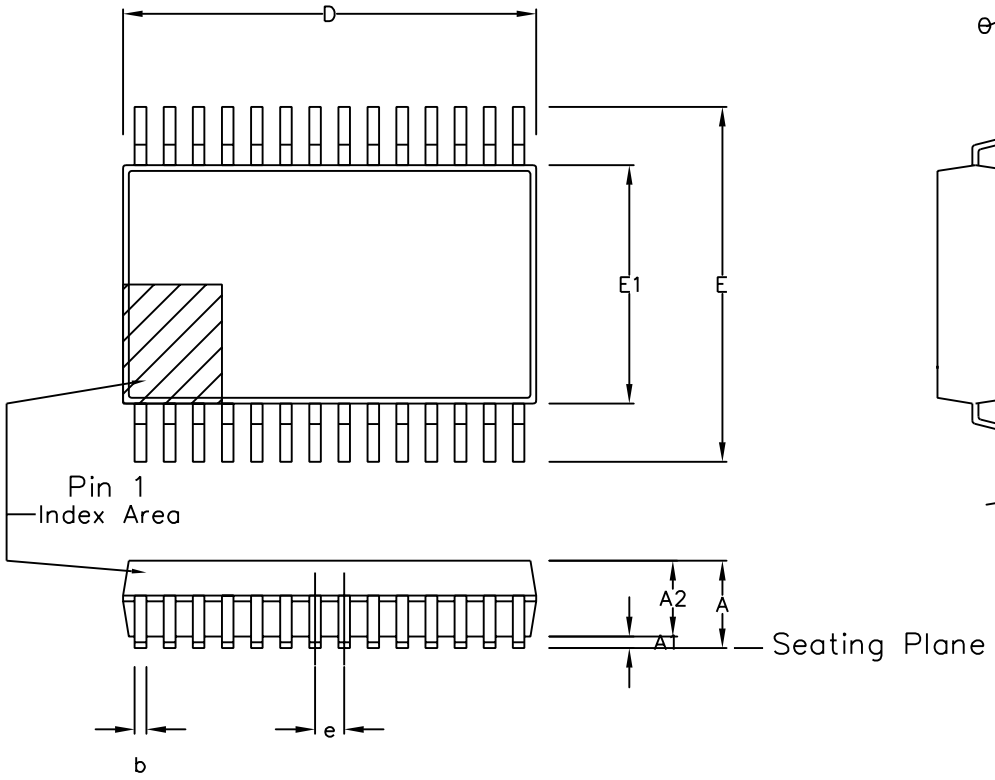


Fig. 4 Test circuit



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	1.70		2.00		0.067		0.079
A1	0.05		0.20		0.002		0.008
A2	1.65		1.85		0.065		0.073
D	9.90		10.50		0.390		0.413
E	7.40		8.20		0.291		0.323
E1	5.00		5.60		0.197		0.220
L	0.55		0.95		0.022		0.037
e	0.65 BSC.				0.026 BSC.		
b	0.22		0.38		0.009		0.015
c	0.09		0.25		0.004		0.010
θ	0°		8°		0°		8°
	Pin features						
N	28						
Conforms to JEDEC MO-150 AH Iss. B							

This drawing supersedes:-
418/ED/51481/004 (Swindon/Plymouth)

Notes:
1. A visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimensions D and E1 do not include mould flash or protusion. Mould flash or protusion shall not exceed 0.20 mm per side. D and E1 are maximum plastic body size dimensions including mould mismatch.
4. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.13 mm total in excess of b dimension. Dambar intrusion shall not reduce dimension b by more than 0.07 mm.

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APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes
NP / N

Package Code DD

Package Outline for 28 lead SSOP (5.3mm Body Width)

GPD00296

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