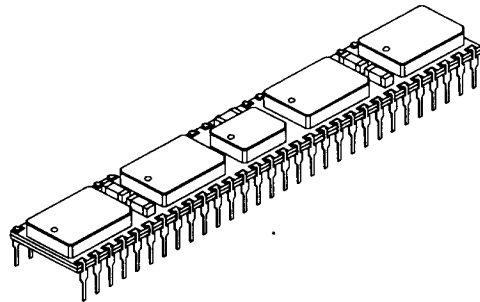


DESCRIPTION:

The DPS6433 is a fully asynchronous Static Random Access Memory (SRAM) and may be organized as 64K X 32, 128 X 16 or 256K X 8.

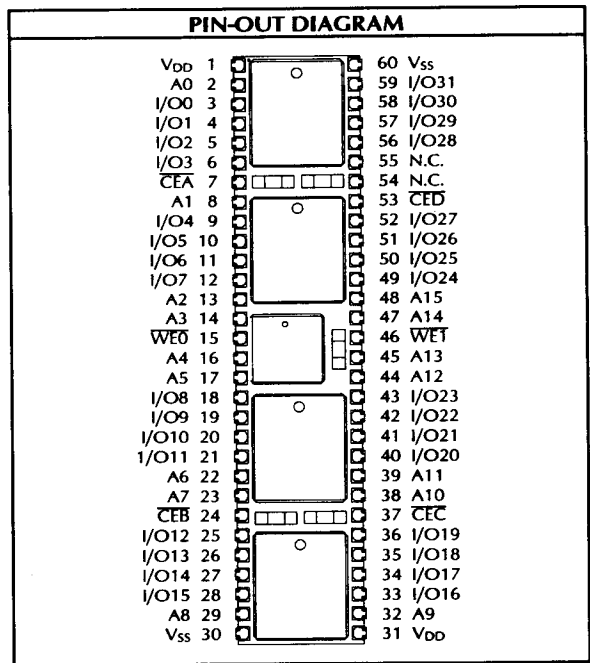
The module is built with eight low-power CMOS 32K X 8 SRAM's and two high speed 139 decoders. The DPS6433 is ideally suited for those computer systems having a 32-bit architecture.



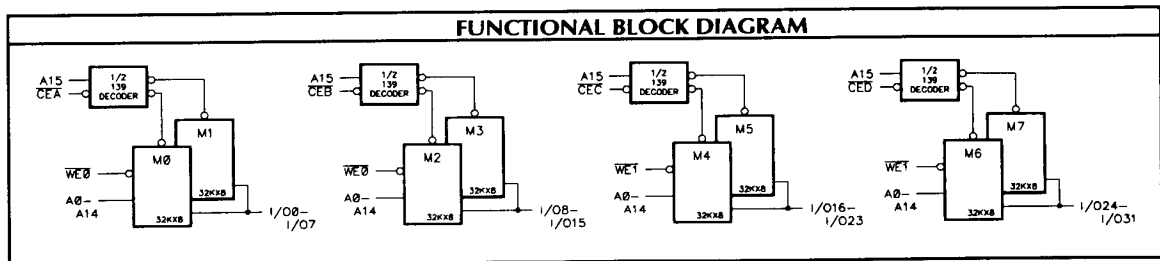
4

FEATURES:

- Organization Available:
64K X 32, 128 X 16 or 256K X 8
- Access Times: 35, 45, 55, 70, 85
100, 120, 150ns (max.)
- Byte, Word, and Double Word Selectable
- Low-Power CMOS Design
- Single +5V Operation ($\pm 10\%$ Tolerance)
- TTL-compatible Inputs and Outputs
- 60-Pin, 600 Mil Wide Ceramic DIP Package



PIN NAMES	
A0 - A15	Address Inputs
I/O0 - I/O31	Data Input/Output
CEA	Chip Enable for I/O0 - I/O7
CEB	Chip Enable for I/O8 - I/O15
CEC	Chip Enable for I/O16 - I/O23
CED	Chip Enable for I/O24 - I/O31
WE0	Write Enable for I/O0 - I/O15
WET	Write Enable for I/O16 - I/O31
V _{DD}	Power (+5V)
V _{SS}	Ground
N.C.	No Connect



DPS6433-35, -45, -55, -70, -85, -100 DC OPERATING CHARACTERISTICS: Over operating ranges									
Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I _{IN}	Input Leakage Current	V _{IN} = 0V to V _{DD}	-20	+20	-20	+20	-20	+20	μA
I _{OUT}	Output Leakage Current	V _{I/O} = 0V to V _{DD} , CE = V _{IH} or WE = V _{IL}	-20	+20	-20	+20	-20	+20	μA
I _{CC1}	Active Supply Current	CE = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	X32	530		610		630	mA
			X16	390		450		560	
			X8	320		370		375	
I _{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I _{OUT} = 0mA	X32	690		790		790	mA
			X16	470		540		540	
			X8	360		415		415	
I _{SB1}	Full Standby Supply Current (CMOS)	V _{IN} ≥ V _{DD} - 0.2V or V _{IN} ≤ V _{SS} + 0.2V, CE ≥ V _{DD} - 0.2V		16		16		16	mA
I _{SB2}	Standby Current (TTL)	CE = V _{IH}		280		280		280	mA
V _{OL}	Output Low Voltage	I _{OUT} = 2.1mA		0.4		0.4		0.4	V
V _{OH}	Output High Voltage	I _{OUT} = -1.0mA	2.4		2.4		2.4		V

DPS6433-35, -45, -55, -70, -85, -100 DATA RETENTION CHARACTERISTICS						
Symbol	Parameter	Test Condition	Min.	TYP.	Max.	Unit
I _{CCDR2}	Data Retention Supply Current	V _{DR} = 2V, CE ≥ V _{DD} - 0.2V		0.2	0.6	mA
I _{CCDR3}	Data Retention Supply Current	V _{DR} = 3V, CE ≥ V _{DD} - 0.2V		0.5	1.2	mA
t _{CDR}	Chip Disable to Data Retention Time		0			ns
t _R	Recovery Time	t _{rc} = Read Cycle Timing	5			ms

DPS6433-120, -150 DC OPERATING CHARACTERISTICS: Over operating ranges									
Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I _{IN}	Input Leakage Current	V _{IN} = 0V to V _{DD}	-16	+16	-16	+16	-16	+16	μA
I _{OUT}	Output Leakage Current	V _{I/O} = 0V to V _{DD} , CE = V _{IH} or WE = V _{IL}	-16	+16	-16	+16	-16	+16	μA
I _{CC1}	Active Supply Current	CE = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	X32	195		195		195	mA
			X16	105		105		105	
			X8	60		60		60	
I _{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I _{OUT} = 0mA	X32	255		275		295	mA
			X16	135		145		155	
			X8	75		80		85	
I _{SB1}	Full Standby Supply Current (CMOS)	V _{IN} ≥ V _{DD} - 0.2V or V _{IN} ≤ V _{SS} + 0.2V, CE ≥ V _{DD} - 0.2V		1		1.8		2.6	mA
I _{SB2}	Standby Current (TTL)	CE = V _{IH}		20		20		20	mA
V _{OL}	Output Low Voltage	I _{OUT} = 2.1mA		0.4		0.4		0.4	V
V _{OH}	Output High Voltage	I _{OUT} = -1.0mA	2.4		2.4		2.4		V

DPS6433-120, -150 DATA RETENTION CHARACTERISTICS						
Symbol	Parameter	Test Condition	Min.	TYP.	Max.	Unit
I _{CCDR2}	Data Retention Supply Current	V _{DR} = 2V, CE ≥ V _{DD} - 0.2V		6	200	μA
I _{CCDR3}	Data Retention Supply Current	V _{DR} = 3V, CE ≥ V _{DD} - 0.2V		8	220	μA
t _{CDR}	Chip Disable to Data Retention Time		0			ns
t _R	Recovery Time	t _{rc} = Read Cycle Timing	5			ms

RECOMMENDED OPERATING RANGE ¹						
Symbol	Characteristic	Min.	Typ.	Max.	Unit	
V _{DD}	Supply Voltage	4.5	5.0	5.5	V	
V _{IH}	Input HIGH Voltage	2.2		V _{DD} +0.3	V	
V _{IL}	Input LOW Voltage	-0.5 ²		0.8	V	
T _A	Operating Temperature	C	0	+25	+70	°C
		I	-40	+25	+85	
		M/B	-55	+25	+125	

ABSOLUTE MAXIMUM RATINGS ³			
Symbol	Parameter	Value	Unit
T _{STG}	Storage Temperature	-65 to +150	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
V _{DD}	Supply Voltage ¹	-0.5 to +7.0	V
V _{I/O}	Input/Output Voltage ¹	-0.5 to V _{DD} +0.5	V

TRUTH TABLE				
Mode	\overline{CE}	\overline{WE}	I/O Pin	Supply Current
Not Selected	H	X	HIGH-Z	Standby
Read	L	H	D _{OUT}	Active
Write	L	L	D _{IN}	Active

H = HIGH L = LOW X = Don't Care

CAPACITANCE ⁴ : T _A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C _{ADR}	Address Input	80	pF	V _{IN} = 0V
C _{CE}	Chip Enable	20		
C _{WE}	Write Enable	50		
C _{I/O}	Data Input/Output	20		

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5V

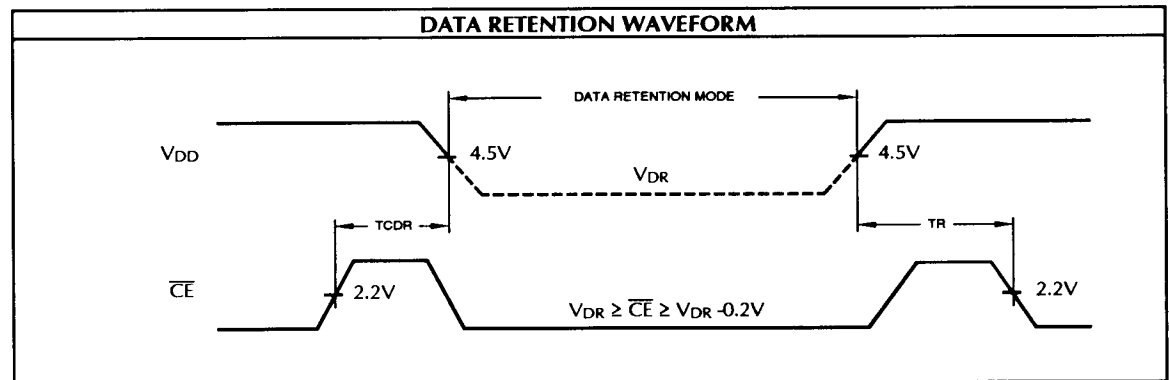
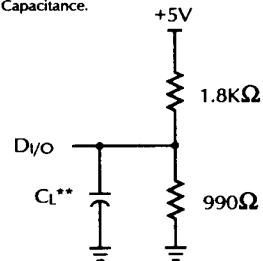
* Transition between 0.8V and 2.2V.

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V _{OH}	HIGH Voltage	I _{OH} = -1.0mA	2.4	-	V
V _{OL}	LOW Voltage	I _{OL} = 2.1mA	-	0.4	V

OUTPUT LOAD		
Load	C _L	Parameters Measured
1	100 pF	except t _{CLZ} , t _{CHZ} , t _{WHZ} , and t _{WLZ}
2	5 pF	t _{CLZ} , t _{CHZ} , t _{WHZ} , and t _{WLZ}

Figure 1. Output Load

** Including Probe and Jig Capacitance.



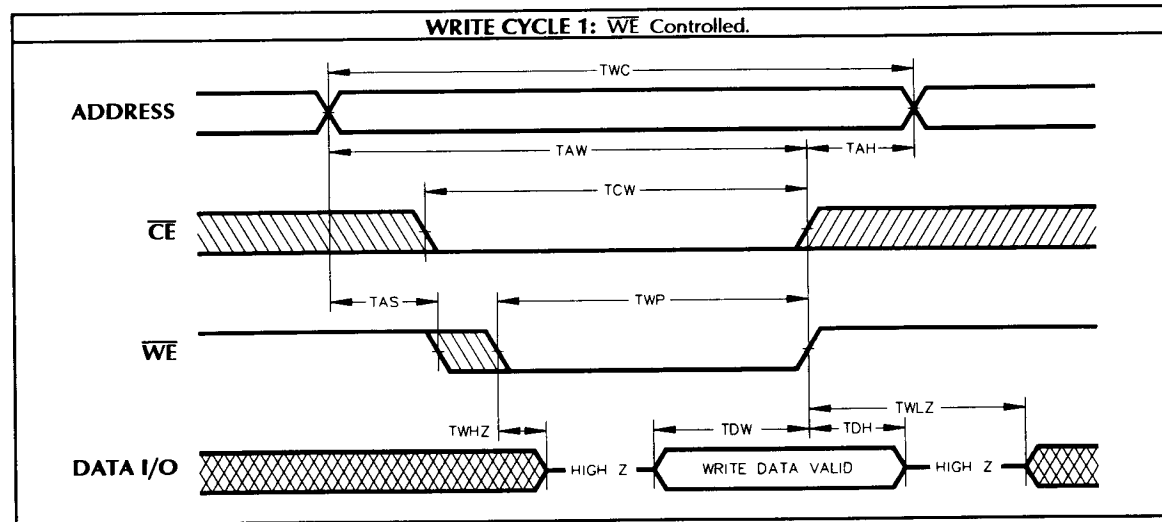
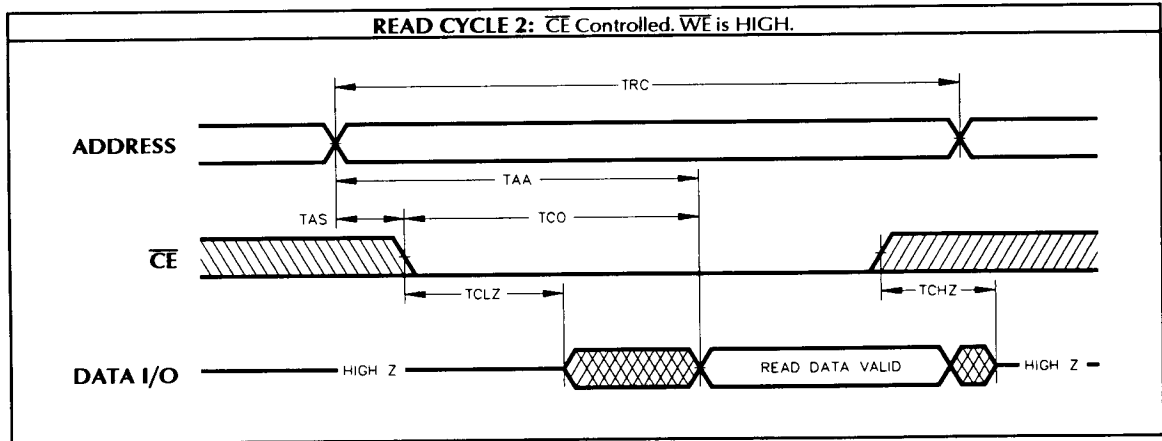
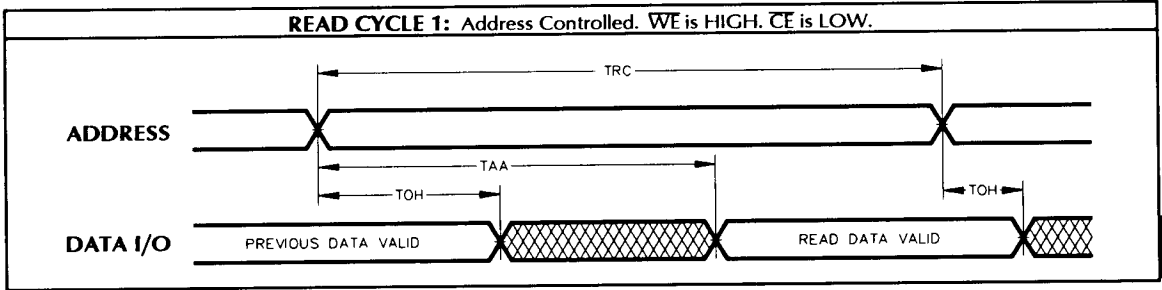
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges											
No.	Symbol	Parameter	-35		-45		-55		-70		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t _{RC}	Read Cycle Time	35		45		55		70		ns
2	t _{AA}	Address Access Time		35		45		55		70	ns
3	t _{CO}	Chip Enable to Output Valid		35		45		55		70	ns
4	t _{OH}	Output Hold from Address Change	3		3		3		3		ns
5	t _{CLZ}	Chip Enable to Output in LOW-Z ^{4, 6}	5		5		5		5		ns
6	t _{CHZ}	Chip Enable to Output in HIGH-Z ^{4, 6}		15		20		25		30	ns

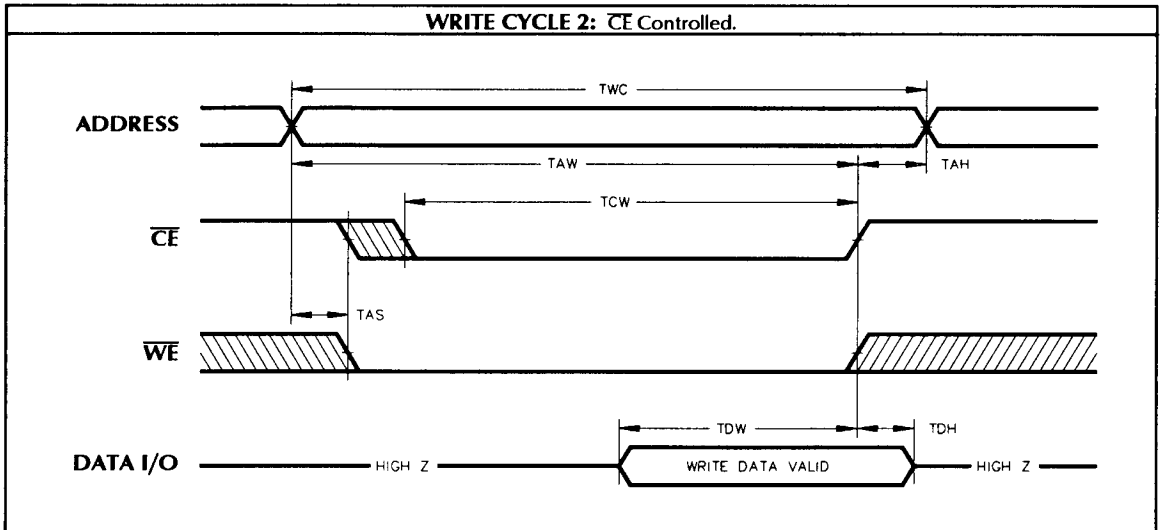
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges ⁷											
No.	Symbol	Parameter	-35		-45		-55		-70		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
7	t _{WC}	Write Cycle Time	35		45		55		70		ns
8	t _{AW}	Address Valid to End of Write	30		40		50		65		ns
9	t _{CW}	Chip Enable to End of Write	30		40		50		65		ns
10	t _{DW}	Data Valid to End of Write	20		25		25		30		ns
11	t _{DH}	Data Hold Time	3		3		3		3		ns
12	t _{WP}	Write Pulse Width	30		40		50		60		ns
13	t _{AS}	Address Set-up Time*	0		0		0		0		ns
14	t _{AH}	Address Hold Time	0		0		0		0		ns
15	t _{WHZ}	Write Enable to Output in HIGH-Z ^{4, 6}		15		20		25		30	ns
16	t _{WLZ}	Write Enable to Output in LOW-Z ^{4, 6}	5		5		5		5		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges											
No.	Symbol	Parameter	-85		-100		-120		-150		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t _{RC}	Read Cycle Time	85		100		120		150		ns
2	t _{AA}	Address Access Time		85		100		120		150	ns
3	t _{CO}	Chip Enable to Output Valid		85		100		120		150	ns
4	t _{OH}	Output Hold from Address Change	5		10		10		10		ns
5	t _{CLZ}	Chip Enable to Output in LOW-Z ^{4, 6}	10		10		10		10		ns
6	t _{CHZ}	Chip Enable to Output in HIGH-Z ^{4, 6}		30		35		40		50	ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges ⁷											
No.	Symbol	Parameter	-85		-100		-120		-150		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
7	t _{WC}	Write Cycle Time	85		100		120		150		ns
8	t _{AW}	Address Valid to End of Write	75		90		100		120		ns
9	t _{CW}	Chip Enable to End of Write	75		90		100		120		ns
10	t _{DW}	Data Valid to End of Write	35		40		50		60		ns
11	t _{DH}	Data Hold Time	0		0		0		0		ns
12	t _{WP}	Write Pulse Width	75		80		90		100		ns
13	t _{AS}	Address Set-up Time*	0		0		0		0		ns
14	t _{AH}	Address Hold Time	0		0		0		0		ns
15	t _{WHZ}	Write Enable to Output in HIGH-Z ^{4, 6}		25		35		40		50	ns
16	t _{WLZ}	Write Enable to Output in LOW-Z ^{4, 6}	5		5		5		5		ns

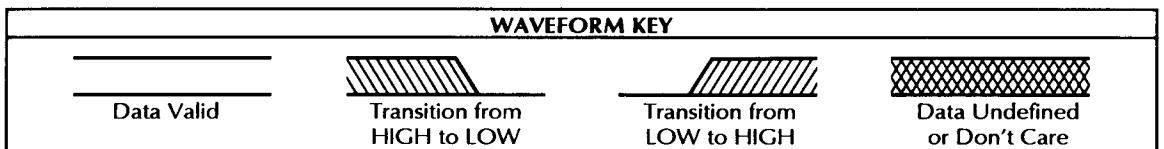
* Valid for both Read and Write Cycles.





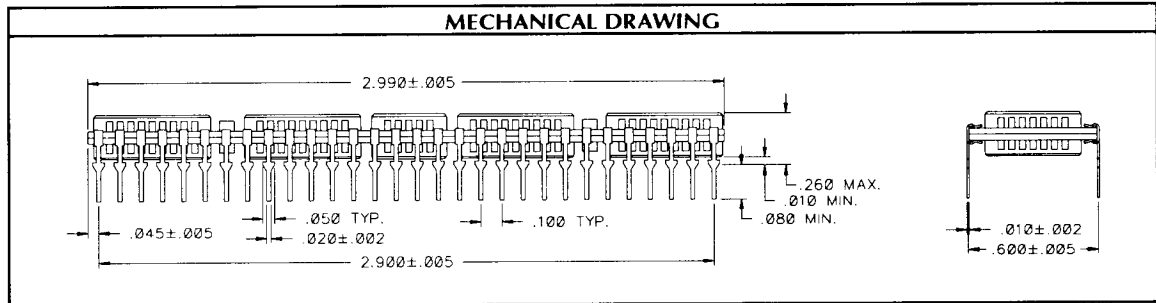
NOTES:

1. All voltages are with respect to V_{SS} .
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ± 500 mV from steady state voltage.
6. When \overline{CE} is LOW and \overline{WE} is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when \overline{WE} is LOW.



ORDERING INFORMATION					
DP	S6433	- XXX	X		
<u>PREFIX</u>	<u>DEVICE TYPE</u>	<u>SPEED</u>	<u>GRADE</u>		
				C	COMMERCIAL 0°C to +70°C
				I	INDUSTRIAL -40°C to +85°C
				M	MILITARY -55°C to +125°C
				B*	MIL-PROCESSED -55°C to +125°C
				35	35ns
				45	45ns
				55	55ns
				70	70ns
				85	85ns
				100	100ns
				120	120ns
				150	150ns
					CMOS SRAM 64KX32, 128KX16 or 256KX8

* B grade modules can be constructed with 883 devices.



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