CAT28C16V3

16K-Bit CMOS POWER MISER™ E²PROM

FEATURES

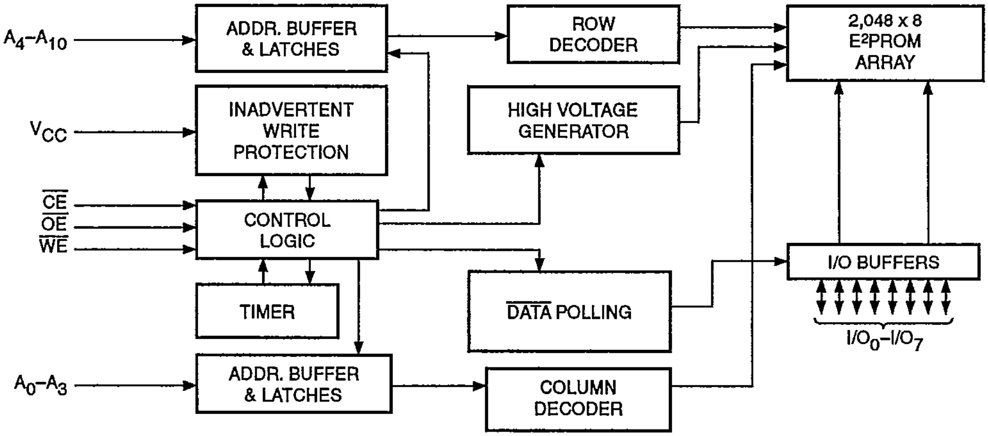
- Fast Read Access Times: 700 ns
- Low Power CMOS Dissipation:
  - –Active: 10mA Max.
  - –Standby: 50µA Max.
- Simple Write Operation:
  - –On-Chip Address and Data Latches
  - –Self-Timed Write Cycle with Auto-Clear
- Fast Nonvolatile Write Cycle: 20ms Max
- End of Write Detection: $\overline{\text{DATA}}$ Polling
- Hardware Write Protection
- CMOS and TTL Compatible I/O
- 10,000 Program/Erase Cycles
- 10 Year Data Retention

DESCRIPTION

The CAT28C16V3 is a fast, low power, 3V-only CMOS E²PROM organized as 2K x 8 bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. $\overline{\text{DATA}}$ Polling signals the start and end of the self-timed write cycle. Additionally, the CAT28C16V3 features hardware write protection.

The CAT28C16V3 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 24 pin DIP and SO or 32 pin PLCC packages.

BLOCK DIAGRAM



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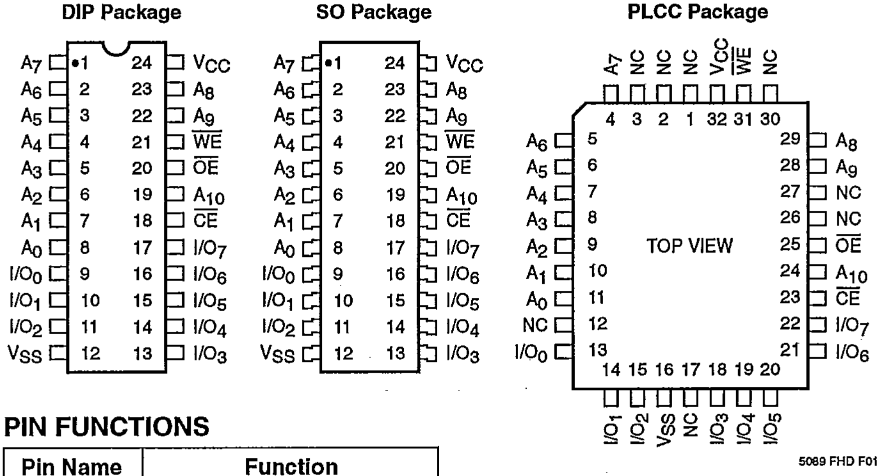
PIN CONFIGURATION



PIN FUNCTIONS

Pin Name	Function
A_0–A_{10}	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	3V Supply
V_{SS}	Ground
NC	No Connect

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte Write ($\overline{WE}$ Controlled)	L	_/	H	D_{IN}	ACTIVE
Byte Write ($\overline{CE}$ Controlled)	_/	L	H	D_{IN}	ACTIVE
Standby, and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

CAPACITANCE $T_A = 25°C$, f = 1.0 MHz, $V_{CC} = 5V$

Symbol	Test	Max.	Units	Conditions
$C_{I/O}^{(1)}$	Input/Output Capacitance	10	pF	$V_{I/O} = 0V$
$C_{IN}^{(1)}$	Input Capacitance	6	pF	$V_{IN} = 0V$

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ....–55°C to +125°C

Storage Temperature ....–65°C to +150°C

Voltage on Any Pin with
Respect to Ground(2) ....–2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ....–2.0V to +7.0V

Package Power Dissipation
Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ....300°C

Output Short Circuit Current(3) ....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(1)	Endurance	10,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(1)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT28C16V3 T_A = 0°C to +70°C, V_{CC} = 3V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CCC}(5)	V_{CC} Current (Operating, CMOS)			10	mA	$\overline{CE} = \overline{OE} = V_{ILC}$, f = 1/$t_{RC}$ min, All I/O's Open
I_{SBC}(6)	V_{CC} Current (Standby, CMOS)			50	µA	$\overline{CE} = V_{IHC}$, All I/O's Open
I_{LI}	Input Leakage Current	–10		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	–10		10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE} = V_{IH}$
V_{IH}(6)	High Level Input Voltage	V_{CC} –0.3		V_{CC} +0.3	V	
V_{IL}(5)	Low Level Input Voltage	–0.3		0.3	V	
V_{OH}	High Level Output Voltage	V_{CC} –0.3			V	I_{OH} = –10µA
V_{OL}	Low Level Output Voltage			0.3	V	I_{OL} = 10mA
V_{WI}	Write Inhibit Voltage	2.0			V	

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} +1V.
(5) V_{ILC} = –0.3V to +0.3V.
(6) V_{IHC} = V_{CC} –0.3V to V_{CC} +0.3V.

A.C. CHARACTERISTICS, Read Cycle

CAT28C16V3 T_A = 0°C to +70°C, V_{CC} = 3V ±10%, unless otherwise specified.

Symbol	Parameter	28C16V3-20		Units
		Min.	Max.	
t_{RC}	Read Cycle Time	700		ns
t_{CE}	$\overline{CE}$ Access Time		700	ns
t_{AA}	Address Access Time		700	ns
t_{OE}	$\overline{OE}$ Access Time		450	ns
$t_{LZ}^{(1)}$	$\overline{CE}$ Low to Active Output	10		ns
$t_{OLZ}^{(1)}$	$\overline{OE}$ Low to Active Output	10		ns
$t_{HZ}^{(1)(7)}$	$\overline{CE}$ High to High-Z Output		80	ns
$t_{OHZ}^{(1)(7)}$	$\overline{OE}$ High to High-Z Output		80	ns
$t_{OH}^{(1)}$	Output Hold from Address Change	100		ns

Figure 1. A.C. Testing Input/Output Waveform(8)

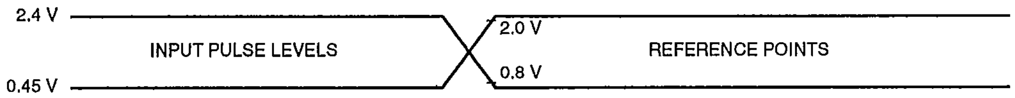


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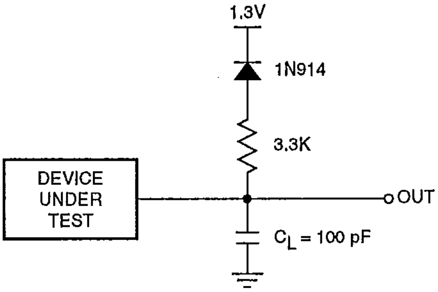
Figure 2. A.C. Testing Load Circuit (example)



C_L INCLUDES JIG CAPACITANCE

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Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(7) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.
(8) Input rise and fall times (10% and 90%) < 10 ns.

A.C. CHARACTERISTICS, Write Cycle

CAT28C16V3 T_A = 0°C to +70°C, V_{CC} = 3V ±10%, unless otherwise specified.

Symbol	Parameter	28C16V3-20		Units
		Min.	Max.	
t_{WC}	Write Cycle Time		20	ms
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time	150		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}(9)	$\overline{CE}$ Pulse Time	200		ns
t_{OES}	$\overline{OE}$ Setup Time	20		ns
t_{OEH}	$\overline{OE}$ Hold Time	20		ns
t_{WP}(9)	$\overline{WE}$ Pulse Width	200		ns
t_{DS}	Data Setup Time	100		ns
t_{DH}	Data Hold Time	20		ns
t_{DL}	Data Latch Time	100		ns
t_{INIT}(1)	Write Inhibit Period After Power-up	10	30	ms

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(9) A write pulse of less than 20ns duration will not initiate a write cycle.

DEVICE OPERATION

Read

Data stored in the CAT28C16V3 is transferred to the data bus when $\overline{\text{WE}}$ is held high, and both $\overline{\text{OE}}$ and $\overline{\text{CE}}$ are held low. The data bus is set to a high impedance state when either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Figure 3. Read Cycle

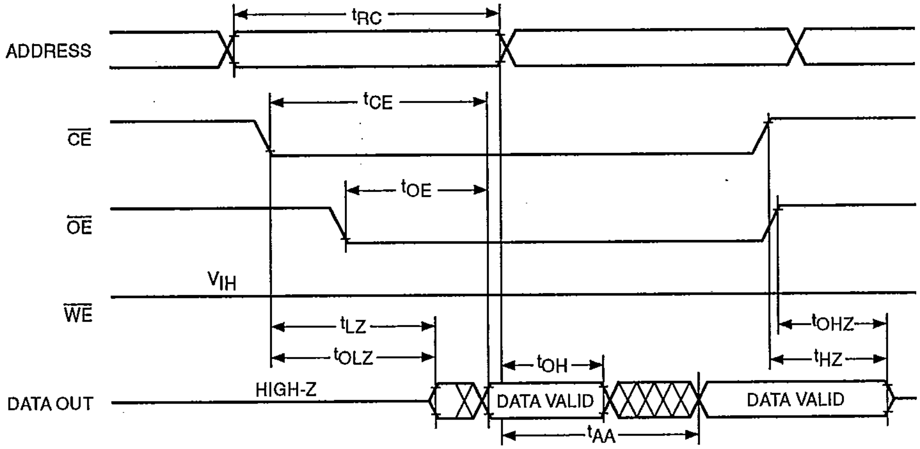

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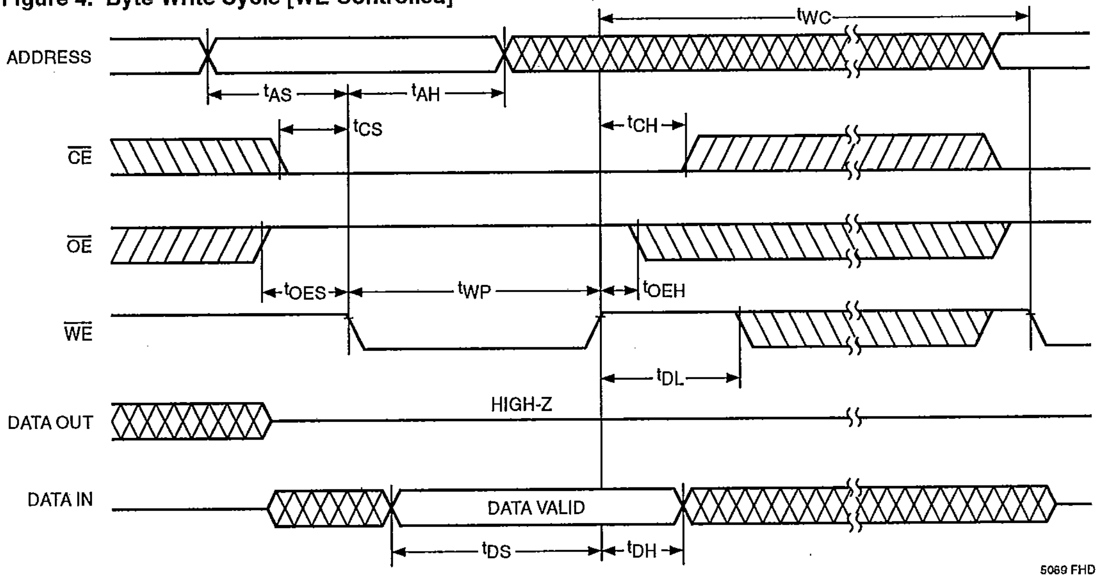
Figure 4. Byte Write Cycle [$\overline{\text{WE}}$ Controlled]



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Byte Write

A write cycle is executed when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be initiated using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 20 ms.

$\overline{\text{DATA}}$ Polling

$\overline{\text{DATA}}$ polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0–I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle, all I/O's will output true data during a read cycle.

Figure 5. Byte Write Cycle [$\overline{\text{CE}}$ Controlled]

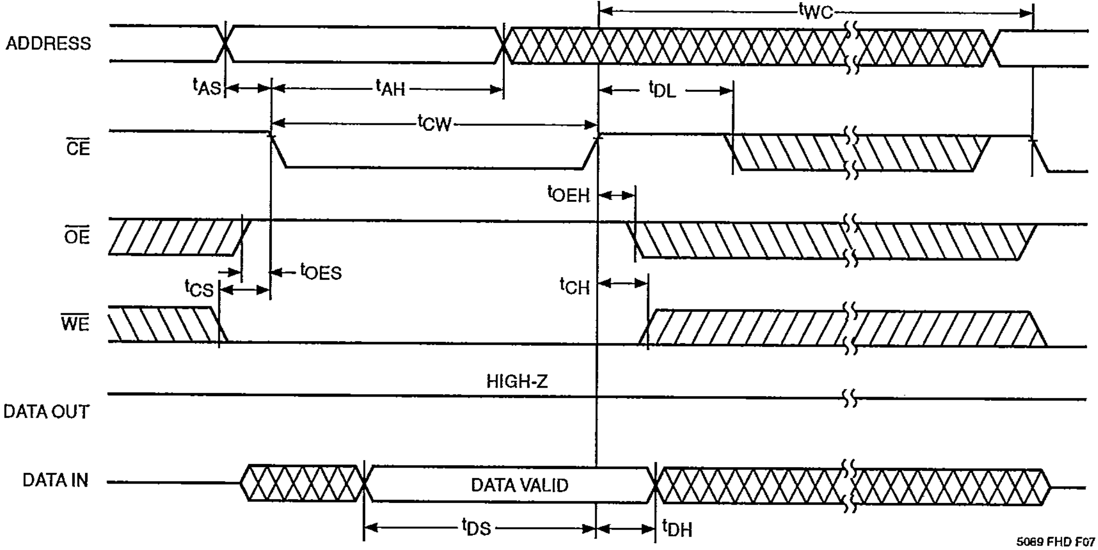
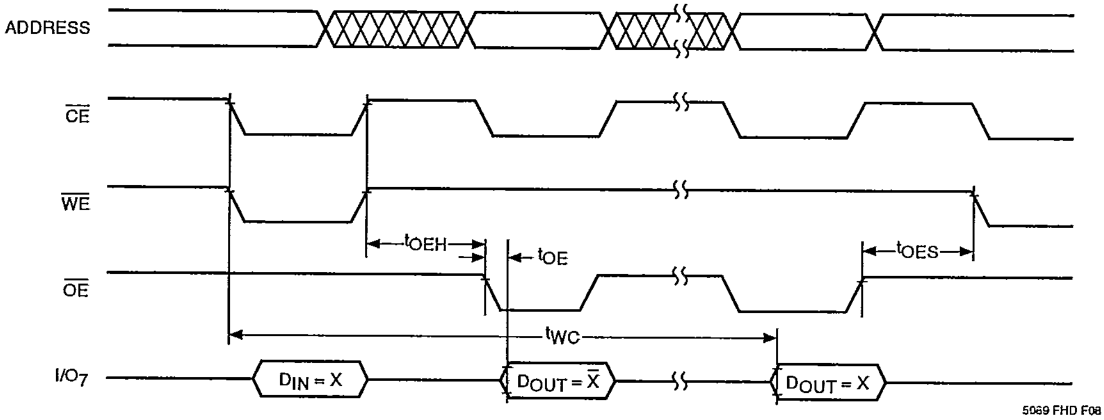


Figure 6. $\overline{\text{DATA}}$ Polling



HARDWARE DATA PROTECTION

The following is a list of hardware data protection features that are incorporated into the CAT28C16V3.

(1) V_{CC} sense provides for write protection when V_{CC} falls below 2.0V min.

(2) A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 10 to 30 ms delay before a write sequence, after V_{CC} has reached 2.0V min.

(3) Write inhibit is activated by holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.

(4) Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs will not result in a write cycle.