ANALOG DEVICES

Complete 12-Bit 5 MSPS Monolithic A/D Converter

SMD/883B AD871

Scope

This specification covers the detail requirements for a complete monolithic 12-bit, 5 Msps A/D converter with an on-chip, high performance track-and-hold amplifier (THA) and voltage reference. The electrical specifications match the Standard Military Drawing (SMD) 5962-94686 in effect at the release of this data sheet. For a copy of the latest official SMD, contact DESC-ELDS.

Part Number/Case Outline

For case outline dimensions, see Package Information Appendix of General Specification ADI-M-1000. The complete part numbers of these SMD and 883 devices are as follows:

Device Type	SMD Part Number	ADI 883 Part Number	Package Description	Package Designation ADI	Package Designation MIL-STD-1835
01	5962-9468601MXA	AD871SD/883B	28-Pin Side Brazed DIP	D-28	CDIP2-T28
02	5962-9468602MYA	AD871SE/883B	44-Terminal LCC	E-44A	CQCCI-N44

Absolute Maximum Ratings (T_A = +25°C unless otherwise noted)[1]

AV_{DD} to AGND ..... −0.5 V to +6.5 V
AV_{SS} to AGND ..... −6.5 V to +0.5 V
DV_{DD}, DRV_{DD}[2] to DGND, DRGND[2] ..... −0.5 V to +6.5 V
DRV_{DD} to DV_{DD}[2] ..... −6.5 V to +6.5 V
DRGND to DGND[2] ..... −0.3 V to +0.3 V
AGND to DGND ..... −1 V to +1 V
AV_{DD} to DV_{DD} ..... −6.5 V to +6.5 V
Clock Input, OEN[2] to DGND ..... −0.5 V to DV_{DD} + 0.5 V
Digital Outputs to DGND ..... −0.5 V to DV_{DD} + 0.3 V
REF IN to AGND ..... AV_{SS} to AV_{DD}
V_{INA}, V_{INB}, REF IN to AGND ..... −6.5 V to +6.5 V
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature Range (Soldering 10 sec) ..... +300°C

Recommended Operating Conditions

Operating Ambient Temperature Range ..... −55°C to +125°C

Thermal Characteristics

Thermal Resistance, Junction-to-Case (θ_{JC}) for D-28 ..... 28°C/W
Thermal Resistance, Junction-to-Ambient (θ_{JA}) for D-28 ..... 60°C/W
Thermal Resistance, Junction-to-Case (θ_{JC}) for E-44A ..... 20°C/W
Thermal Resistance, Junction-to-Ambient (θ_{JA}) for E-44A ..... 70°C/W

NOTES
[1]Permanent damage may occur if any absolute maximum ratings is exceeded. Functional operation is not implied, and device reliability may be impaired by exposure to higher-than-recommended voltages for extended periods of time.
[2]Device Type 02 only.

REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

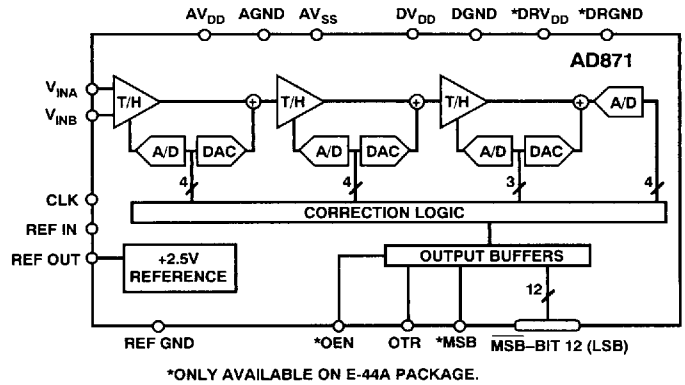
AD871—SPECIFICATIONS

Table 1. Electrical Performance Characteristics[1]

Test	Symbol	Conditions AV_{DD} = +5 V, AV_{SS} = −5 V, DV_{DD} = +5 V, DRV_{DD} = +5 V unless otherwise specified	Group A Subgroups	Device Type	Limits Min	Limits Max	Units
Resolution	RES		1, 2, 3	01, 02	12		Bits
Differential Nonlinearity[2]	DNL	All Codes Histogram	1, 2, 3	01, 02	12		Bits
Zero Error	B_{POE}		1	01, 02		0.75	±% FSR
Gain Error	A_E		1	01, 02		1.25	±% FSR
Zero Error Drift	TCB_{POE}	External 2.5 V Reference	2, 3	01, 02		0.30	±% FSR
Gain Error Drift	TCA_{INT}	Internal 2.5 V Reference	2, 3	01, 02		1.75	±% FSR
Gain Error Drift	TCA_{EXT}	External 2.5 V Reference	2, 3	01, 02		0.5	±% FSR
Power Supply Rejection	PSR	See Note 3	1, 2, 3	01, 02		0.125	±% FSR
Analog Input Range	V_{IN}		1, 2, 3	01, 02		1	±V
Input Resistance	R_{IN}	T_A = +25°C		01, 02	50 typ		kΩ
Input Capacitance	C_{IN}	T_A = +25°C	—	01, 02	10 typ		pF
Internal Reference Output Voltage	V_{REF}		1, 2, 3	01, 02	2.46	2.54	V
Power Dissipation	PD		1, 2, 3	01, 02		1.3	Watts
Power Supply Current	I_{AVDD}		1, 2, 3	01, 02		88	mA
	I_{AVSS}					150	
	I_{DVDD}					21	
	I_{DRVDD}		1, 2, 3	02		2	
Signal-to-Noise and Distortion Ratio	S/(N+D)	f_{IN} = 1 MHz; f_S = 5 MHz	1, 2, 3	01, 02	62		dB
Total Harmonic Distortion	THD	f_{IN} = 1 MHz; f_S = 5 MHz	1, 2, 3	01, 02		−63	dB
Logic Input High Voltage	V_{IH}		1, 2, 3	01, 02	2.0		V
Logic Input Low Voltage	V_{IL}		1, 2, 3	01, 02		0.8	V
Logic Input High Current (CLK)	I_{IH}		1, 2, 3	01		10	±μA
Logic Input Low Current (CLK)	I_{IL}		1, 2, 3	01		10	±μA
Logic Input High Current (OEN, CLK)	I_{IH}		1, 2, 3	02		10	±μA
Logic Input Low Current (OEN, CLK)	I_{IL}		1, 2, 3	02		10	±μA
Logic Output High Voltage ($\overline{MSB}$–Bit 12, OTR)	V_{OH}	I_{SOURCE} = 500 μA	1, 2, 3	01, 02	2.4		V
Logic Output Low Voltage ($\overline{MSB}$–Bit 12, OTR)	V_{OL}	I_{SINK} = 1.6 mA	1, 2, 3	01, 02		0.4	V
Leakage	I_Z	Three-State	1, 2, 3	02		10	±μA
Clock Period	t_C		1, 2, 3	01, 02	200		ns
Output Delay	t_{OD}		1, 2, 3	01, 02	10		ns

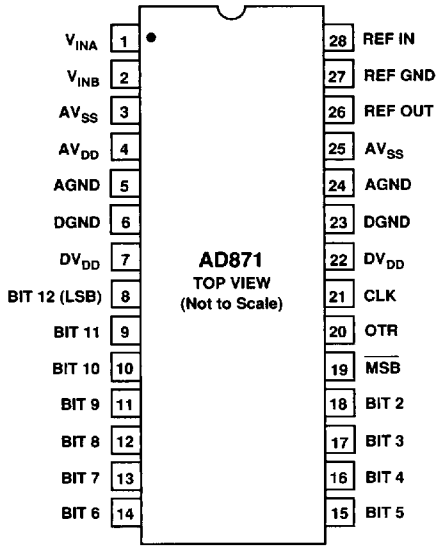
NOTES
[1]See Figure 1 for timing information.
[2]Minimum resolution for which "no missing codes" is guaranteed.
[3]Test conditions for PSR: 4.75 V ≤ AV_{DD} ≤ 5.25 V, −5.25 V ≤ AV_{SS} ≤ −4.75 V, 4.75 V ≤ DV_{DD} ≤ 5.25 V.

Functional Block Diagram and Terminal Assignments

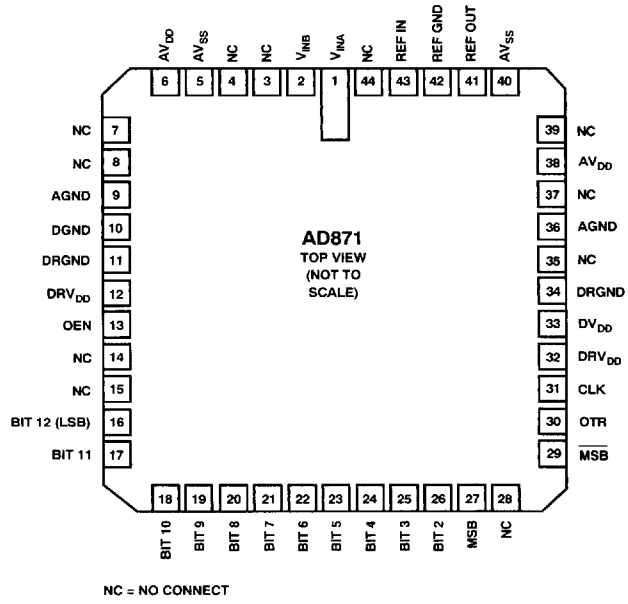


*ONLY AVAILABLE ON E-44A PACKAGE.

D-28 Package



E-44A Package



NC = NO CONNECT

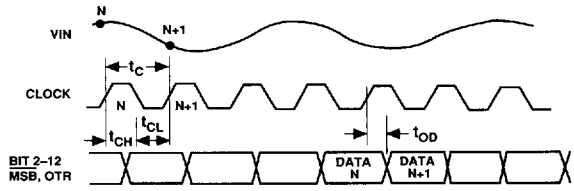


Figure 1. Timing Diagram

SWITCHING SPECIFICATIONS

(T_{MIN} to T_{MAX} with AV_{DD} = +5 V, DV_{DD} = +5 V, DRV_{DD} = +5 V, AV_{SS} = −5 V; V_{IL} = 0.8 V, V_{IH} = 2.0 V. These characteristics are included for design guidance only and are not tested or guaranteed.)

Parameter	Symbol	Limits	Units
CLOCK Pulse Width High	t_{CH}	95	ns min
CLOCK Pulse Width Low	t_{CL}	95	ns min
Clock Duty Cycle		40	% min (50% typ)
		60	% max
Pipeline Delay (Latency)		3	Clock Cycles

Microcircuit Technology Group

This microcircuit is covered by technology group (93).

Life Test/Burn-In Circuit

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).