MOTOROLA

Advance Information

256K x 4 Bit Static Random Access Memory

ELECTRICALLY TESTED PER:
MPG6229A

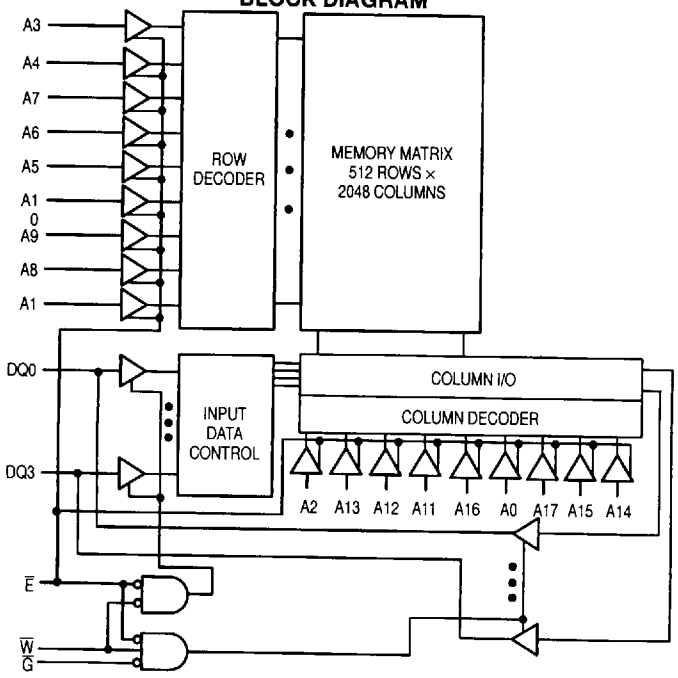
The 6229A is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The 6229A is equipped with both chip enable ($\overline{E}$) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems. These devices also incorporate internal power down circuitry that will reduce active current for less than 100% duty cycle applications. These features provide reduced system power requirements without degrading access time performance.

The 6229A is available in a 600 mil ceramic DIL, 550 x 650 mil surface-mount LCC, or a 490 x 830 mil flat-pack.

- Single 5 V ± 10% Power Supply
- Low Power Operation: 170/150/140/130/120/110/90 mA Maximum, Active AC
- Fast Access Time: 6229A: 20/25/35/45/55/70/100 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible
- Three-State Outputs

BLOCK DIAGRAM



6229A

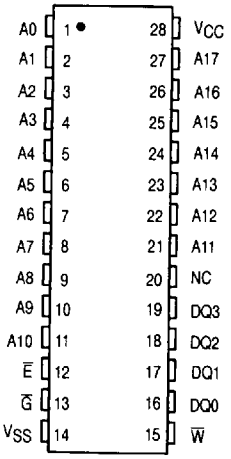
Commercial Plus and Mil/Aero Applications

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 6229A - XX/BXAJC
X = CASE OUTLINE AS FOLLOWS:
PACKAGE: DIL: X
LCC: U
FP: Y
XX = Speed in ns
(25, 30, 35, 45, 55, 70, 100)

The letter "M" appears after the speed on LCC

PIN ASSIGNMENT



PIN NAMES

A0 – A17	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ0 – DQ3	Data Inputs/Outputs
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High-Z	—	I_{SB1}, I_{SB2}
L	H	H	Output Disabled	High-Z	—	I_{CCA}
L	L	H	Read	D_{out}	Read	I_{CCA}
L	X	L	Write	D_{in}	Write	I_{CCA}

H = High, L = Low, X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 25°C)	P_D	1.1	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = - 55 to + 125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns); V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Typ*	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	- 2	2	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	- 2	2	µA
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	I_{CCA}				mA
6229A-20: t_{AVAV} = 25 ns		140	—	170	
6229A-25: t_{AVAV} = 30 ns		120	—	150	
6229A-35: t_{AVAV} = 35 ns		110	—	140	
6229A-45: t_{AVAV} = 45 ns		100	—	130	
6229A-55: t_{AVAV} = 55 ns		90	—	125	
6229A-70: t_{AVAV} = 70 ns		80	—	120	
6229A-100: t_{AVAV} = 100 ns		70	—	110	
AC Standby Current (V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}, f = f_{max})	I_{SB1}	10	—	40	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = 5.5 V, f = 0 MHz)	I_{SB2}	7	—	30	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	—	2.4	—	V

* Typical measurements are taken at 25°C, V_{CC} = 5 V.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQ	C_{in}	6	9	pF
	$\overline{E}$, $\overline{G}$, and $\overline{W}$	C_{ck}	7	10	
Input/Output Capacitance	DQ	$C_{I/O}$	10	14	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = - 55 to + 125°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1a

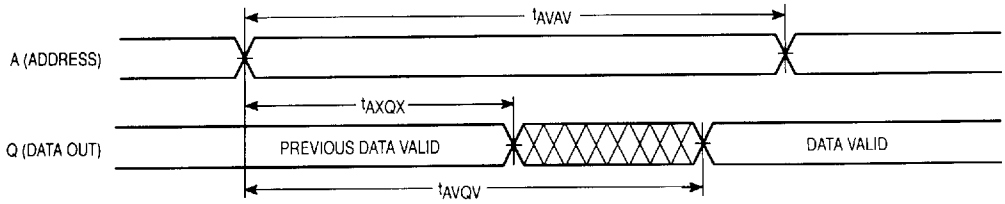
READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol		6229A-25		6229A-30		6229A-35		6229A-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	25	—	30	—	35	—	45	—	ns	2,3
Address Access Time	t_{AVQV}	t_{AA}	—	25	—	30	—	35	—	45	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	25	—	30	—	35	—	45	ns	4
Output Enable Access Time	t_{GLQV}	t_{OE}	—	12	—	10	—	15	—	20	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	0	—	0	—	0	—	0	—	ns	
Enable Low before Output Active	t_{ELQX}	t_{ELZ}	3	—	3	—	3	—	3	—	ns	5,6
Output Enable Low before Output Active	t_{GLQX}	t_{GLZ}	0	—	0	—	0	—	0	—	ns	5,6
Enable High to Output High-Z	t_{EHQZ}	t_{EHZ}	0	10	0	10	0	15	0	20	ns	5,6
Output Enable High to Output High-Z	t_{GHQZ}	t_{ELZ}	0	10	0	10	0	15	0	20	ns	5,6
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	25	—	30	—	35	—	45	ns	

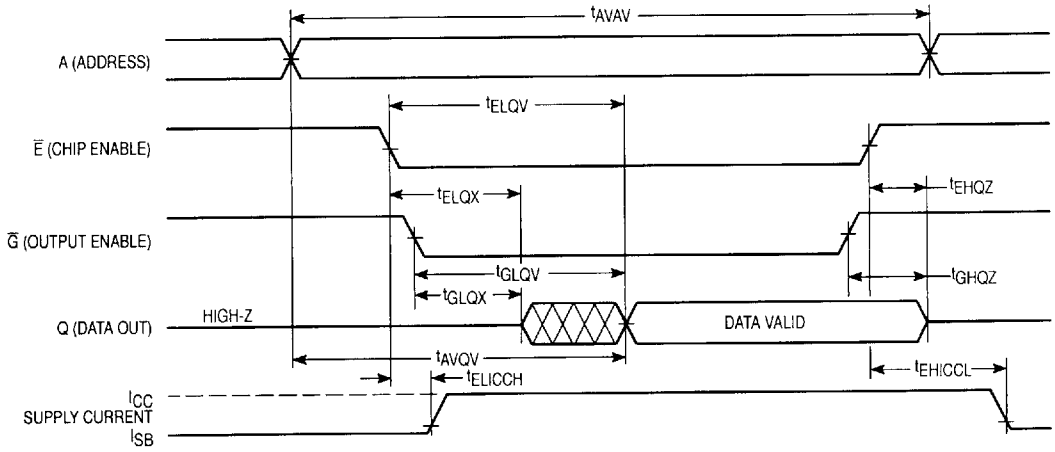
NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

Parameter	Symbol		6229A-55		6229A-70		6229A-100		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	55	—	70	—	100	—	ns	2,3
Address Access Time	t_{AVQV}	t_{AA}	—	55	—	70	—	100	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	55	—	70	—	100	ns	4
Output Enable Access Time	t_{GLQV}	t_{OE}	—	20	—	25	—	25	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	0	—	0	—	0	—	ns	
Enable Low before Output Active	t_{ELQX}	t_{ELZ}	3	—	3	—	3	—	ns	5,6
Output Enable Low before Output Active	t_{GLQX}	t_{GLZ}	0	—	0	—	0	—	ns	5,6
Enable High to Output High-Z	t_{EHQZ}	t_{EHZ}	0	20	0	30	0	30	ns	5,6
Output Enable High to Output High-Z	t_{GHQZ}	t_{ELZ}	0	20	0	30	0	30	ns	5,6
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	55	—	70	—	100	ns	

READ CYCLE 1 (See Notes 1, 2, and 8)



READ CYCLE 2 (See Note 8)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2 and 3)

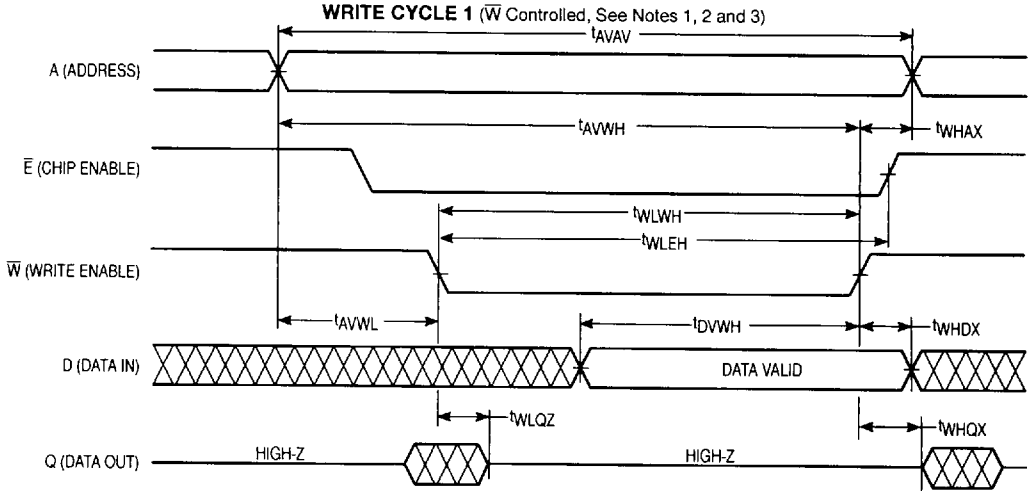
Parameter	Symbol		6229A-25		6229A-30		6229A-35		6229A-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	35	—	45	—	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	17	—	25	—	30	—	35	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	17	—	25	—	30	—	35	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	15	—	20	—	25	—	ns	
Data Write Hold TIme	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Enable Time	t_{WLQZ}	t_{WZ}	0	10	0	10	0	15	0	20	ns	5,6
Write High before Output Active	t_{WHQX}	t_{OW}	0	—	0	—	0	—	0	—	ns	5,6
Write Address Hold Time	t_{WHAX}	t_{WA}	5	—	5	—	5	—	5	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2 and 3)

Parameter	Symbol		6229A-55		6229A-70		6229A-100		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	55	—	70	—	100	—	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	35	—	45	—	45	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	35	—	40	—	40	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	30	—	35	—	40	—	ns	
Data Write Hold TIme	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Enable Time	t_{WLQZ}	t_{WZ}	0	20	0	30	0	35	ns	5,6
Write High before Output Active	t_{WHQX}	t_{OW}	0	—	0	—	0	—	ns	5,6
Write Address Hold Time	t_{WHAX}	t_{WA}	5	—	5	—	5	—	ns	5,6

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2 and 3)



AC TEST LOADS

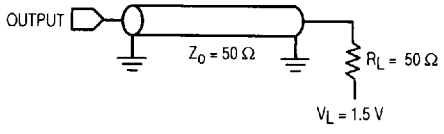


Figure 1a

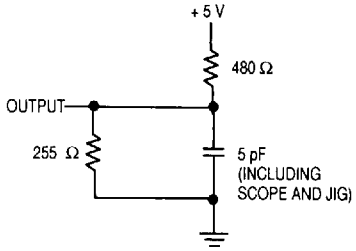


Figure 1b

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2 and 3)

Parameter	Symbol		6229A-25		6229A-30		6229A-35		6229A-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	35	—	45	—	ns	4
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Enable	t_{AVEH}	t_{AE}	17	—	15	—	20	—	25	—	ns	
Enable Write Pulse Width	t_{ELEH}	t_{EP}	17	—	20	—	25	—	35	—	ns	5,6
Enable to End of Write Window	t_{ELWH}	t_{EW}	17	—	20	—	25	—	35	—	ns	
Write to End of Enable Window	t_{WLEH}	t_{WE}	17	—	20	—	25	—	35	—	ns	
Data Valid to End of Enable	t_{DVEH}	t_{DE}	10	—	15	—	20	—	25	—	ns	
Data Enable Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Enable Address Hold Time	t_{EHAX}	t_{EH}	5	—	5	—	5	—	5	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high-impedance state.

Parameter	Symbol		6229A-55		6229A-70		6229A-100		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	35	—	45	—	ns	4
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Enable	t_{AVEH}	t_{AE}	30	—	35	—	40	—	ns	
Enable Write Pulse Width	t_{ELEH}	t_{EP}	35	—	40	—	40	—	ns	5,6
Enable to End of Write Window	t_{ELWH}	t_{EW}	35	—	45	—	45	—	ns	
Write to End of Enable Window	t_{WLEH}	t_{WE}	35	—	45	—	45	—	ns	
Data Valid to End of Enable	t_{DVEH}	t_{DE}	30	—	35	—	40	—	ns	
Data Enable Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	
Enable Address Hold Time	t_{EHAX}	t_{EH}	5	—	5	—	5	—	ns	

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2 and 3)