68020 FEATURES

- Selection of Processor Speeds: 16.67, 20, 25 MHz
- Military Temperature Range: -55°C to +125°C
- Packaging
  - 114 pin Ceramic PGA (P2)
  - 132 lead Ceramic Quad Flatpack, CQFP (Q2)
- Object-code compatible with earlier 68000 Microprocessors
- Addressing mode extensions for enhanced support of high-level languages
- Bit Field Data Type Accelerates Bit-Oriented Applications–i.e., Video Graphics
- Fast On-Chip Instruction Cache Speeds Instructions and Improves Bus Bandwidth
- Coprocessor Interface to Companion 32-Bit Peripherals–the 68881 and 68882 Floating-Point Coprocessors and the 68851 Paged Memory Management Unit
- Pipelined Architecture with High Degree of Internal Parallelism allowing Multiple Instructions to be executed concurrently
- High-Performance Asynchronous Bus Is Nonmultiplexed and Full 32-Bits
- Dynamic Bus Sizing Efficiently Supports 8-/16-/32-Bit Memories and Peripherals
- Full Support of Virtual Memory and Virtual Machine
- 16 32-Bit General-Purpose Data and Address Registers
- Two 32-Bit Supervisor Stack Pointers and Five Special-Purpose Control Registers
- 18 Addressing Modes and 7 Data Types
- 4 GigaByte Direct Addressing Range

DESCRIPTION

The WC32P020 is a 32-bit implementation of the 68000 Family of microprocessors. Using HCMOS technology, the WC32P020 is implemented with 32-bit registers and data paths, 32-bit addresses, a powerful instruction set, and flexible addressing modes.

FIG. 1
BLOCK DIAGRAM

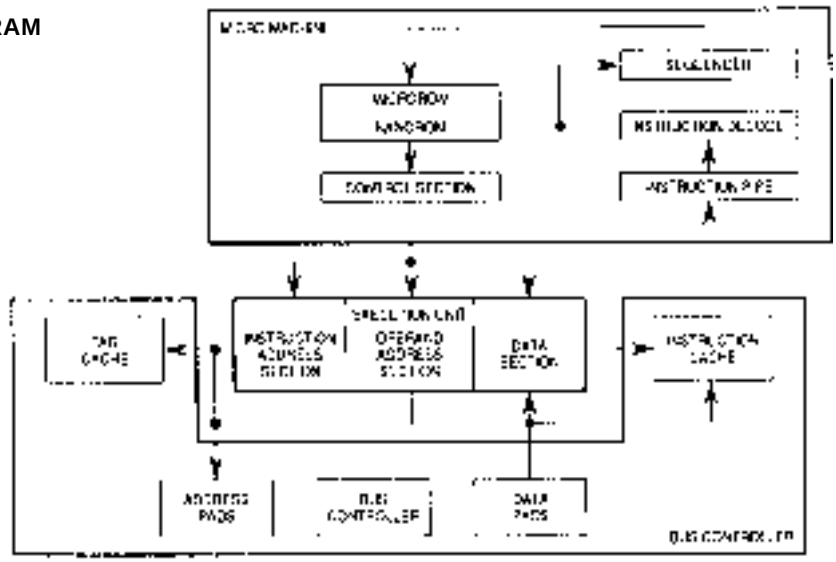


FIG. 2 PIN CONFIGURATION FOR WC32P020-XXM, CQFP (Q2)

TOP VIEW

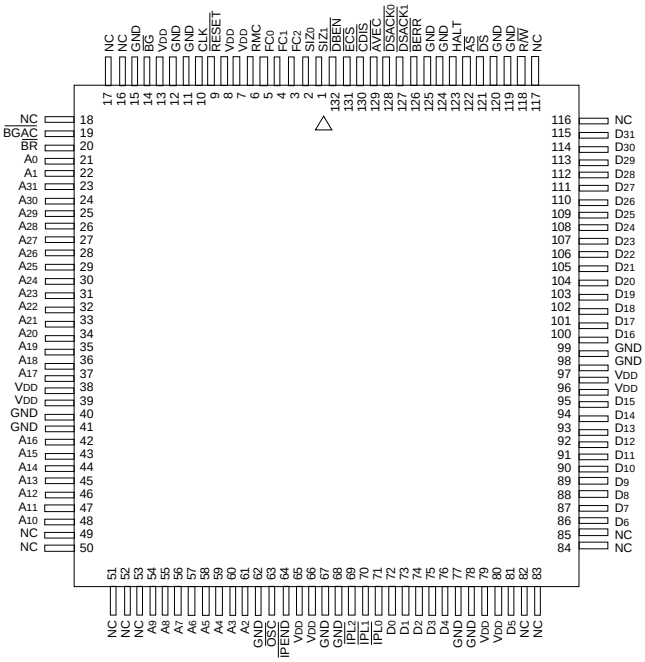
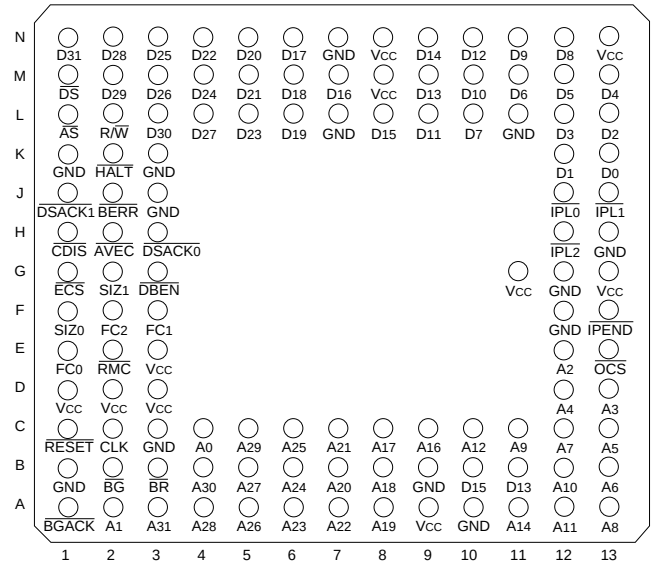


FIG. 3 PIN CONFIGURATION FOR WC32P020-XXM, PGA (P2)



ADDRESSING MODES

Addressing	Syntax
Register Direct	
Data Register Direct	Dn
Address Register Direct	An
Register Indirect	
Address Register Indirect	(An)
Address Register Indirect with Postincrement	(An) +
Address Register Indirect with Predecrement	- (An)
Address Register Indirect with Displacement	(d_{16},An)
Register Indirect with Index	
Address Register Indirect with Index (8-Bit Displacement)	(d_8,An,Xn)
Address Register Indirect with Index (Base Displacement)	(bd,An,Xn)
Memory Indirect	
Memory Indirect Postindexed	([bd,An],Xn,od)
Memory Indirect Preindexed	([bd,An,Xn],od)
Program Counter Indirect with Displacement	(d_{16},PC)
Program Counter Indirect with Index	
PC Indirect with Index (8-Bit Displacement)	(d_8,PC,Xn)
PC Indirect with Index (Base Displacement)	(bd,PC,Xn)
Program Counter Memory Indirect	
PC Memory Indirect Postindexed	([bd,PC],Xn,od)
PC Memory Indirect Preindexed	([bd,PC,Xn],od)
Absolute	
Absolute Short	(xxx).W
Absolute Long	(xxx).L
Immediate	#(data)

NOTES:

Dn = Data Register, DO-D7

An = Address Register, AO-A7

d_8, d_{16} = A twos-complement or sign-extended displacement; added as part of the effective address calculation; size is 8 (d8) or 16 (d16) bits; when omitted, assemblers use a value of zero.

Xn = Address or data register used as an index register; form is Xn.SIZE*SCALE, where SIZE is.W or .L (indicates index register size) and SCALE is 1, 2, 4, or 8 (index register is multiplied by SCALE); use of SIZE and/or SCALE is optional.

bd = A twos-complement base displacement; when present, size can be 16 or 32 bits.

od = Outer displacement, added as part of effective address calculation after any memory indirection, use is optional with a size of 16 or 32 bits.

PC = Program Counter

(data) = Immediate value of 8, 16, or 32 bits

( ) = Effective Address

[ ] = Use as indirect access to long-word address.

INSTRUCTION SET

Mnemonic	Description
ABCD	Add Decimal with Extend
ADD	Add
ADDA	Add Address
ADDI	Add Immediate
ADDQ	Add Quick
ADDX	Add with Extend
AND	Logical AND
ANDI	Logical AND Immediate
ASL, ASR	Arithmetic Shift Left and Right
Bcc	Branch Conditionally
BCHG	Test Bit and Change
BCLR	Test Bit and Clear
BFCHG	Test Bit Field and Change
BFCLR	Test Bit Field and Clear
BFEXTS	Signed Bit Field Extract
BFEXTU	Unsigned Bit Field Extract
BFFFO	Bit Field Find First One
BFINS	Bit Field Insert
BFSET	Test Bit Field and Set
BFTST	Test Bit Field
BKPT	Breakpoint
BRA	Branch
BSET	Test Bit and Set
BSR	Branch to Subroutine
BTST	Test Bit
CALLM	Call Module
CAS	Compare and Swap Operands
CAS2	Compare and Swap Dual Operands
CHK	Check Register Against Bound
CHK2	Check Register Against Upper and Lower Bounds
CLR	Clear
CMP	Compare
CMPA	Compare Address
CMPI	Compare Immediate
CMPM	Compare Memory to Memory
CMP2	Compare Register Against Upper and Lower Bounds
DBcc	Test Condition, Decrement and Branch
DIVS, DIVSL	Signed Divide
DIVU, DIVUL	Unsigned Divide
EOR	Logical Exclusive OR
EORI	Logical Exclusive OR Immediate
EXG	Exchange Registers
EXT, EXTB	Sign Extend
ILLEGAL	Take Illegal Instruction Trap
JMP	Jump
JSR	Jump to Subroutine
LEA	Load Effective Address
LINK	Link and Allocate
LSL, LSR	Logical Shift Left and Right
MOVE	Move
MOVEA	Move Address
MOVE CCR	Move Condition Code Register
MOVE SR	Move Status Register
MOVE USP	Move User Stack Pointer
MOVEC	Move Control Register
MOVEM	Move Multiple Registers
MOVEP	Move Peripheral
MOVEQ	Move Quick
MOVES	Move Alternate Address Space
MULS	Signed Multiply
MULU	Unsigned Multiple

INSTRUCTION SET (cont.)

Mnemonic	Description
NBCD	Negate Decimal with Extend
NEG	Negate
NEGX	Negate with Extend
NOP	No Operation
NOT	Logical Complement
OR	Logical Inclusive OR
ORI	Logical Inclusive OR Immediate
ORI CCR	Logical Inclusive OR Immediate to Condition Codes
ORI SR	Logical Inclusive OR Immediate to Status Register
PACK	Pack BCD
PEA	Push Effective Address
RESET	Reset External Devices
ROL, ROR	Rotate Left and Right
ROXL, ROXR	Rotate with Extend Left and Right
RTD	Return and Deallocate
RTE	Return from Exception
RTM	Return from Module
RTR	Return and Restore Codes
RTS	Return from Subroutine
SBCD	Subtract Decimal with Extend
Scc	Set Conditionally
STOP	Stop
SUB	Subtract
SUBA	Subtract Address
SUBI	Subtract Immediate
SUBQ	Subtract Quick
SUBX	Subtract with Extend
SWAP	Swap Register Words
TAS	Test Operand and Set
TRAP	Trap
TRAPcc	Trap Conditionally
TRAPV	Trap on Overflow
TST	Test Operand
UNLK	Unlink
UNPK	Unpack BCD

Coprocessor Instructions

Mnemonic	Description
cpBcc	Branch Conditionally
cpDBcc	Test Coprocessor Condition, Decrement and Branch
cpGEN	Coprocessor General Instruction

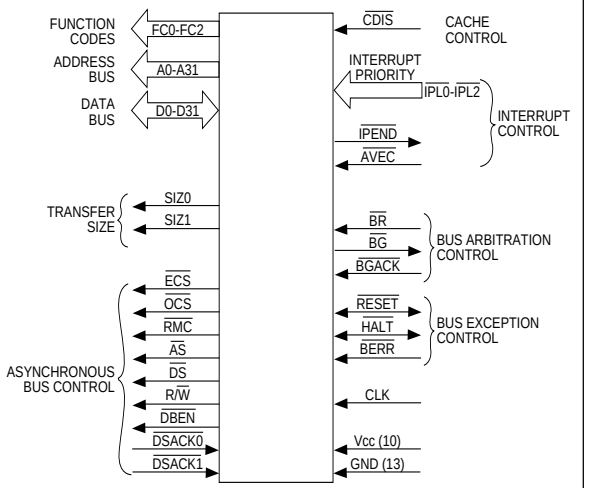
Mnemonic	Description
cpRESTORE	Restore Internal State of Coprocessor
cpSAVE	Save Internal State of Coprocessor
cpScc	Set Conditionally
cpTRAPcc	Trap Conditionally

SIGNAL DESCRIPTION

The Vcc and GND pins are separated into four groups to provide individual power supply connections for the address bus buffers, data bus buffers, and all other buffers and internal logic. See Fig. 4.

Group	Vcc	GND
Address Bus	A9, D3	A10, B9, C3, F12
Data Bus	M8, N8, N13	L7, L11, N7, K3
Logic	D1, D2, E3, G11, G13	G12, H13, J3, K1
Clock	—	B1

FIG. 4
FUNCTIONAL SIGNAL GROUPS



SIGNAL INDEX

Signal Name	Mnemonic	Function
Function Codes	FC2-FC0	3-bit function code used to identify the address space of each bus cycle.
Address Bus	A0-A31	32-bit address bus.
Data Bus	D0-D31	32-bit data bus used to transfer 8, 16, 24, or 32 bits of data per bus cycle.
Size	SIZ0/SIZ1	Indicates the number of bytes remaining to be transferred for this cycle. These signals, together with A1 and A0, define the active sections of the data bus.
External Cycle Start	$\overline{ECS}$	Provides an indication that a bus cycle is beginning.
Operand Cycle Start	$\overline{OCS}$	Identical operation to that of ECS except that OCS is asserted only during the first bus cycle of an operand transfer.
Read,Write	R/$\overline{W}$	Defines the bus transfer as a processor read or write.
Read-Modify-Write Cycle	$\overline{RMC}$	Provides an indicator that the current bus cycle is part of an indivisible read-modify-write operation.
Address Strobe	$\overline{AS}$	Indicates that a valid address is on the bus.
Data Strobe	$\overline{DS}$	Indicates that valid data is to be placed on the data bus by an external device or has been placed on the data bus by the WC32P020-XXM.
Data Buffer Enable	$\overline{DBEN}$	Provides an enable signal for external data buffers.
Data Transfer and Size Acknowledge	$\overline{DSACK0}$/$\overline{DSACK1}$	Bus response signals that indicate the requested data transfer operation has completed. In addition, these two lines indicate the size of the external bus port on a cycle-by-cycle basis and are used for asynchronous transfers.
Interrupt Priority Level	$\overline{IPL0}$-$\overline{IPL2}$	Provides an encoded interrupt level to the processor.
Interrupt Pending	$\overline{IPEND}$	Indicates that an interrupt is pending.
Autovector	$\overline{AVEC}$	Requests an autovector during an interrupt acknowledge cycle.
Bus Request	$\overline{BR}$	Indicates that an external device requires bus mastership.
Bus Grant	$\overline{BG}$	Indicates that an external device may assume bus mastership.
Bus Grant Acknowledge	$\overline{BGACK}$	Indicates that an external device has assumed bus mastership.
Reset	$\overline{RESET}$	System reset.
Halt	$\overline{HALT}$	Indicates that the processor should suspend bus activity.
Bus Error	$\overline{BERR}$	Indicates that an erroneous bus operation is being attempted.
Cache Disable	$\overline{CDIS}$	Dynamically disables the on-chip cache to assist emulator support
Clock	CLK	Clock input to the processor.
Power Supply	Vcc	Power supply.
Ground	GND	Ground connection.

MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
Vcc	Supply voltage	-0.3	+7.0	V
V_I	Input voltage	-0.3	+7.0	V
Pdmax	Max Power dissipation		2.0	W
Tcase	Operating temperature (Mil.)	-55	+125	°C
Tcase	Operating temperature (Ind.)	-40	+85	°C
Tstg	Storage temperature	-55	+150	°C
Tj	Junction temperature		+160	°C

THERMAL CHARACTERISTICS
(with no heat sink or airflow)

Characteristic	Symbol	Value	Rating
Thermal Resistance — Junction to Ambient	θ_{JA}		°C/W
PGA Package		26	
CQFP Package		46	
Thermal Resistance — Junction to Case	θ_{JC}		°C/W
PGA Package		3	
CQFP Package		15	

POWER CONSIDERATIONS

The average chip junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D = P_{INT}+$P_{I/O}$

P_{INT} = I_{CC} x V_{CC}, Watts-Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins-User Determined

For most applications, $P_{I/O}<P_{INT}$ and can be neglected.

The following is an approximate relationship between PD and TJ (if $P_{I/O}$ is neglected):

$$PD = K \div (T_J + 273°C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = PD \bullet (TA + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring PD (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case) surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling, and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 V_{DC} ±5%, GND = 0 V_{DC}, T_A = -55°C to +125°C)

Characteristics		Symbol	Min	Max	Unit
Input High Voltage		V_{IH}	2.0	Vcc	V
Input Low Voltage		V_{IL}	GND -0.5	0.8	V
Input Leakage Current GND ≤ V_{IN} ≤ Vcc	$\overline{BERR}$, $\overline{BR}$, $\overline{BGACK}$, CLK, $\overline{IPL_{0-2}}$, $\overline{AVEC}$, $\overline{CDIS}$, $\overline{DSACK0}$, $\overline{DSACK1}$ $\overline{HALT}$, $\overline{RESET}$	I_{IN}	-4 -20	4.0 20	µA
High-Z (Off State) Leakage Current	A_{31-0}, $\overline{AS}$, $\overline{DBEN}$, $\overline{DS}$, D_{31-0}, FC_{2-0} R/$\overline{W}$, $\overline{RMC}$, SIZ_{1-0}	I_{TSI}	-20	20	µA
Output High Voltage	A_{31-0}, $\overline{AS}$, $\overline{BG}$, D_{31-0}, $\overline{DBEN}$, $\overline{DS}$, $\overline{ECS}$, R/$\overline{W}$, $\overline{IPEND}$, $\overline{OCS}$, $\overline{RMC}$, SIZ_{1-0}, FC_{2-0}	V_{OH}	2.4	-	V
Output Low Voltage I_{OL} = 3.2 mA I_{OL} = 5.3 mA I_{OL} = 2.0 mA I_{OL} = 10.7 mA	 A_{31-0}, FC_{2-0}, SIZ_{1-0}, $\overline{BG}$, D_{31-0} $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, $\overline{RMC}$, $\overline{DBEN}$, $\overline{IPEND}$ $\overline{ECS}$, $\overline{OCS}$ $\overline{HALT}$, $\overline{RESET}$	V_{OL}	 - - - -	 0.5 0.5 0.5 0.5	V
Maximum Supply Current		I_{CC}	-	333	mA
Capacitance (1) V_{IN} = 0V, T_A = 25°C, f = 1MHz		C_{IN}	-	20	pF
Load Capacitance	$\overline{ECS}$, $\overline{OCS}$ All Other	C_L	-	50 130	pF

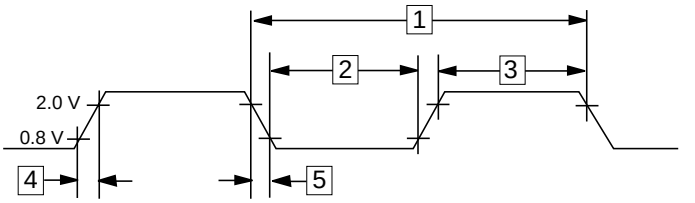
NOTES:

1. Capacitance is guaranteed by design but not tested.

AC ELECTRICAL SPECIFICATIONS – CLOCK INPUT (see Fig. 5)

Characteristic	Specification	16.67 MHz		20 MHz		25MHz		Unit
		Min	Max	Min	Max	Min	Max	
Frequency of Operation		8	16.67	12.5	20	12.5	25	MHz
Cycle Time	1	60	125	50	80	40	80	ns
Clock Pulse Width	2,3	24	95	20	54	19	61	ns
Rise and Fall Times	4,5	–	5	–	5	–	4	ns

FIG.5
CLOCK INPUT TIMING DIAGRAM



NOTE:

Timing measurements are referenced to and from a low 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8V and 2.0V.

AC ELECTRICAL SPECIFICATIONS – READ AND WRITE CYCLES

(V_{CC} = 5.0 V_{DC} ±5%, GND = 0 V_{DC}, T_A = -55°C to +125°C)

Characteristic	Specification	16.67 MHz		20 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock high to Address, FC, Size, $\overline{RMC}$ Valid	6	0	30	0	25	0	25	ns
Clock High to $\overline{ECS}$, $\overline{OCS}$ Asserted	6A	0	20	0	15	0	12	ns
Clock High to Address, Data, FC, Size, $\overline{RMC}$, High Impedance	7	0	60	0	50	0	40	ns
Clock high to Address, FC, Size, $\overline{RMC}$ Invalid	8	0	-	0	-	0	-	ns
Clock Low to $\overline{AS}$, $\overline{DS}$ Asserted	9	1	30	1	25	1	18	ns
$\overline{AS}$ to $\overline{DS}$ Assertion (Read) (Skew)	9A (1)	-15	15	-10	10	-10	10	ns
$\overline{AS}$ Asserted to $\overline{DS}$ Asserted (Write)	9B (11)	37	-	32	-	27	-	ns
$\overline{ECS}$ Width Asserted	10	20	-	15	-	15	-	ns
$\overline{OCS}$ Width Asserted	10	20	-	15	-	15	-	ns
$\overline{ECS}$, $\overline{OCS}$ width Negated	10B (7)	15	-	10	-	5	-	ns
Address, FC, Size, $\overline{RMC}$, Valid to $\overline{AS}$ (and $\overline{DS}$ Asserted Read)	11	15	-	10	-	6	-	ns
Clock Low to $\overline{AS}$, $\overline{DS}$ Negated	12	0	30	0	25	0	15	ns
Clock Low to $\overline{ECS}$, $\overline{OCS}$ Negated	12A	0	30	0	25	0	15	ns
$\overline{AS}$, $\overline{DS}$ Negated to Address, FC, Size, $\overline{RMC}$ Invalid	13	15	-	10	-	10	-	ns
$\overline{AS}$ (and $\overline{DS}$ Read) Width Asserted	14	100	-	85	-	70	-	ns
$\overline{DS}$ Width Asserted Write	14A	40	-	38	-	30	-	ns
$\overline{AS}$, $\overline{DS}$ Width Negated	15	40	-	38	-	30	-	ns
$\overline{DS}$ Negated to $\overline{AS}$ Asserted	15A (8)	35	-	30	-	25	-	ns
Clock High to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Invalid, High Impedance	16	-	60	-	50	-	40	ns
$\overline{AS}$, $\overline{DS}$ Negated to R/$\overline{W}$ Invalid	17	15	-	10	-	10	-	ns
Clock High to R/$\overline{W}$ High	18	0	30	0	25	0	20	ns
Clock High to R/$\overline{W}$ Low	20	0	30	0	25	0	20	ns
R/$\overline{W}$ High to $\overline{AS}$ Asserted	21	15	-	10	-	5	-	ns
R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write)	22	75	-	60	-	50	-	ns
Clock High to Data Out Valid	23	-	30	-	25	-	25	ns
$\overline{DS}$ Negated to Data Out Invalid	25	15	-	10	-	5	-	ns
$\overline{DS}$ Negated to $\overline{DBEN}$ Negated (Write)	25A (9)	15	-	10	-	5	-	ns
Data Out Valid to $\overline{DS}$ Asserted (Write)	26	15	-	10	-	5	-	ns
Data-In Valid to Clock Low (Data Setup)	27	5	-	5	-	5	-	ns
Late $\overline{BERR}$/$\overline{HALT}$ Asserted to Clock Low Setup Time	27A	20	-	15	-	10	-	ns
$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DSACKx}$, $\overline{BERR}$, $\overline{HALT}$, $\overline{AVEC}$ Negated	28	0	80	0	65	0	50	ns
$\overline{DS}$ Negated to Data-In Invalid (Data-In Hold Time)	29	0	-	0	-	0	-	ns
$\overline{DS}$ Negated to Data-In (High Impedance)	29A	-	60	-	50	-	40	ns
$\overline{DSACKx}$ Asserted to Data-In Valid	31 (2)	-	50	-	43	-	32	ns
$\overline{DSACKx}$ Asserted to $\overline{DSACKx}$ Valid ($\overline{DSACK}$ Asserted Skew)	31A (3)	-	15	-	10	-	10	ns
$\overline{RESET}$ Input Transition Time	32	-	1.5	-	1.5	-	1.5	Clks
Clock Low to $\overline{BG}$ Asserted	33	0	30	0	25	0	20	ns
Clock Low to $\overline{BG}$ Negated	34	0	30	0	25	0	20	ns
$\overline{BR}$ Asserted to $\overline{BG}$ Asserted ($\overline{RMC}$ Not Asserted)	35	1.5	3.5	1.5	3.5	1.5	3.5	Clks
$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	37	1.5	3.5	1.5	3.5	1.5	3.5	Clks

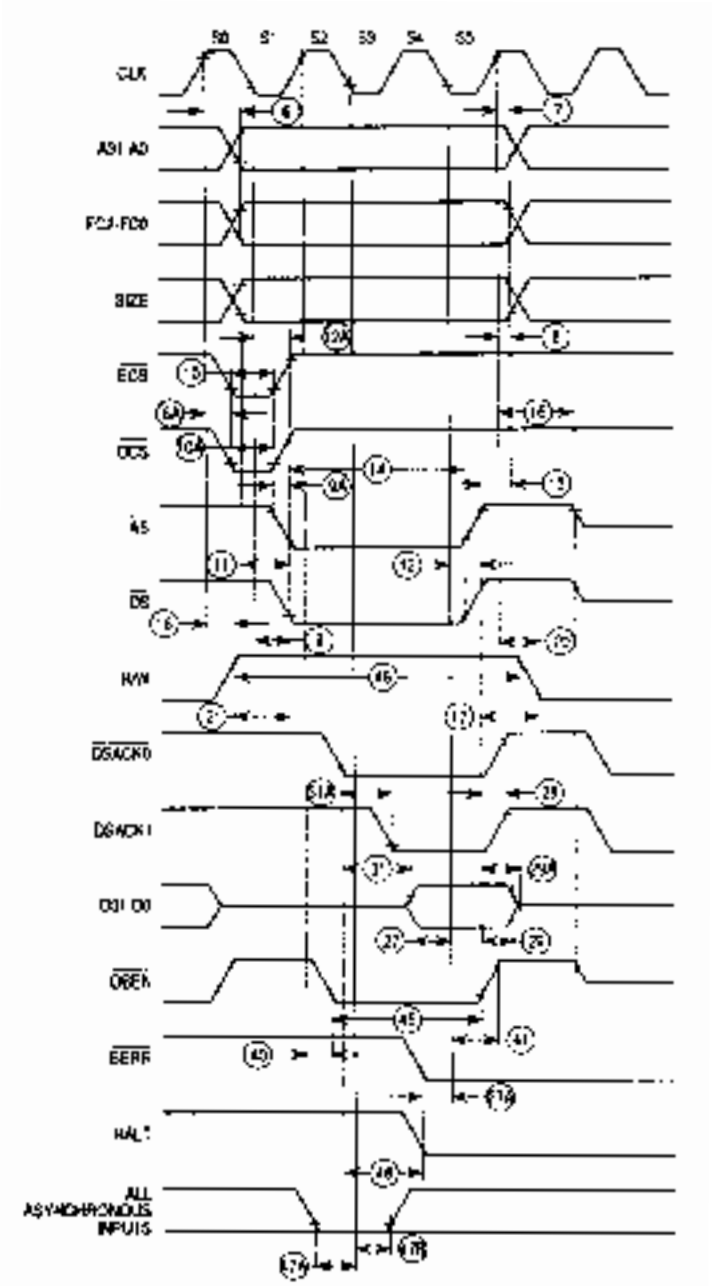
AC ELECTRICAL SPECIFICATIONS – READ AND WRITE CYCLES (cont.)

Characteristic	Specification	16.67 MHz		20 MHz		25MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{BGACK}$ Asserted to $\overline{BR}$ Negated	37A (6)	0	1.5	0	1.5	0	1.5	Clks
$\overline{BG}$ Width Negated	39	90	-	75	-	60	-	ns
$\overline{BG}$ Width Asserted	39A	90	-	75	-	60	-	ns
Clock High to $\overline{DBEN}$ Asserted (Read)	40	0	30	0	25	0	20	ns
Clock High to $\overline{DBEN}$ Negated (Read)	41	0	30	0	25	0	20	ns
Clock High to $\overline{DBEN}$ Asserted (Write)	42	0	30	0	25	0	20	ns
Clock High to $\overline{DBEN}$ Negated (Write)	43	0	30	0	25	0	20	ns
R/$\overline{W}$ Low to $\overline{DBEN}$ Asserted (Write)	44	15	-	10	-	10	-	ns
$\overline{DBEN}$ Width Asserted Read	45 (5)	60	-	50	-	40	-	ns
Write		120	-	100	-	80	-	
R/$\overline{W}$ Width Valid (Write or Read)	46	150	-	125	-	100	-	ns
Asynchronous Input Setup Time	47A	5	-	5	-	5	-	ns
Asynchronous Input Hold Time	47B	15	-	15	-	10	-	ns
$\overline{DSACK}$x Asserted to $\overline{BERR}$, $\overline{HALT}$ Asserted	48 (4)	-	30	-	20	-	18	ns
Data Out Hold from Clock High	53	0	-	0	-	0	-	ns
R/$\overline{W}$ Valid to Data Bus Impedance Change	55	30	-	25	-	20	-	ns
$\overline{RESET}$ Pulse Width (Reset Instruction)	56	512	-	512	-	512	-	Clks
$\overline{BERR}$ Negated to $\overline{HALT}$ Negated (Rerun)	57	0	-	0	-	0	-	ns
$\overline{BGACK}$ Negated to Bus Driven	58 (10)	1	-	1	-	1	-	Clks
$\overline{BG}$ Negated to Bus Driven	59 (10)	1	-	1	-	1	-	Clks

NOTES:

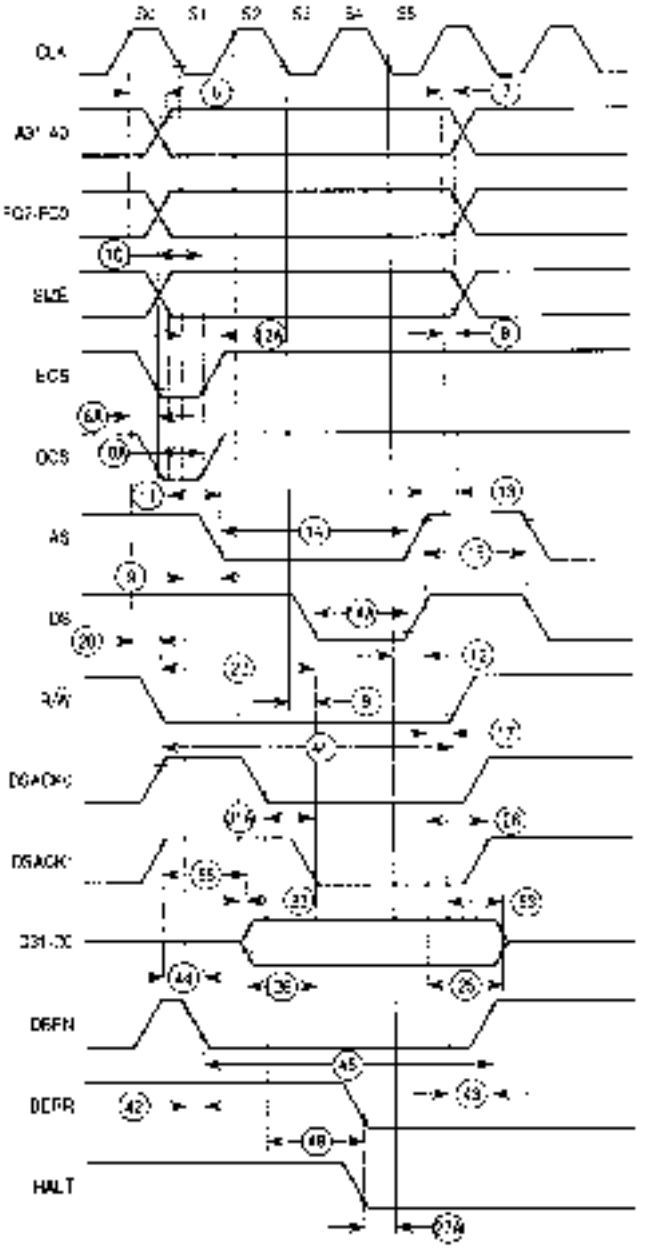
1. This number can be reduced to 5ns if strobes have equal loads.
2. If the asynchronous setup time (#47A) requirements are satisfied, the $\overline{DSACK}$x low data setup time (#31) and $\overline{DSACK}$x low to $\overline{BERR}$ low setup time (#48) can be ignored. The data must only satisfy the data-in to clock low setup time (#27) for the following clock cycle, and $\overline{BERR}$ must only satisfy the late $\overline{BERR}$ low to clock low setup time (#27A) for the following clock cycle.
3. This parameter specifies the maximum allowable skew between $\overline{DSACK0}$ to $\overline{DSACK1}$ asserted or $\overline{DSACK1}$ to $\overline{DSACK0}$ asserted; specification #47A must be met by $\overline{DSACK0}$ or $\overline{DSACK1}$.
4. This specification applies to the first ($\overline{DSACK0}$ or $\overline{DSACK1}$) $\overline{DSACK}$x signal asserted. In the absence of $\overline{DSACK}$x, $\overline{BERR}$ is an asynchronous input setup time (347A).
5. $\overline{DBEN}$ may stay asserted on consecutive write cycles.
6. The minimum values must be met to guarantee proper operation. If this maximum value is exceeded, BG may be reasserted.
7. This specification indicates the minimum high time for $\overline{ECS}$ and $\overline{OCS}$ in the event of an internal cache hit followed immediately by a cache miss or operand cycle.
8. This specification guarantees operation with the 68881/68882, which specifies a minimum time for $\overline{DS}$ negated to $\overline{AS}$ asserted. Without this specification, incorrect interpretation of specifications #9A and #15 would indicate that the WC32P020-XXM does not meet the 68881/68882 requirements.
9. This specification allows a system designer to guarantee data hold times on the output side of data buffers that have output enable signals generated with $\overline{DBEN}$.
10. These specifications allow system designers to guarantee that an alternate bus master has stopped driving the bus when the 68020 regains control of the bus after an arbitration sequence.
11. This specification allows system designers to qualify the $\overline{CS}$ signal of an 68881/68882 with $\overline{AS}$ (allowing 7 ns for a gate delay) and still meet the $\overline{CS}$ to $\overline{DS}$ setup time requirement.

FIG. 6
READ CYCLE TIMING DIAGRAM



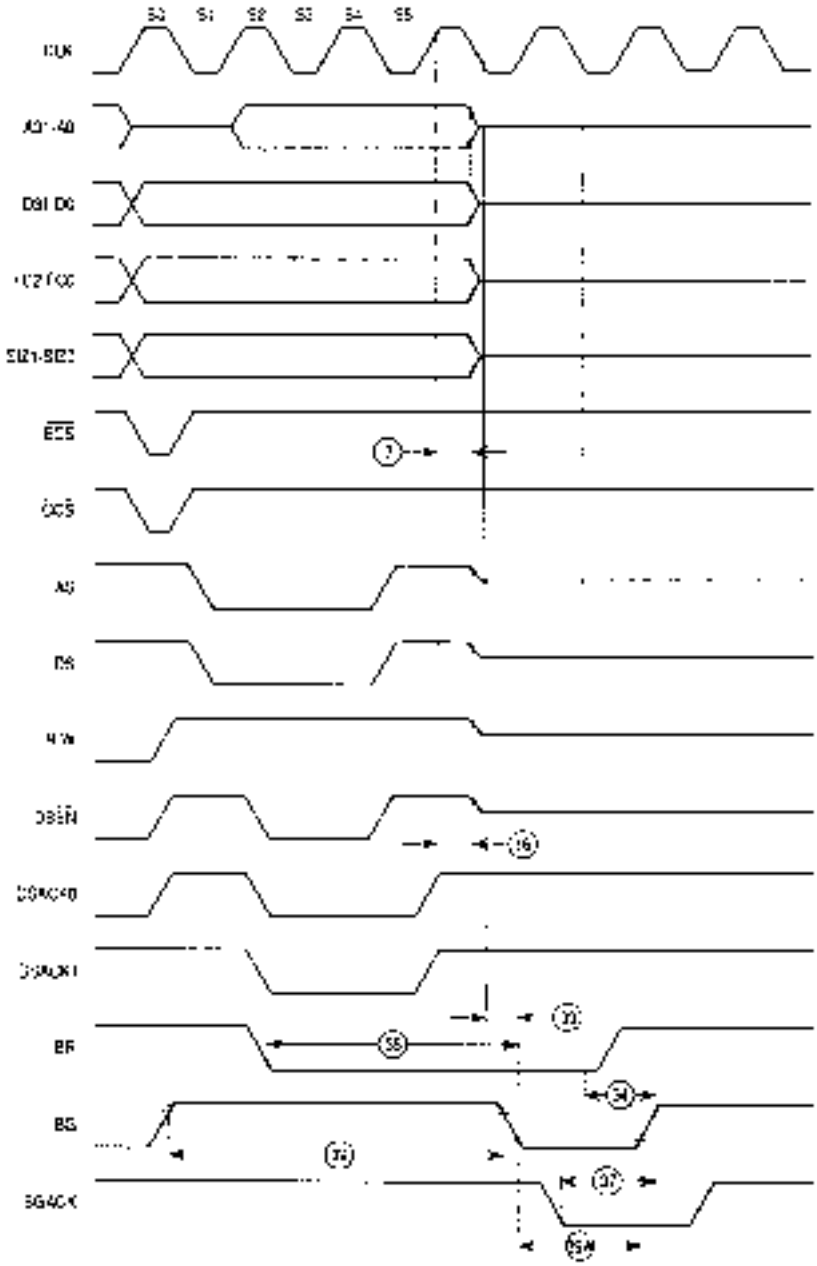
NOTE:
Timing measurements are referenced to and from a low 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8V and 2.0V.

FIG. 7
WRITE CYCLE TIMING DIAGRAM



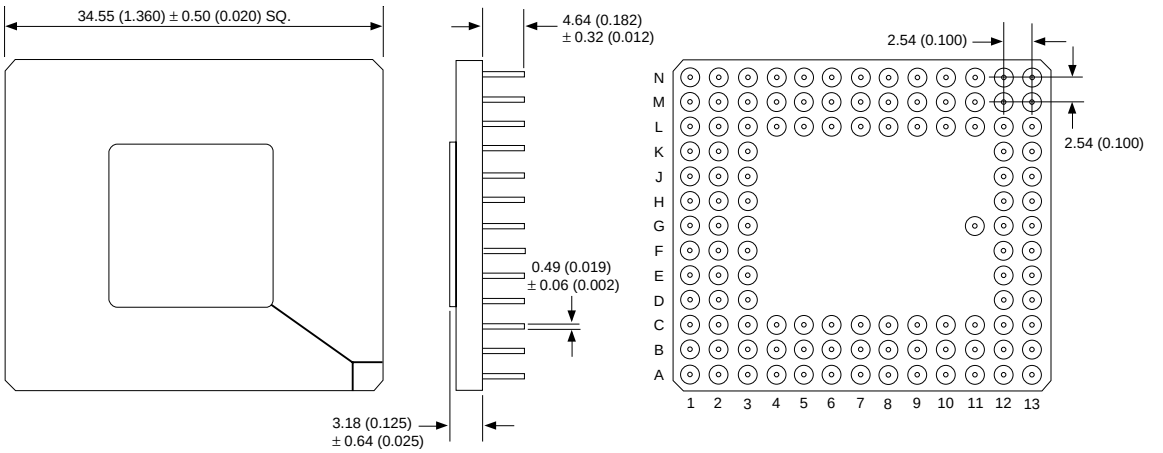
NOTE:
Timing measurements are referenced to and from a low 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8V and 2.0V.

FIG. 8
BUS ARBITRATION TIMING DIAGRAM



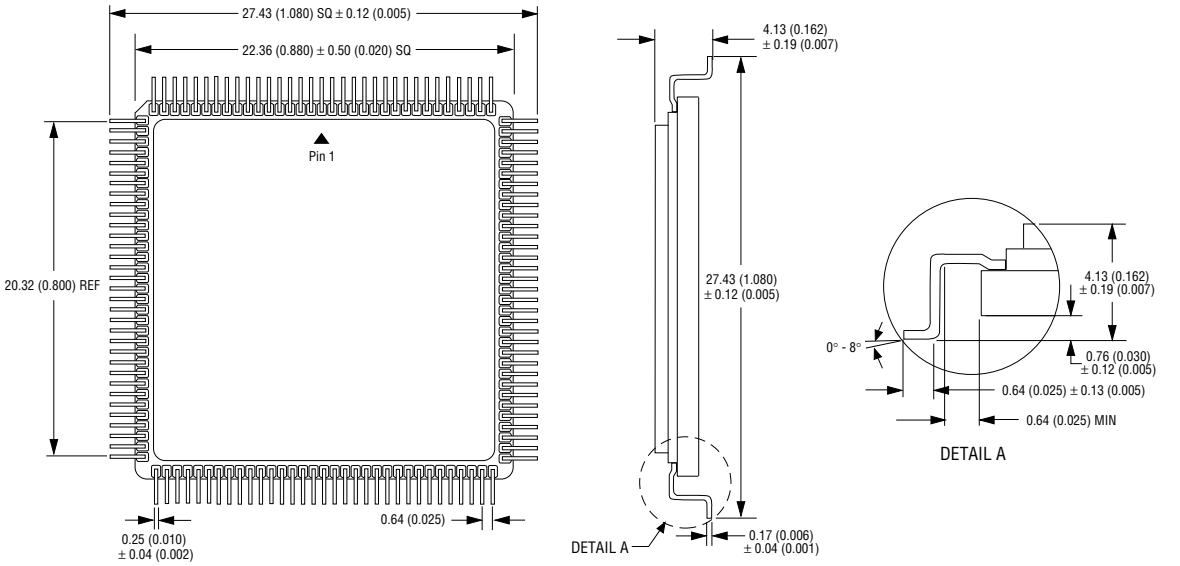
NOTE:
Timing measurements are referenced to and from a low 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8V and 2.0V.

FIG. 9 114 PIN GRID ARRAY, PGA (P2)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

FIG. 10 132 LEAD, CERAMIC QUAD FLAT PACK, CQFP (Q2)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

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